

**LVDS HF VCXO  
SU-A3DCXXX Series**

**Description**

The **SU-A3DCXXX Series** of voltage controlled crystal oscillators (VCXO) provides high frequency with LVDS complementary outputs. The outputs can be disabled for test automation or combining multiple clocks. The device does not use any frequency multiplication, providing exceptionally low Phase Noise and Jitter. It is packaged in a miniature, FR-4 based 9x14mm SMD package.

**Applications and Features**

- Wide frequency range – 12.0MHz to 280.000MHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SONET/SDH
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Extremely Low Phase Noise and Jitter
- High shock resistance, to 1000g
- No Multiplication
- Absolute Pull Range (APR) to ±100 ppm
- SONET ±20 ppm overall free-run stability available
- RoHS Compliant, Lead Free Construction

| Creating a Part Number         |                     |                                 |                   |
|--------------------------------|---------------------|---------------------------------|-------------------|
| <b>SU - A 3DC X X X - FREQ</b> |                     |                                 |                   |
| <b>Package Code</b>            | _____               | <b>Absolute Pull Range, ppm</b> | _____             |
| SU                             | 6 pad 9x14 mm SMD   | E                               | ±20               |
|                                |                     | F                               | ±32               |
|                                |                     | G                               | ±50               |
|                                |                     | H                               | ±100              |
|                                |                     | 9                               | Customer specific |
| <b>Input Voltage</b>           | _____               | <b>Temperature Range, °C</b>    | _____             |
| A                              | 3.3V±5%             | A                               | 0 to 50           |
|                                |                     | B                               | 0 to 70           |
|                                |                     | C                               | -20 to 70         |
|                                |                     | D                               | -40 to 85         |
|                                |                     | 9                               | Customer specific |
| <b>Enable Option</b>           | _____               |                                 |                   |
| H                              | Positive CMOS level |                                 |                   |
| N                              | N/A                 |                                 |                   |



SU-A3DCXXX Series Continued  
LVDS HF VCXO

Rev. B

### Absolute Maximum Ratings

| Parameter                   | Symbol  | Value       | Unit |
|-----------------------------|---------|-------------|------|
| Operating Temperature Range | To      | -40 to +85  | °C   |
| Storage Temperature Range   | Tst     | -50 to +90  | °C   |
| Supply Voltage              | Vcc     | -0.5 to 4.5 | V    |
| Enable/Disable Voltage      | Ven/dis | 0 to Vcc    | V    |

### Electrical Parameters

| Parameter             | Symb                    | Conditions, Note  | MIN   | TYP   | MAX   | Unit   |    |
|-----------------------|-------------------------|---|---|---|---|--------|----|
| Nominal Frequency     | Fo                      |   | 12  |   | 280   | MHz    |    |
| Supply Voltage        | Vcc                     | Code A  | 3.135   | 3.3   | 3.465                                       | V      |    |
| Supply current        | Icc                     |   |   | 80  | 100   | mA     |    |
| Output Logic Type     |                         |   |   | LVDS  |   |        |    |
| Load                  |                         | At receiving end between the outputs  | 90  | 100   | 110   | Ohm    |    |
| Output Levels         | Vod                     | Differential amplitude  | 247   | 330   | 454   | mV     |    |
|                       |                         | Amplitude error   |   |   | 50  | mV     |    |
|                       | Vof                     | Offset Voltage  | 1.125   | 1.25  | 1.375                                       | V      |    |
|                       |                         | Offset Voltage error  |   |   | 50  | mV     |    |
| Duty Cycle (Symmetry) |                         | At outputs crossing, room temperature   | 45/55   | 50/50                                       | 55/45                                       | %      |    |
| Rise/Fall Time        | Tr/Tf                   | 20 to 80, 80 to 20 %  |   | 0.5   | 0.7   | ns     |    |
| <b>Jitter</b>         | Integrated              | J   | Integrated from Phase Noise, 12 KHz to 20 MHz, RMS          |   | 0.1   | 0.2    | ps |
|                       |                         |   |   |   |   | 1.0    | ps |
|                       |                         |   |   |   | 0.3   | ps     |    |
|                       | Wavecrest characterized |   | Random period,  |   | 2.5   |        | ps |
|                       |                         |   | Accumul., pk-to-pk  |   | 17  |        | ps |
|                       |                         |   | Deterministic   |   | 0   |        | ps |
| Sub-Harmonics         |                         |   |   | None  |   | dBc    |    |
| Phase Noise           | £(Δf)                   | 155.52 MHz, APR 50ppm or less   | @ 10 Hz<br>@100 Hz<br>@1 KHz<br>@10KHz<br>@100KHz<br>@>1MHz | -75<br>-105<br>-128<br>-142<br>-147<br>-147 | -70<br>-100<br>-125<br>-140<br>-145<br>-145 | dBc/Hz |    |
| Frequency Stability   | ΔF/F                    | Overall, including initial calibration, temperature, aging 10 years, shock and vibration @ Vc=Vcc/2; APR 50ppm, or less | ±20   | ±30   |   | ppm    |    |
| Control Voltage Range | Vc                      |   | 0V  |   | Vcc   | V      |    |
| Setability            | Vcs                     | Vc to set F at Fo; T, Vcc, load - nominal, as shipped   | 0.4 Vcc   | 0.5 Vcc                                     | 0.6 Vcc                                     | V      |    |
| Absolute Pull Range   | APR                     | Over all conditions, see part # creation  | 20,32, 50,100   |   |   | ppm    |    |
| Input Impedance       | Zin                     | @ Fmod < 100 KHz  | 50  |   |   | KOhm   |    |
| Modulation Bandwidth  |                         | At Vc = Vcc/2, -3dB   | 20  |   |   | KHz    |    |
| Enable/Disable Option |                         |   |   |   |   |        |    |
| Pin 2 Enabled         |                         | CMOS logic 1 or N/C   | 0.7 Vcc   |   | Vcc   | V      |    |
| Pin 2 Disabled        |                         | CMOS logic 0  | 0   |   | 0.3 Vcc                                     | V      |    |



FREQUENCY  
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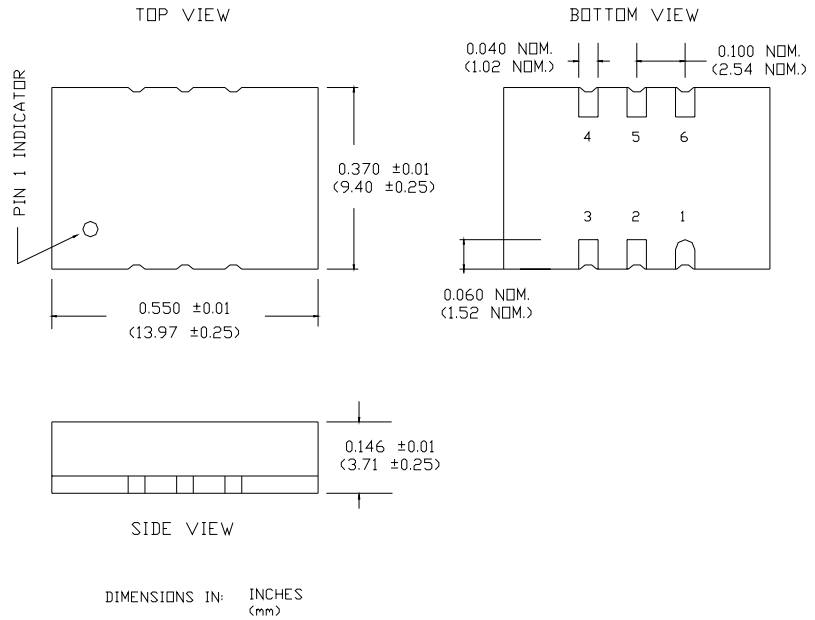
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### SU-A3DCXXX Series Continued

### LVDS HF VCXO

### Electrical Connection

| Pin | Connection        |
|-----|-------------------|
| 1   | V <sub>co</sub>   |
| 2   | Enable/Disable    |
| 3   | Gnd               |
| 4   | Output            |
| 5   | Output Complement |
| 6   | V <sub>cc</sub>   |



## Environmental and Mechanical Characteristics

|                              |   |
|------------------------------|---|
| <b>Operating temp. range</b> | see part # table  |
| <b>Mechanical Shock</b>      | Per MIL-STD-202, Method 213, Cond. E                      |
| <b>Thermal Shock</b>         | Per MIL-STD-883, Method 1011, Cond. A                     |
| <b>Vibration</b>             | Per MIL-STD-883, Method 2007, Cond. A                     |
| <b>Hermetic Seal</b>         | Leak rate less than $1 \times 10^{-8}$ atm.cc/s of helium |
| <b>Soldering conditions</b>  | See MAX reflow profile below                              |

### Maximum Reflow Profile

