SP8402

Very Low Phase Noise Divider by 2^N

September 2005

The SP8402 is a very low phase noise divider which divides by powers of two. The S0, S1, S2 data inputs select the division ratio in the range 2^1 to 2^8. Special circuits techniques have been used to reduce the phase noise considerably below that produced by standard dividers. The data inputs are CMOS or TTL compatible.

The SP8402 is packaged in a 28 pin plastic SO package to be compatible with the SP8400 and SP8401 devices.

FEATURES

- Very low Phase Noise (Typically -155 to 160dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Output Current	20mA
Storage Temperature Range	-55°C to +125°C
Maximum Clock Input Voltage	2.5V p-p

Ordering Information

SP8402/KG/MPES	28 Pin SOIC	Tubes
SP8402/KG/MPFP	28 Pin SOIC*	Tubes
SP8402/KG/MP1T	28 Pin SOIC	Tape & Reel

*Pb Free Matte Tin

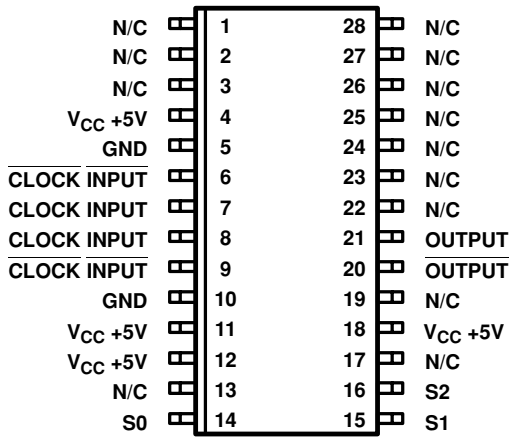


Fig.1 Pin connections - top view

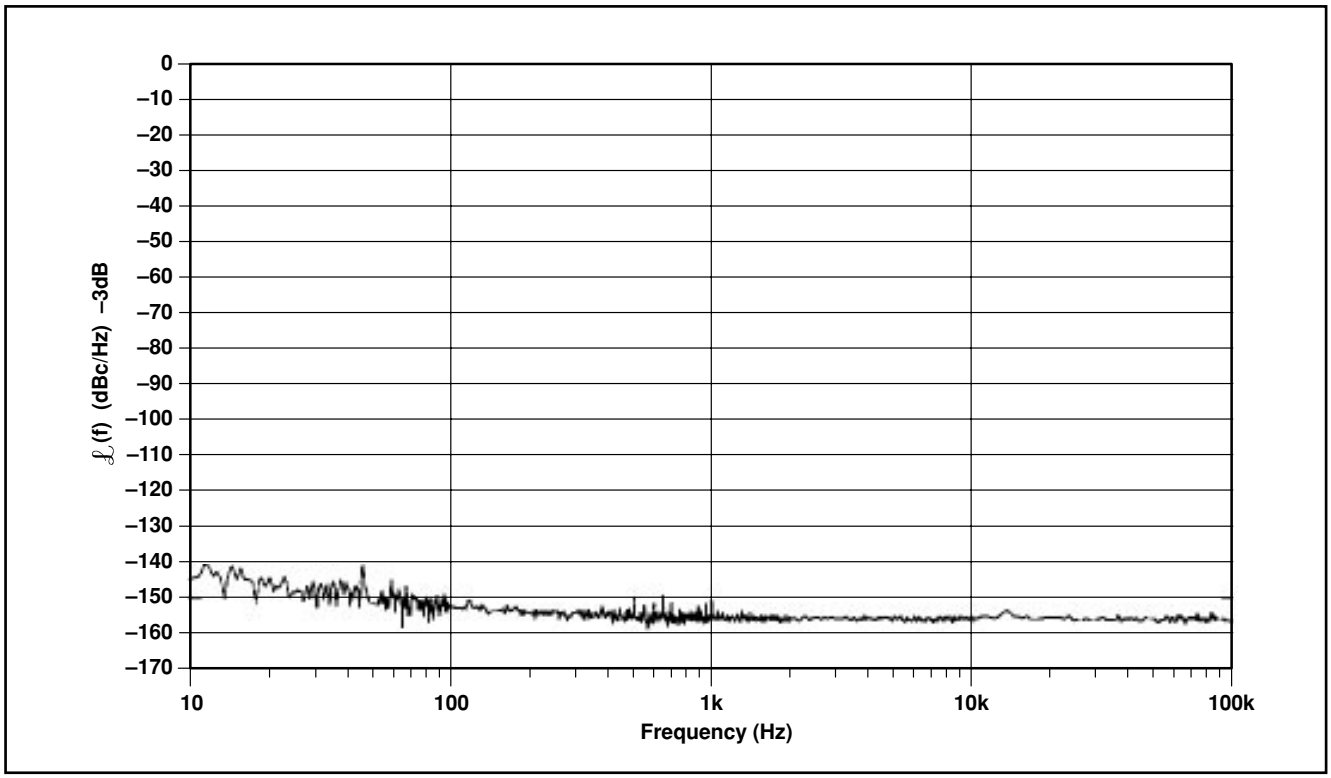


Fig.2 Typical single sideband phase noise measured at 768MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over: Supply voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = -10°C to +75°C
Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	4, 11, 12, 18	82	92	102	mA	Output loaded with 300R See Fig.5
Output voltage swing	20, 21	320	410		mV	p-p @ 1.4GHz input ÷ 256 mode outputs loaded with 330R See Fig.5
Input sensitivity 200MHz to 1.5GHz	7, 8			140	mV	RMS Sine wave into 50 Ohms
				(-4)	dBm	(dBm equivalent) See Fig.3
Data Inputs						
Logic high voltage		2.2			V	
Low low voltage				0.8	V	
Input current				180	µA	5V Data input voltage

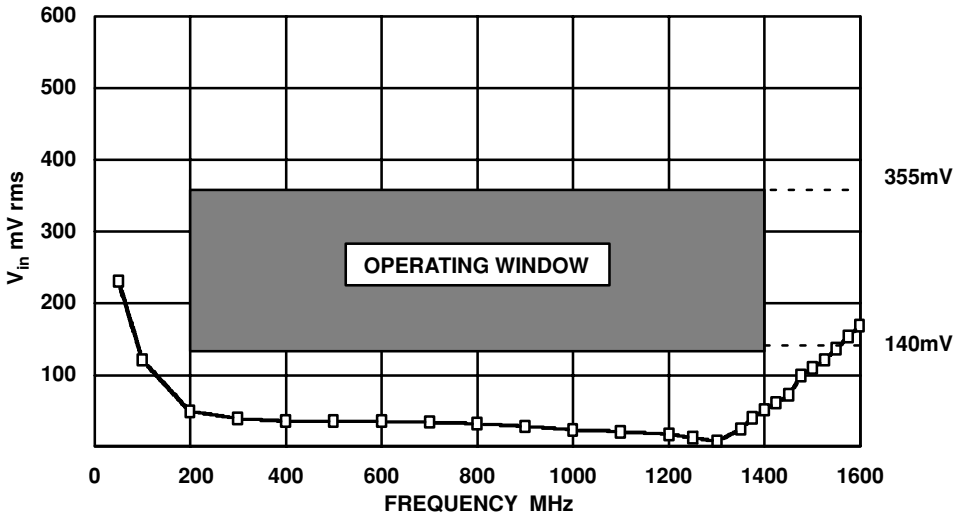


Fig.3 Typical input sensitivity

S0	S1	S2	DIVISION RATIO
L	L	L	2
H	L	L	4
L	H	L	8
H	H	L	16
L	L	H	32
H	L	H	64
L	H	H	128
H	H	H	256

Fig.4 Truth table

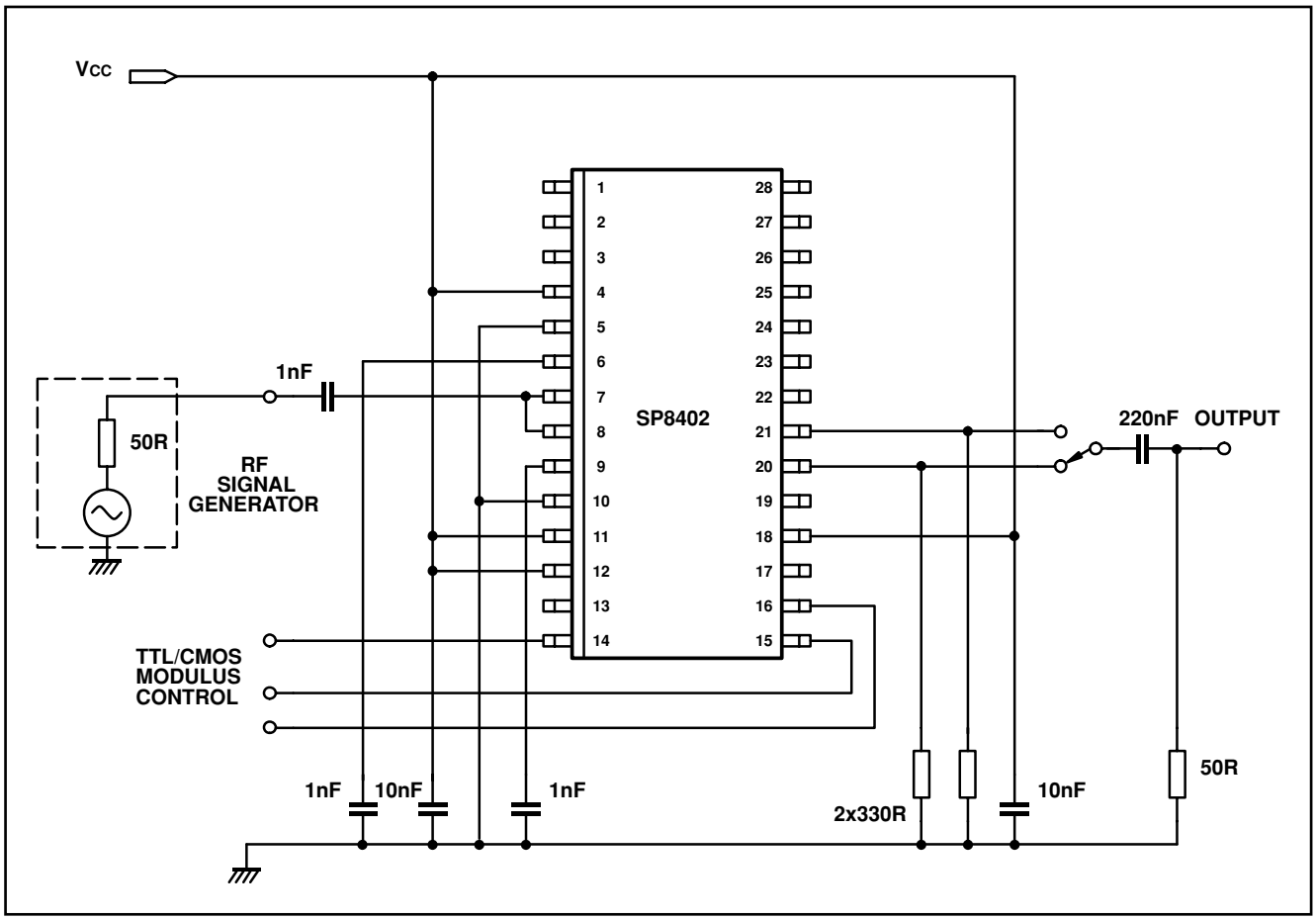


Fig.5 Test circuit

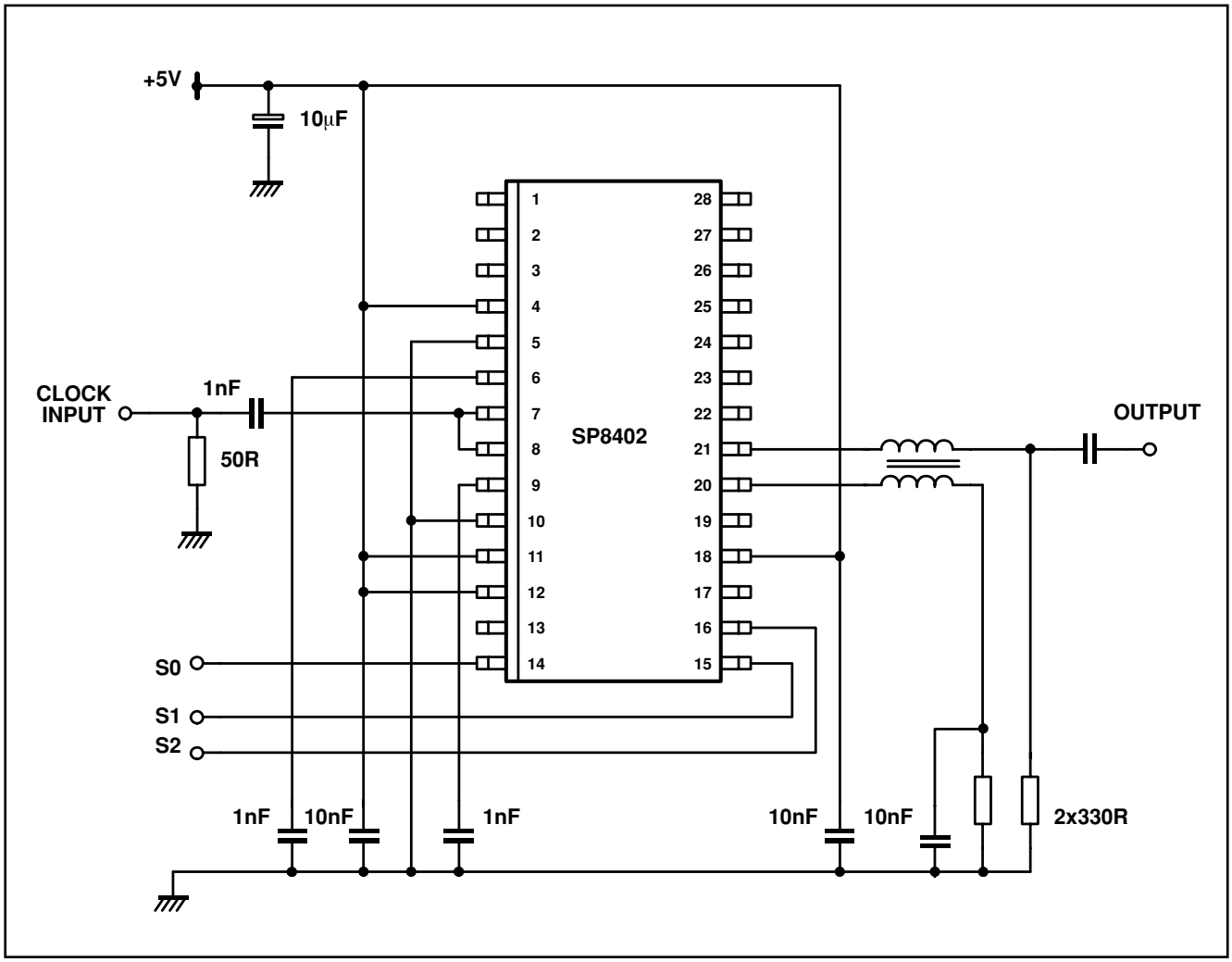
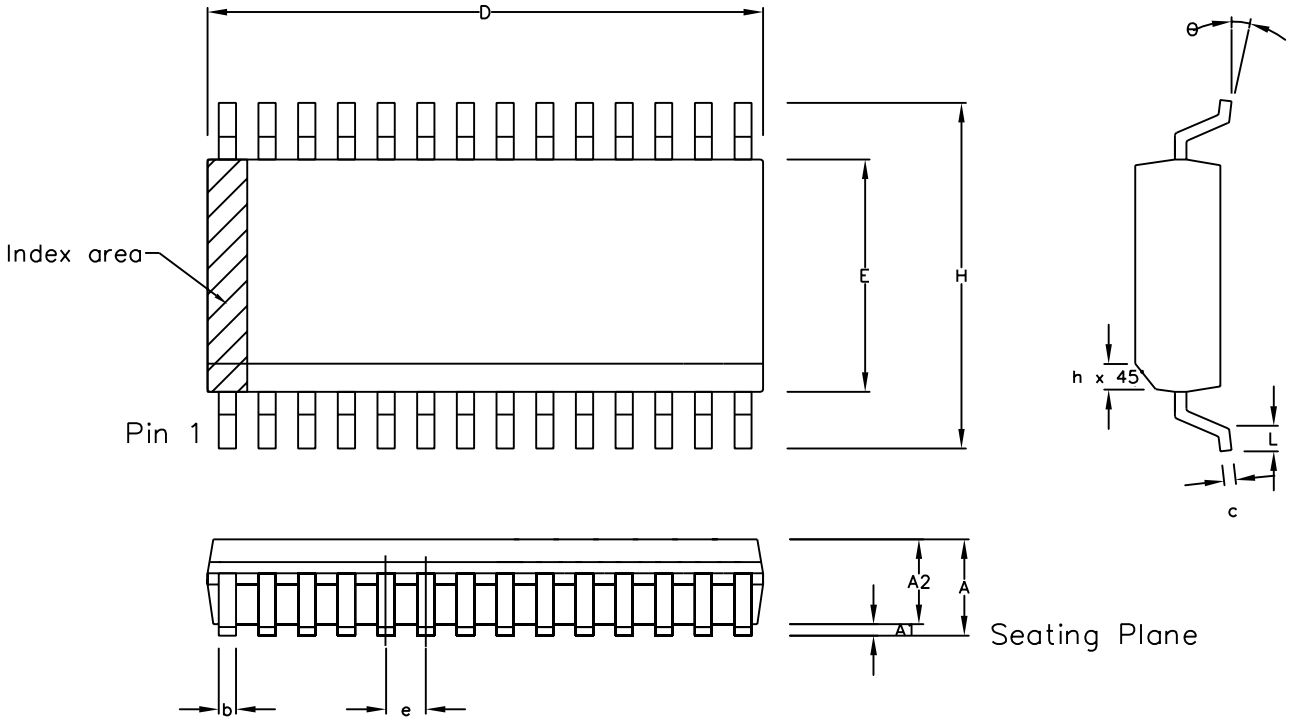


Fig.5 Typical application combining output to increase signal and retain low phase noise



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	17.70		18.10		0.697		0.713
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	28						
Conforms to JEDEC MS-013AE Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201943	213100	
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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for
28 lead SOIC
(0.300" Body Width)

GPD00017

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