P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.015 @ V_{GS} = -10 V	-8
	0.024 @ V_{GS} = -4.5 V	-6.4

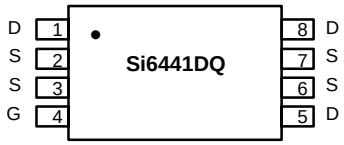
FEATURES

- TrenchFET® Power MOSFET

APPLICATIONS

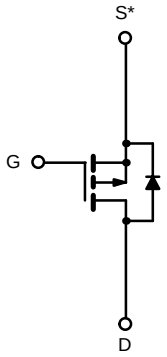
- Battery Switch
- Load Switch

TSSOP-8



Top View

Ordering Information: Si6441DQ-T1



P-Channel MOSFET

* Source Pins 2, 3, 6 and 7 must be tied common.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**10 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	-30		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	-8	-6.3	A
	T_A = 70°C		-6.4	-5.0	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	-30		
Continuous Source Current (Diode Conduction)[a]		I_S	-1.6	-01.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.75	1.08	W
	T_A = 70°C		1.14	0.69	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	55	70	°C/W
	Steady State		95	115	
Maximum Junction-to-Foot	Steady State	R_{thJF}	38	50	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

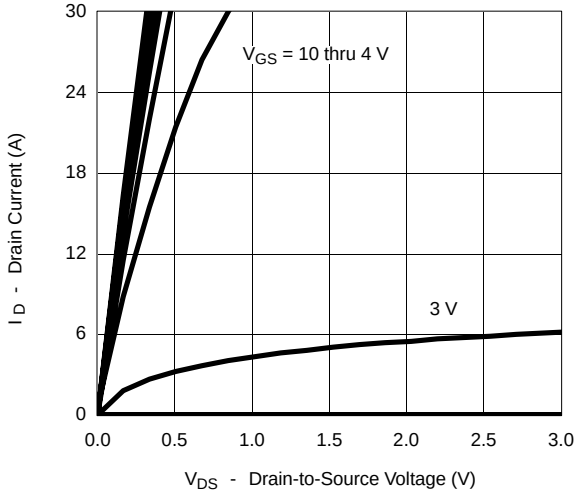
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1		-3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} -5 V, V_{GS} = -10 V	-20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -8 A		0.012	0.015	Ω
		V_{GS} = -4.5 V, I_D = -6.4 A		0.019	0.024	
Forward Transconductance[a]	g_{fs}	V_{DS} = -15 V, I_D = -8 A		25		S
Diode Forward Voltage[a]	V_{SD}	I_S = -1.6 A, V_{GS} = 0 V		-0.75	-1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -15 V, V_{GS} = -5 V, I_D = -8 A		27	40	nC
Gate-Source Charge	Q_{gs}			7.0		
Gate-Drain Charge	Q_{gd}			12.8		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15 V, R_L = 15 Ω I_D ≅ -1 A, V_{GEN} = -10 V, R_G = 6 Ω		15	25	ns
Rise Time	t_r			13	25	
Turn-Off Delay Time	$t_{d(off)}$			95	150	
Fall Time	t_f			56	90	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = -1.6 A, di/dt = 100 A/µs		60	100	

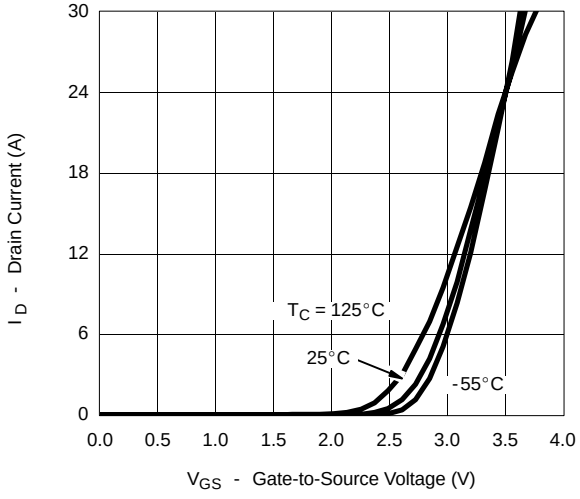
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

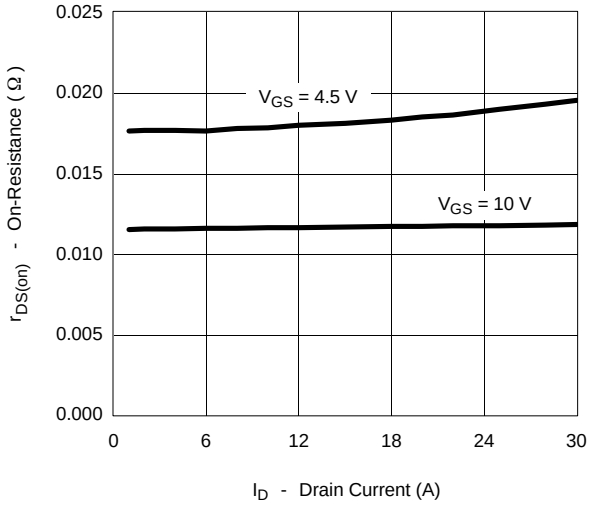


Transfer Characteristics

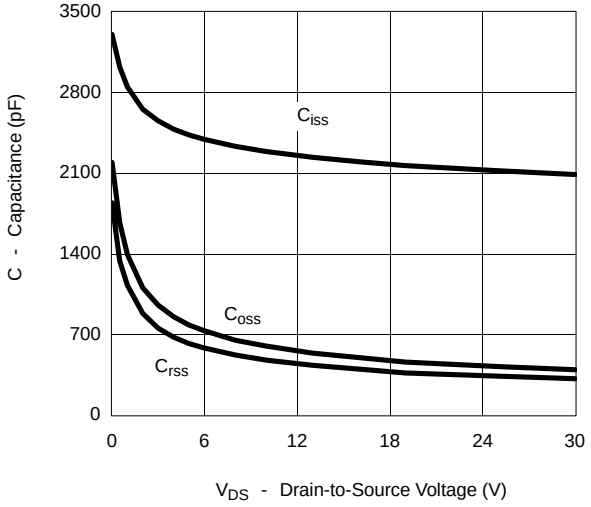


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

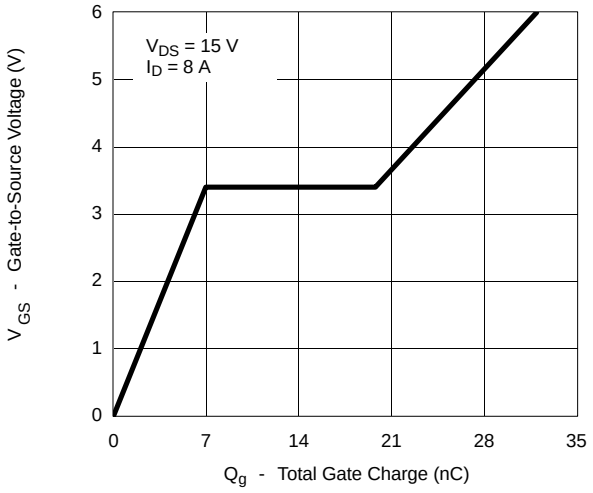
On-Resistance vs. Drain Current



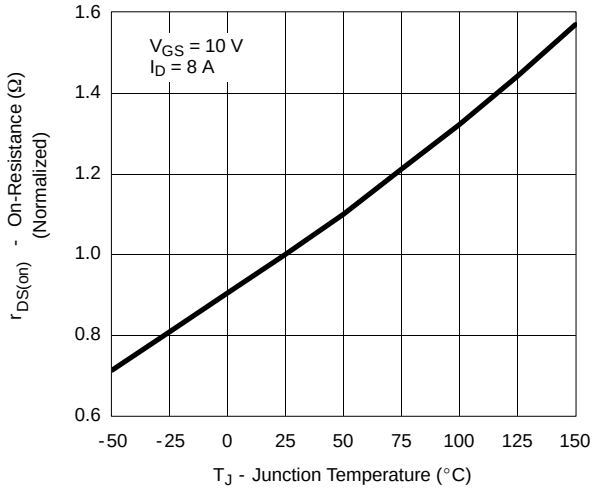
Capacitance



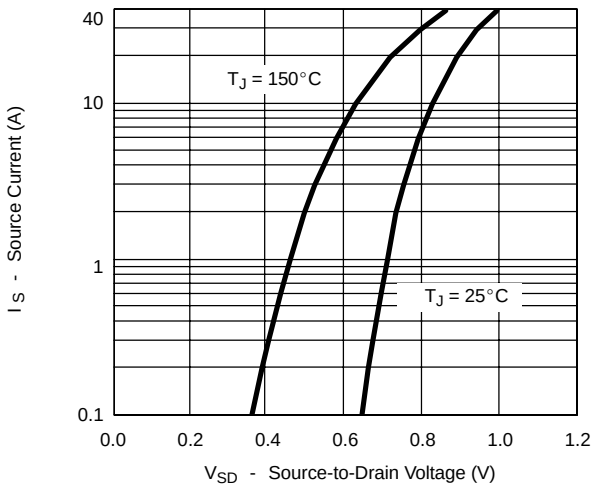
Gate Charge



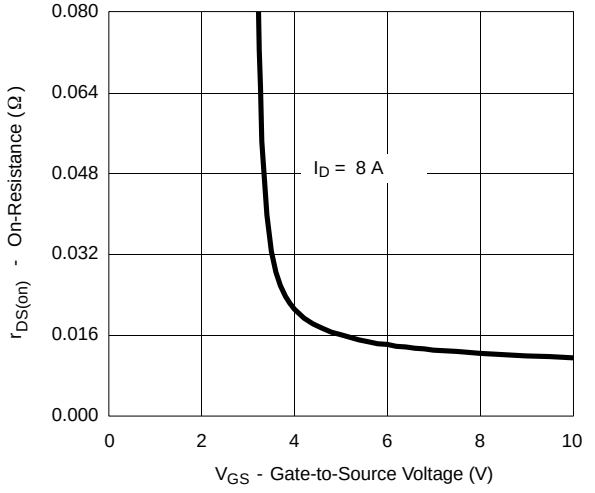
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

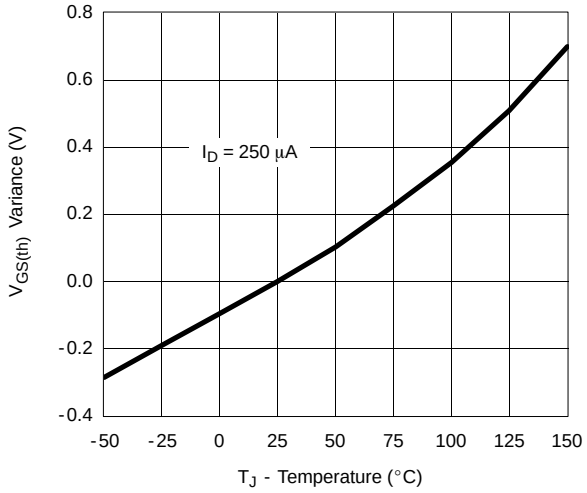


On-Resistance vs. Gate-to-Source Voltage

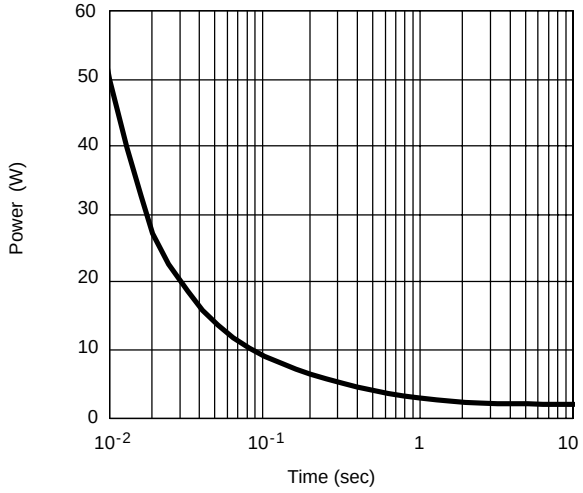


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

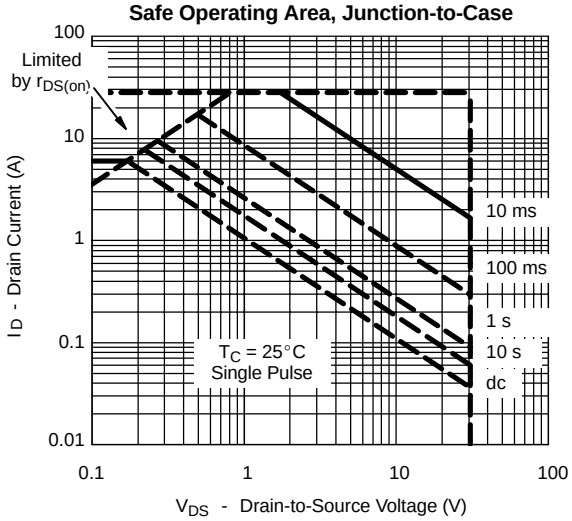
Threshold Voltage



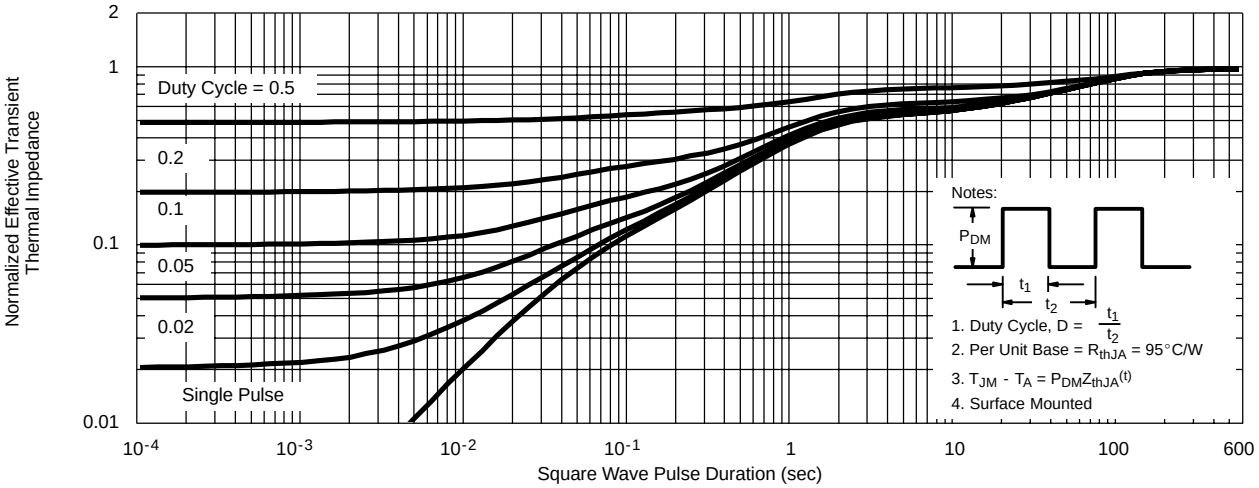
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)