S6C1652

6 BIT 300 / 309 CHANNEL TFT-LCD SOURCE DRIVER

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Ver. 0.0

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S6C1652 Specification Revision History		
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CONTENTS

INTRODUCTION

The S6C1652 is a 300 / 309 channel output, TFT-LCD source driver for an 64 gray-scale LCD panel. Data input is based on digital input consisting of 6 bits by 3 dots, which can realize a full-color display of 260,000 color by output of 64 values gamma-corrected.

This device has an internal D/A (digital-to-analog) converter for each output and 18 (9-by-2) reference voltages. Because the output dynamic range is as large as 6.0 - 12.6 Vp-p, it is unnecessary to operate level inversion of the LCD's common electrode. Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray-scale voltages with different polarity can be output to the odd number output pins and the even output pins.

S6C1652 can be adopted to larger panel, and SHL (shift direction selection) pin makes the use of the LCD panel connection conveniently. Maximum operation clock frequency is 55 MHz at 2.7 V logic operation, single edge and it can be applied to the TFT-LCD panel of SVGA to XGA standard.

FEATURES

- TFT active matrix LCD source driver LSI
- 64 gray-scale is possible through 18 (9-by-2) reference voltages and D/A converter
- Dot inversion display is possible
- CMOS level input
- Compatible with gamma-correction
- Input of 6bits (gray-scale data) by 3 dots (R,G,B)
- Logic supply voltage: 2.7 - 3.6 V
- LCD driver supply voltage: 6.4 - 13.0 V
- Output dynamic range: 6.0 - 12.6 Vp-p
- Maximum operating frequency: fMAX = 55 MHz (internal data transmission rate at 2.7 V operation)
- Output: 300 / 309 outputs
- TCP available

BLOCK DIAGRAM

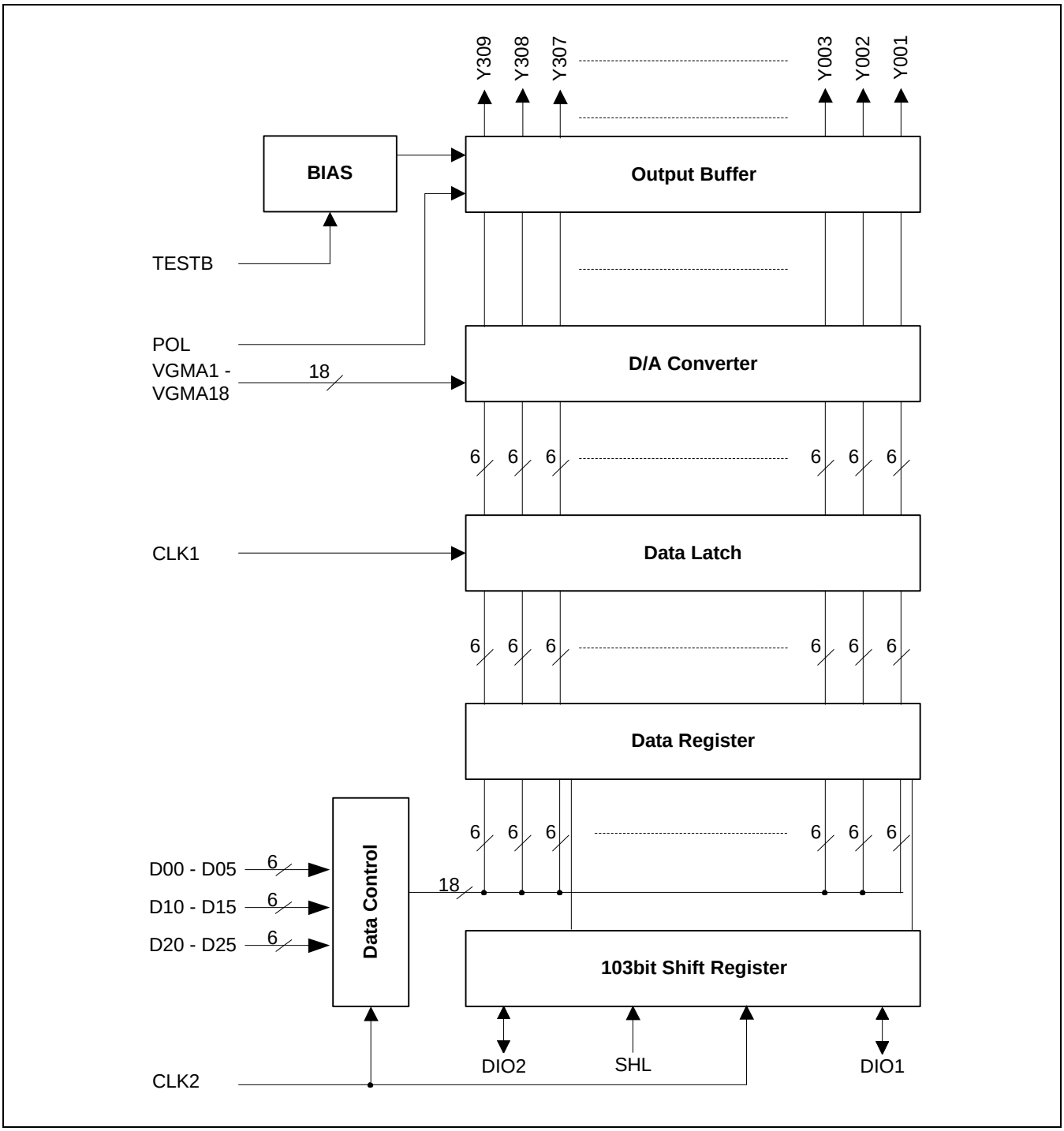

Figure 1. S6C1652 Block Diagram

PIN ASSIGNMENTS

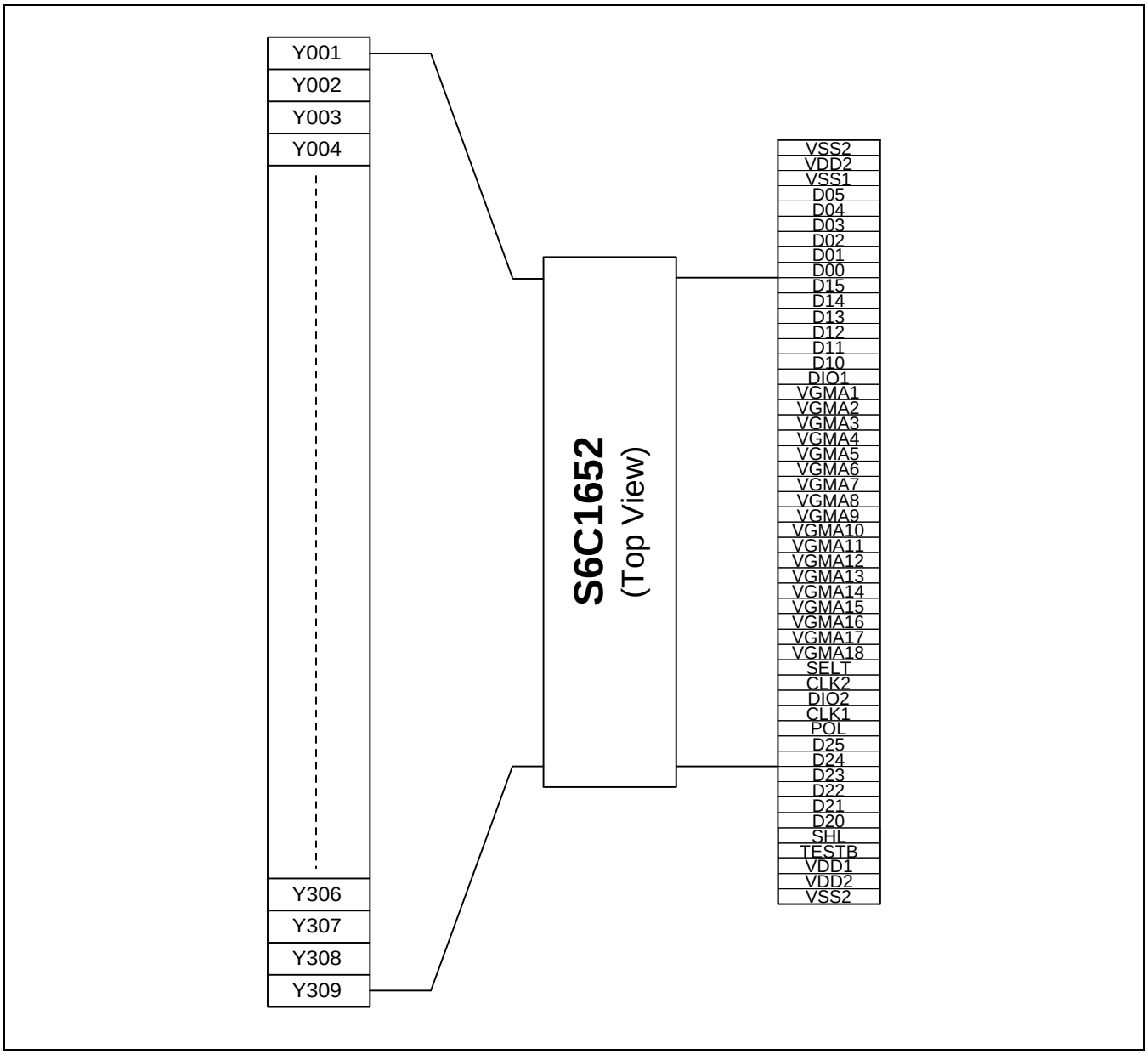

Figure 2. S6C1652 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.7 - 3.6 V
VDD2	Driver power supply	6.4 - 13.0 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 - Y309	Driver outputs	The D/A converted 64 gray-scale analog voltage is output.
D0<0:5> - D2<0:5>	Display data input	The display data is input with a width of 18 bits, gray-scale data (6 bits) by 3 dots (R,G,B) DX0: LSB, DX5: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift registers is as follows. SHL = H: DIO1 input, Y1 → Y309, DIO2 output SHL = L: DIO2 input, Y309 → Y1, DIO1 output
DIO1	Start pulse input / output	SHL = H: Used as the start pulse input pin SHL = L: Used as the start pulse output pin
DIO2	Start pulse input / output	SHL = H: Used as the start pulse output pin SHL = L: Used as the start pulse input pin
POL	Polarity input	POL = H: The reference voltage for odd number outputs are VGMA1 – VGMA9 and those for even number outputs are VGMA10 – VGMA18 POL = L: The reference voltage for odd number outputs are VGMA10 – VGMA18 and those for even number outputs are VGMA1 – VGMA9
CLK2	Shift clock input	Refer to the shift register's shift clock input. The display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	Latches the contents of the data register at rising edge and transfers them to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the "Relationships between CLK1 start pulse (DIO1, DIO2) and blanking period" of the switching characteristic waveform. Outputs the gray-scale data at rising edge.
VGMA1 – VGMA18	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2 > VGMA1 > VGMA2 > …… > VGMA17 > VGMA18 > VSS2 Keep gray-scale power supply unchanged during the gray-scale voltage output.
SELT	Output selection input	SELT = H: 300 Output (Y151 - Y159 are disabled) SELT = L: 309 Output
TESTB	Test input	TESTB = H: Normal operation mode TESTB = L: Test mode (OP AMP CUT-OFF, Rpu = 30kΩ)

OPERATION DESCRIPTION

DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into internal latch on the rising edge of CLK2, DIO1 (or DIO2) pulse enables the data transfer operation. After the falling edge of DIO1 (or DIO2), display data is valid on the rising edge of CLK2. Once all the data of 300 / 309 channels are loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the next rising edge of CLK2 after the falling edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

(1) SHL = "L"

Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

(2) SHL = "H"

Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 18 (9-by-2) gamma corrected power supplies (VGMA1 - VGMA18). Besides, to be able to deal with dot-line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 9-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 9 gamma corrected voltages of VGMA1 - VGMA9 and VGMA10 - VGMA18**.**

SHL = H

OUTPUT	Y1	Y2	Y3	.....	Y307	Y308	Y309
-	First			→	Last		
DATA	D00 - D05	D10 - D15	D20 - D25	.....	D00 - D05	D10 - D15	D20 - D25

SHL = L

OUTPUT	Y1	Y2	Y3	.....	Y307	Y308	Y309
-	Last			←	First		
DATA	D00 - D05	D10 - D15	D20 - D25	.....	D00 - D05	D10 - D15	D20 - D25

Figure 3. Relationship between Shift Direction and Output Data

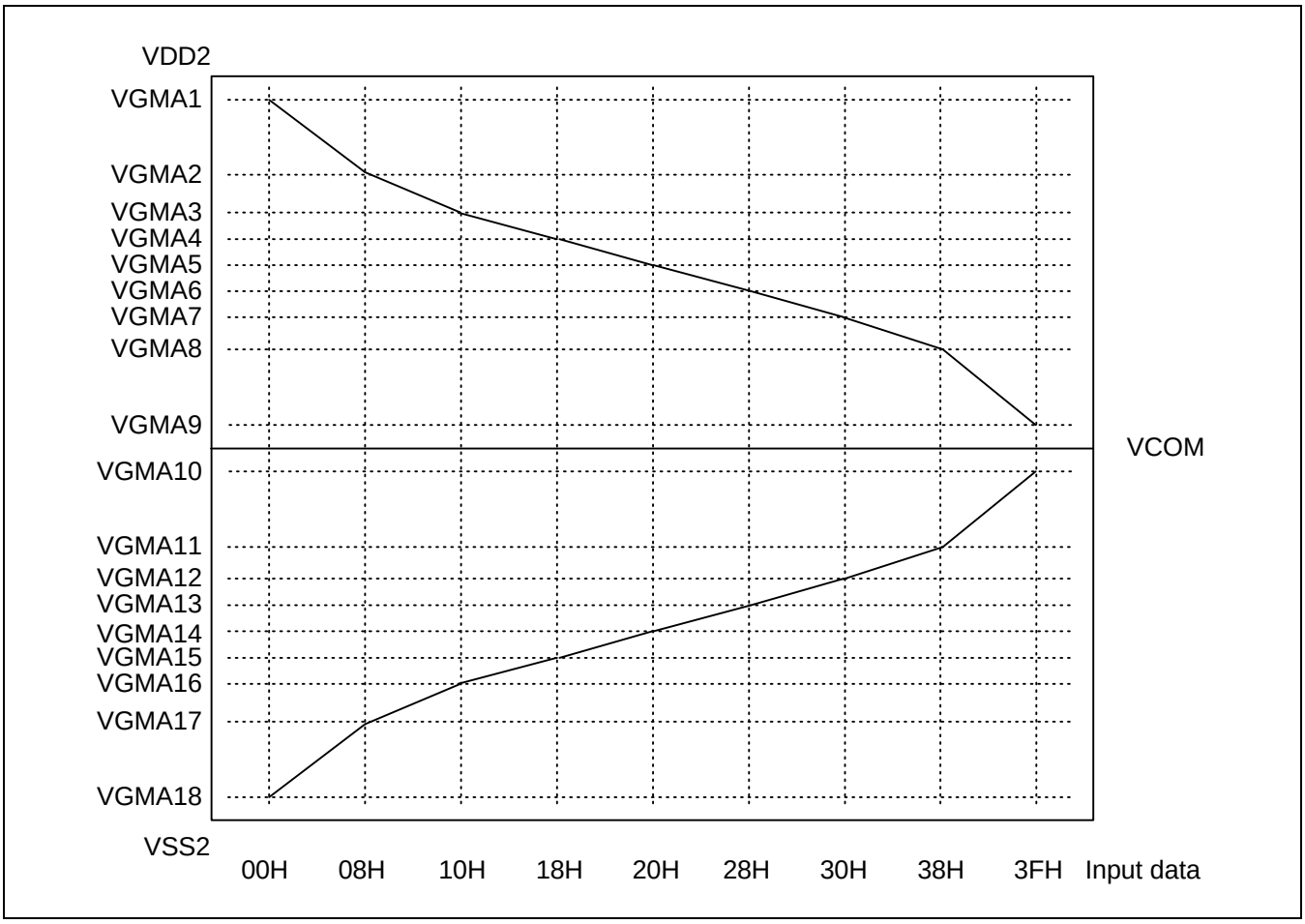

Figure 4. Gamma Correction Curve

Table 1. Resistor Strings (R0 - R63, unit: Ω)

Name	Value	Name	Value	Name	Value	Name	Value
R0	510	R16	170	R32	170	R48	255
R1	510	R17	170	R33	170	R49	255
R2	510	R18	170	R34	170	R50	255
R3	510	R19	170	R35	170	R51	255
R4	510	R20	170	R36	170	R52	255
R5	510	R21	170	R37	170	R53	255
R6	510	R22	170	R38	170	R54	255
R7	510	R23	170	R39	170	R55	255
R8	255	R24	170	R40	170	R56	510
R9	255	R25	170	R41	170	R57	510
R10	255	R26	170	R42	170	R58	510
R11	255	R27	170	R43	170	R59	510
R12	255	R28	170	R44	170	R60	510
R13	255	R29	170	R45	170	R61	510
R14	255	R30	170	R46	170	R62	510
R15	255	R31	170	R47	170	R63	510

Table 2. Relationship between Input Data and Output Voltage Value

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	VGMA1 + (VGMA2 - VGMA1) × 1 / 8
02H	0	0	0	0	1	0	VH2	VGMA1 + (VGMA2 - VGMA1) × 2 / 8
03H	0	0	0	0	1	1	VH3	VGMA1 + (VGMA2 - VGMA1) × 3 / 8
04H	0	0	0	1	0	0	VH4	VGMA1 + (VGMA2 - VGMA1) × 4 / 8
05H	0	0	0	1	0	1	VH5	VGMA1 + (VGMA2 - VGMA1) × 5 / 8
06H	0	0	0	1	1	0	VH6	VGMA1 + (VGMA2 - VGMA1) × 6 / 8
07H	0	0	0	1	1	1	VH7	VGMA1 + (VGMA2 - VGMA1) × 7 / 8
08H	0	0	1	0	0	0	VH8	VGMA2
09H	0	0	1	0	0	1	VH9	VGMA2 + (VGMA3 - VGMA2) × 1 / 8
0AH	0	0	1	0	1	0	VH10	VGMA2 + (VGMA3 - VGMA2) × 2 / 8
0BH	0	0	1	0	1	1	VH11	VGMA2 + (VGMA3 - VGMA2) × 3 / 8
0CH	0	0	1	1	0	0	VH12	VGMA2 + (VGMA3 - VGMA2) × 4 / 8
0DH	0	0	1	1	0	1	VH13	VGMA2 + (VGMA3 - VGMA2) × 5 / 8
0EH	0	0	1	1	1	0	VH14	VGMA2 + (VGMA3 - VGMA2) × 6 / 8
0FH	0	0	1	1	1	1	VH15	VGMA2 + (VGMA3 - VGMA2) × 7 / 8
10H	0	1	0	0	0	0	VH16	VGMA3
11H	0	1	0	0	0	1	VH17	VGMA3 + (VGMA4 - VGMA3) × 1 / 8
12H	0	1	0	0	1	0	VH18	VGMA3 + (VGMA4 - VGMA3) × 2 / 8
13H	0	1	0	0	1	1	VH19	VGMA3 + (VGMA4 - VGMA3) × 3 / 8
14H	0	1	0	1	0	0	VH20	VGMA3 + (VGMA4 - VGMA3) × 4 / 8
15H	0	1	0	1	0	1	VH21	VGMA3 + (VGMA4 - VGMA3) × 5 / 8
16H	0	1	0	1	1	0	VH22	VGMA3 + (VGMA4 - VGMA3) × 6 / 8
17H	0	1	0	1	1	1	VH23	VGMA3 + (VGMA4 - VGMA3) × 7 / 8
18H	0	1	1	0	0	0	VH24	VGMA4
19H	0	1	1	0	0	1	VH25	VGMA4 + (VGMA5 - VGMA4) × 1 / 8
1AH	0	1	1	0	1	0	VH26	VGMA4 + (VGMA5 - VGMA4) × 2 / 8
1BH	0	1	1	0	1	1	VH27	VGMA4 + (VGMA5 - VGMA4) × 3 / 8
1CH	0	1	1	1	0	0	VH28	VGMA4 + (VGMA5 - VGMA4) × 4 / 8
1DH	0	1	1	1	0	1	VH29	VGMA4 + (VGMA5 - VGMA4) × 5 / 8
1EH	0	1	1	1	1	0	VH30	VGMA4 + (VGMA5 - VGMA4) × 6 / 8
1FH	0	1	1	1	1	1	VH31	VGMA4 + (VGMA5 - VGMA4) × 7 / 8

NOTE: VDD2>VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGMA9

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VH32	VGMA5
21H	1	0	0	0	0	1	VH33	VGMA5 + (VGMA6 - VGMA5) × 1 / 8
22H	1	0	0	0	1	0	VH34	VGMA5 + (VGMA6 - VGMA5) × 2 / 8
23H	1	0	0	0	1	1	VH35	VGMA5 + (VGMA6 - VGMA5) × 3 / 8
24H	1	0	0	1	0	0	VH36	VGMA5 + (VGMA6 - VGMA5) × 4 / 8
25H	1	0	0	1	0	1	VH37	VGMA5 + (VGMA6 - VGMA5) × 5 / 8
26H	1	0	0	1	1	0	VH38	VGMA5 + (VGMA6 - VGMA5) × 6 / 8
27H	1	0	0	1	1	1	VH39	VGMA5 + (VGMA6 - VGMA5) × 7 / 8
28H	1	0	1	0	0	0	VH40	VGMA6
29H	1	0	1	0	0	1	VH41	VGMA6 + (VGMA7 - VGMA6) × 1 / 8
2AH	1	0	1	0	1	0	VH42	VGMA6 + (VGMA7 - VGMA6) × 2 / 8
2BH	1	0	1	0	1	1	VH43	VGMA6 + (VGMA7 - VGMA6) × 3 / 8
2CH	1	0	1	1	0	0	VH44	VGMA6 + (VGMA7 - VGMA6) × 4 / 8
2DH	1	0	1	1	0	1	VH45	VGMA6 + (VGMA7 - VGMA6) × 5 / 8
2EH	1	0	1	1	1	0	VH46	VGMA6 + (VGMA7 - VGMA6) × 6 / 8
2FH	1	0	1	1	1	1	VH47	VGMA6 + (VGMA7 - VGMA6) × 7 / 8
30H	1	1	0	0	0	0	VH48	VGMA7
31H	1	1	0	0	0	1	VH49	VGMA7 + (VGMA8 - VGMA7) × 1 / 8
32H	1	1	0	0	1	0	VH50	VGMA7 + (VGMA8 - VGMA7) × 2 / 8
33H	1	1	0	0	1	1	VH51	VGMA7 + (VGMA8 - VGMA7) × 3 / 8
34H	1	1	0	1	0	0	VH52	VGMA7 + (VGMA8 - VGMA7) × 4 / 8
35H	1	1	0	1	0	1	VH53	VGMA7 + (VGMA8 - VGMA7) × 5 / 8
36H	1	1	0	1	1	0	VH54	VGMA7 + (VGMA8 - VGMA7) × 6 / 8
37H	1	1	0	1	1	1	VH55	VGMA7 + (VGMA8 - VGMA7) × 7 / 8
38H	1	1	1	0	0	0	VH56	VGMA8
39H	1	1	1	0	0	1	VH57	VGMA8 + (VGMA9 - VGMA8) × 1 / 8
3AH	1	1	1	0	1	0	VH58	VGMA8 + (VGMA9 - VGMA8) × 2 / 8
3BH	1	1	1	0	1	1	VH59	VGMA8 + (VGMA9 - VGMA8) × 3 / 8
3CH	1	1	1	1	0	0	VH60	VGMA8 + (VGMA9 - VGMA8) × 4 / 8
3DH	1	1	1	1	0	1	VH61	VGMA8 + (VGMA9 - VGMA8) × 5 / 8
3EH	1	1	1	1	1	0	VH62	VGMA8 + (VGMA9 - VGMA8) × 6 / 8
3FH	1	1	1	1	1	1	VH63	VGMA8 + (VGMA9 - VGMA8) × 7 / 8

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VL0	VGMA18
01H	0	0	0	0	0	1	VL1	VGMA18 + (VGMA17 - VGMA18) × 1 / 8
02H	0	0	0	0	1	0	VL2	VGMA18 + (VGMA17 - VGMA18) × 2 / 8
03H	0	0	0	0	1	1	VL3	VGMA18 + (VGMA17 - VGMA18) × 3 / 8
04H	0	0	0	1	0	0	VL4	VGMA18 + (VGMA17 - VGMA18) × 4 / 8
05H	0	0	0	1	0	1	VL5	VGMA18 + (VGMA17 - VGMA18) × 5 / 8
06H	0	0	0	1	1	0	VL6	VGMA18 + (VGMA17 - VGMA18) × 6 / 8
07H	0	0	0	1	1	1	VL7	VGMA18 + (VGMA17 - VGMA18) × 7 / 8
08H	0	0	1	0	0	0	VL8	VGMA17
09H	0	0	1	0	0	1	VL9	VGMA17 + (VGMA16 - VGMA17) × 1 / 8
0AH	0	0	1	0	1	0	VL10	VGMA17 + (VGMA16 - VGMA17) × 2 / 8
0BH	0	0	1	0	1	1	VL11	VGMA17 + (VGMA16 - VGMA17) × 3 / 8
0CH	0	0	1	1	0	0	VL12	VGMA17 + (VGMA16 - VGMA17) × 4 / 8
0DH	0	0	1	1	0	1	VL13	VGMA17 + (VGMA16 - VGMA17) × 5 / 8
0EH	0	0	1	1	1	0	VL14	VGMA17 + (VGMA16 - VGMA17) × 6 / 8
0FH	0	0	1	1	1	1	VL15	VGMA17 + (VGMA16 - VGMA17) × 7 / 8
10H	0	1	0	0	0	0	VL16	VGMA16
11H	0	1	0	0	0	1	VL17	VGMA16 + (VGMA15 - VGMA16) × 1 / 8
12H	0	1	0	0	1	0	VL18	VGMA16 + (VGMA15 - VGMA16) × 2 / 8
13H	0	1	0	0	1	1	VL19	VGMA16 + (VGMA15 - VGMA16) × 3 / 8
14H	0	1	0	1	0	0	VL20	VGMA16 + (VGMA15 - VGMA16) × 4 / 8
15H	0	1	0	1	0	1	VL21	VGMA16 + (VGMA15 - VGMA16) × 5 / 8
16H	0	1	0	1	1	0	VL22	VGMA16 + (VGMA15 - VGMA16) × 6 / 8
17H	0	1	0	1	1	1	VL23	VGMA16 + (VGMA15 - VGMA16) × 7 / 8
18H	0	1	1	0	0	0	VL24	VGMA15
19H	0	1	1	0	0	1	VL25	VGMA15 + (VGMA14 - VGMA15) × 1 / 8
1AH	0	1	1	0	1	0	VL26	VGMA15 + (VGMA14 - VGMA15) × 2 / 8
1BH	0	1	1	0	1	1	VL27	VGMA15 + (VGMA14 - VGMA15) × 3 / 8
1CH	0	1	1	1	0	0	VL28	VGMA15 + (VGMA14 - VGMA15) × 4 / 8
1DH	0	1	1	1	0	1	VL29	VGMA15 + (VGMA14 - VGMA15) × 5 / 8
1EH	0	1	1	1	1	0	VL30	VGMA15 + (VGMA14 - VGMA15) × 6 / 8
1FH	0	1	1	1	1	1	VL31	VGMA15 + (VGMA14 - VGMA15) × 7 / 8

NOTE: VGMA10>VGMA11>VGMA12>VGMA13>VGMA14>VGMA15>VGMA16>VGMA17>VGMA18>VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VL32	VGMA14
21H	1	0	0	0	0	1	VL33	VGMA14 + (VGMA13 - VGMA14) × 1 / 8
22H	1	0	0	0	1	0	VL34	VGMA14 + (VGMA13 - VGMA14) × 2 / 8
23H	1	0	0	0	1	1	VL35	VGMA14 + (VGMA13 - VGMA14) × 3 / 8
24H	1	0	0	1	0	0	VL36	VGMA14 + (VGMA13 - VGMA14) × 4 / 8
25H	1	0	0	1	0	1	VL37	VGMA14 + (VGMA13 - VGMA14) × 5 / 8
26H	1	0	0	1	1	0	VL38	VGMA14 + (VGMA13 - VGMA14) × 6 / 8
27H	1	0	0	1	1	1	VL39	VGMA14 + (VGMA13 - VGMA14) × 7 / 8
28H	1	0	1	0	0	0	VL40	VGMA13
29H	1	0	1	0	0	1	VL41	VGMA13 + (VGMA12 - VGMA13) × 1 / 8
2AH	1	0	1	0	1	0	VL42	VGMA13 + (VGMA12 - VGMA13) × 2 / 8
2BH	1	0	1	0	1	1	VL43	VGMA13 + (VGMA12 - VGMA13) × 3 / 8
2CH	1	0	1	1	0	0	VL44	VGMA13 + (VGMA12 - VGMA13) × 4 / 8
2DH	1	0	1	1	0	1	VL45	VGMA13 + (VGMA12 - VGMA13) × 5 / 8
2EH	1	0	1	1	1	0	VL46	VGMA13 + (VGMA12 - VGMA13) × 6 / 8
2FH	1	0	1	1	1	1	VL47	VGMA13 + (VGMA12 - VGMA13) × 7 / 8
30H	1	1	0	0	0	0	VL48	VGMA12
31H	1	1	0	0	0	1	VL49	VGMA12 + (VGMA11 - VGMA12) × 1 / 8
32H	1	1	0	0	1	0	VL50	VGMA12 + (VGMA11 - VGMA12) × 2 / 8
33H	1	1	0	0	1	1	VL51	VGMA12 + (VGMA11 - VGMA12) × 3 / 8
34H	1	1	0	1	0	0	VL52	VGMA12 + (VGMA11 - VGMA12) × 4 / 8
35H	1	1	0	1	0	1	VL53	VGMA12 + (VGMA11 - VGMA12) × 5 / 8
36H	1	1	0	1	1	0	VL54	VGMA12 + (VGMA11 - VGMA12) × 6 / 8
37H	1	1	0	1	1	1	VL55	VGMA12 + (VGMA11 - VGMA12) × 7 / 8
38H	1	1	1	0	0	0	VL56	VGMA11
39H	1	1	1	0	0	1	VL57	VGMA11 + (VGMA10 - VGMA11) × 1 / 8
3AH	1	1	1	0	1	0	VL58	VGMA11 + (VGMA10 - VGMA11) × 2 / 8
3BH	1	1	1	0	1	1	VL59	VGMA11 + (VGMA10 - VGMA11) × 3 / 8
3CH	1	1	1	1	0	0	VL60	VGMA11 + (VGMA10 - VGMA11) × 4 / 8
3DH	1	1	1	1	0	1	VL61	VGMA11 + (VGMA10 - VGMA11) × 5 / 8
3EH	1	1	1	1	1	0	VL62	VGMA11 + (VGMA10 - VGMA11) × 6 / 8
3FH	1	1	1	1	1	1	VL63	VGMA11 + (VGMA10 - VGMA11) × 7 / 8

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 6.5	V
Driver supply voltage	VDD2	-0.3 to 15.0	V
Input voltage	VGMA1 - 18	-0.3 to VDD2 + 0.3	V
	Others	-0.3 to VDD1 + 0.3	
Output voltage	DIO1, 2	-0.3 to VDD1 + 0.3	V
	Y1 - Y309	-0.3 to VDD2 + 0.3	
Operating power dissipation	Pd	150 (1)	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

NOTE: Relationship between TFT-LCD panel and Pd (Pd ∝ CL* (VDD2)^2 * fCLK1)

CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 - VGMA18 Turn off power order: VGMA1 - VGMA18 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = -20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.7	3.0	3.6	V
Driver supply voltage	VDD2 (1)	6.4	9.0	13.0	V
Gamma corrected voltage	VGMA1 - VGMA9	0.5VDD2	-	VDD2 - 0.2	V
	VGMA10 - VGMA18	VSS2 + 0.2	-	0.5VDD2	V
Driver part output voltage	Vyo	VSS2 + 0.2	-	VDD2 - 0.2	V
Maximum clock frequency	fmax	VDD1 = 2.7 V		55	MHz
Output load capacitance	CL(1)	-	-	150	pF / PIN

NOTE: Relationship between TFT-LCD panel and Pd (Pd ∝ CL* (VDD2)^2 * fCLK1)

DC CHARACTERISTICS

Table 5. DC Characteristics (Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 6.4 to 13.0 V, VSS1 = VSS2 = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 - D25, CLK1, SELT, POL, DIO1 (DIO2)	0.75VDD1	-	VDD1	V
Low level input voltage	VIL		0	-	0.25VDD1	
Input leakage current	IL		-1	-	1	µA
High level output voltage	VOH	DIO1 (DIO2), IO = -1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1 (DIO2), IO = +1.0 mA	-	-	0.5	
Resistor	R0 - R63	Refer to Table 1. Resistor Strings	Rn × 0.7	-	Rn × 1.3	Ω
Driver output current	IVOH	VDD2 = 9.0 V, Vx = 2.5 V, Vyo = 8.5 V(1)	-	-1.0	-0.5	mA
	IVOL	VDD2 = 9.0 V, Vx = 6.5 V, Vyo = 0.5 V(1)	0.5	1.0	-	mA
Output voltage deviation	ΔVO	Input data: 00H to 3FH	-	±8	±15	mV
Output voltage range	Vyo	Input data: 00H to 3FH	VSS2 + 0.2	-	VDD2 - 0.2	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V (2)	-	2.0	3.5	mA
Driver part dynamic current	IDD2	VDD1 = 3.0 V, VDD2 = 9.0 V (2)(3)(4)	-	5.0	7.0	

NOTES:

1. Vyo is the output voltage of analog output pins Y1 to Y309. Vx is the voltage applied to analog output pins Y1 to Y309.
2. CLK1 period is defined to be 20 µs at fCLK2 = 33 MHz, data pattern = 101010(checkerboard pattern), Ta = 25 °C.
3. The current consumption per driver when XGA single-sided mounting (10 drivers) is connected in cascade
4. Yout Load Condition

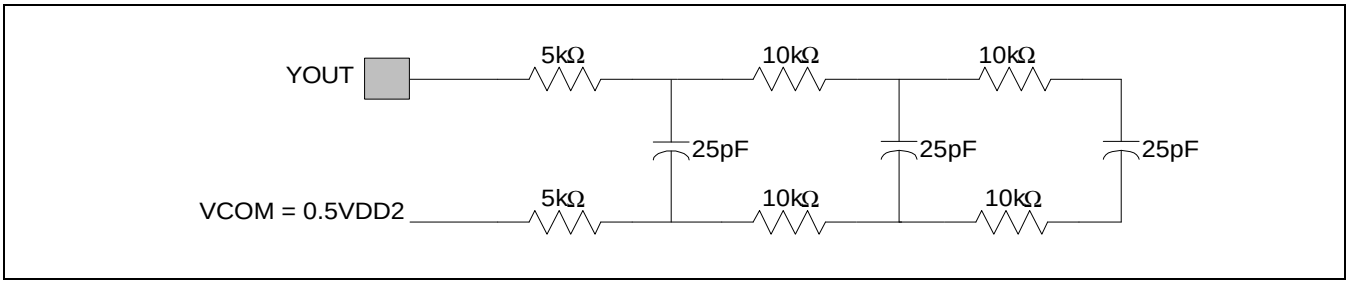

Figure 5. Yout Load Condition

AC CHARACTERISTICS

Table 6. AC Characteristics
(Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 6.4 to 13.0 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	-	18	-	-	ns
Clock pulse low period	PWCLK (L)	-	4	-	-	
Clock pulse high period	PWCLK (H)	-	4	-	-	
Data setup time	tSETUP1	-	4	-	-	
Data hold time	tHOLD1	-	0	-	-	
Start pulse setup time	tSETUP2	-	4	-	-	
Start pulse hold time	tHOLD2	-	0	-	-	
Start pulse delay time	tPLH1	CL = 20pF	-	-	12	
CLK1 – DIO (input) setup time	tSETUP3	-	1	-	-	CLK2 period
CLK1 pulse high period	PWCLK1	-	3	-	-	
Driver output delay time1	tPHL1(1)	Refer to Figure 5	-	-	5	µs
Driver output delay time2	tPHL2(2)	Refer to Figure 5	-	-	10	
Data invalid period	tINV	DIO1 (2)↑ → CLK2↑	1			CLK2 period
Last data timing	tLDT	-	1	-	-	
CLK1 - CLK2 time	tCLK1 - CLK2	CLK1↑ → CLK2↑	6	-	-	ns
POL - CLK1 time	tPOL - CLK1	POL↑or↓ → CLK1↑	-9	-	-	ns

NOTES:
1. The value is specified when the drive voltage value reaches the target output voltage level of 90%
2. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.

WAVEFORMS (VIH = 0.75VDD1, VIL = 0.25VDD1)

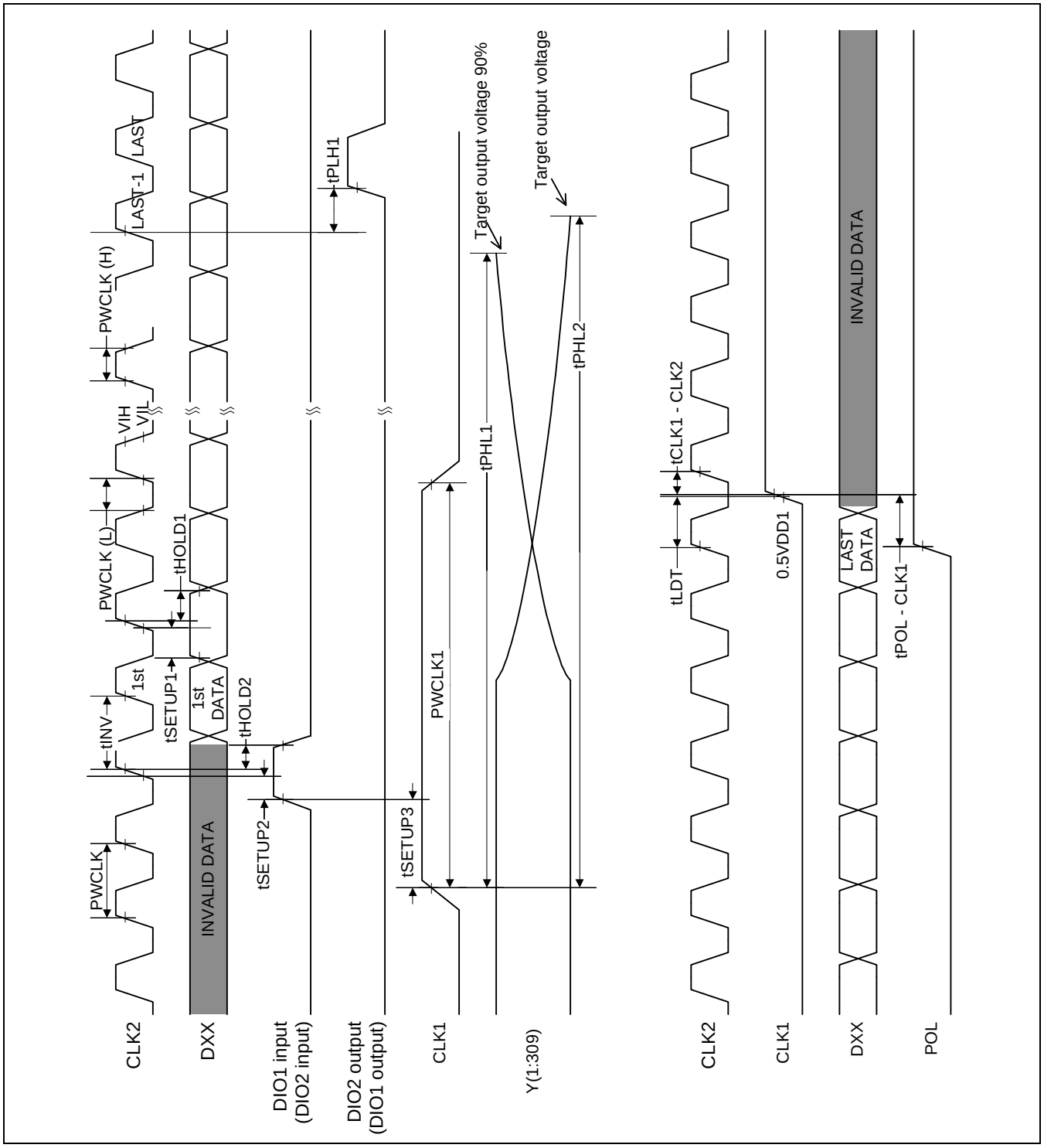

Figure 6. Waveforms

RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

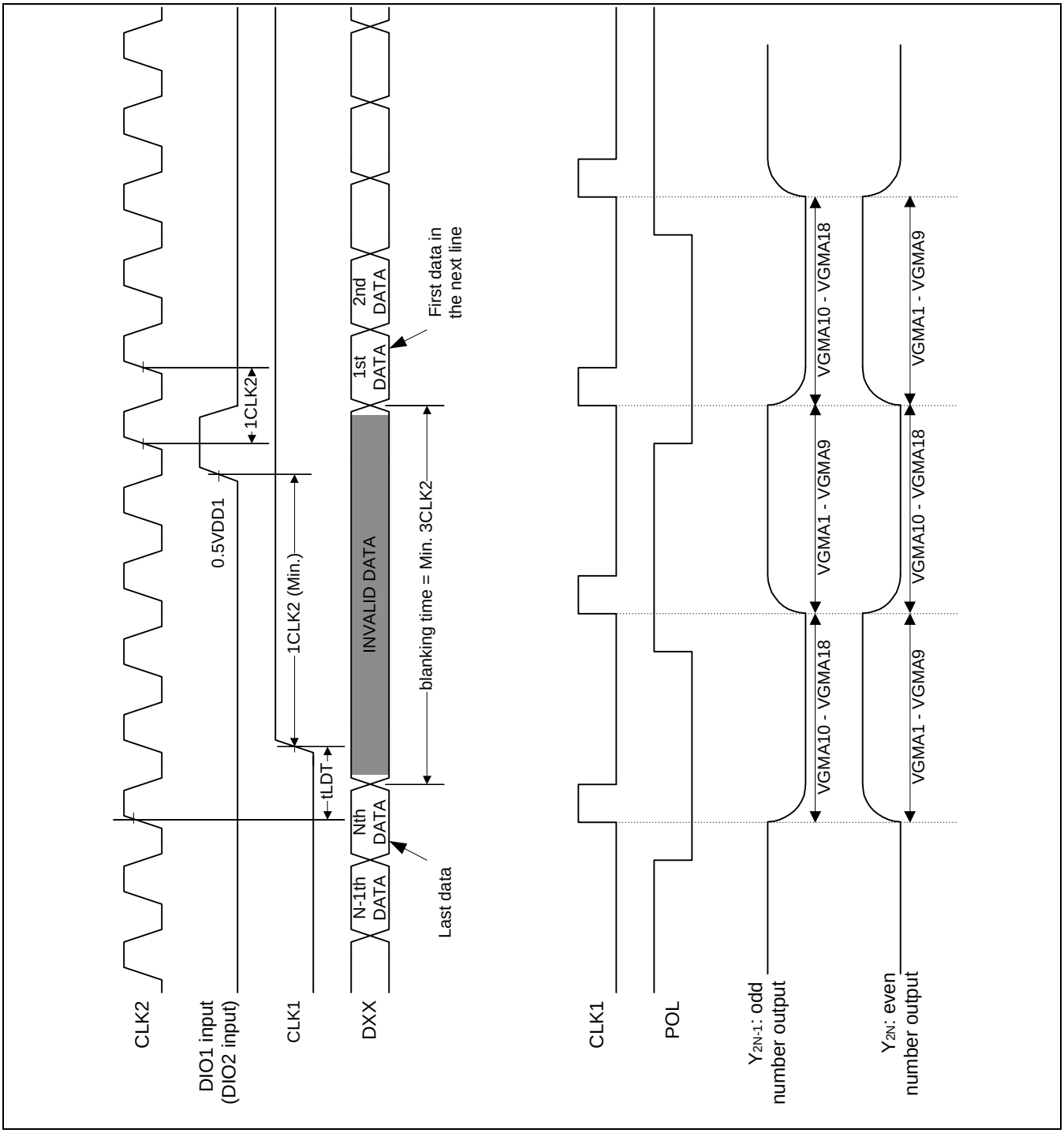

Figure 7. Waveforms