HARRIS Semiconductor

RFM18N08, RFM18N10, RFP18N08, RFP18N10

18A, 80V and 100V, 0.100 Ohm, N-Channel Power MOSFETs

September 1998

Features

- **18A, 80V and 100V**
- **$r_{DS(ON)}$ = 0.100Ω**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFM18N08	TO-204AA	RFM18N08
RFM18N10	TO-204AA	RFM18N10
RFP18N08	TO-220AB	RFP18N08
RFP18N10	TO-220AB	RFP18N10

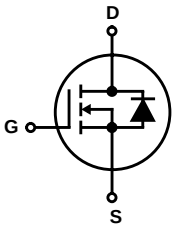
NOTE: When ordering, use the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

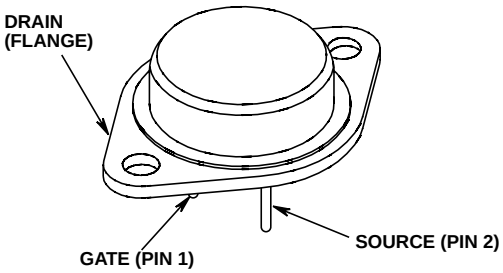
Formerly developmental type TA17421.

Symbol

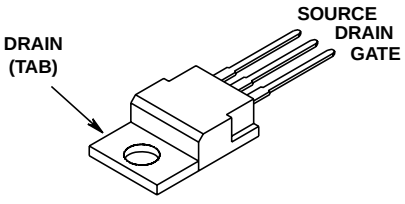


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1446.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	RFM18N08	RFM18N10	RFP18N08	RFP18N10	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DSS}	80	100	80	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	80	100	80	100	V
Continuous Drain Current . . . . . I_D	18	18	18	18	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	45	45	45	45	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D	100	100	75	75	W
Linear Derating Factor	0.8	0.8	0.6	0.6	W/^{o}C
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^{o}C
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V				
RFM18N08, RFP18N08			80	-	-	V
RFM18N10, RFP18N10			100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA, (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 18A, V_{GS} = 10V, (Figures 6, 7)	-	-	0.100	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 18A, V_{GS} = 10V	-	-	1.8	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \approx$ 9A, R_G = 50Ω, V_{GS} = 10V, R_L = 5.5Ω (Figures 10, 11, 12)	-	60	90	ns
Rise Time	t_r		-	300	450	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	150	225	ns
Fall Time	t_f		-	150	225	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz, (Figure 9)	-	-	1700	pF
Output Capacitance	C_{OSS}		-	-	750	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	300	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFM18N08, RFM18N10	-	-	1.25	^{o}C/W
		RFP18N08, RFP18N10	-	-	1.67	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 9A	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/μs	-	150	-	ns

NOTES:

2. Pulse test: width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

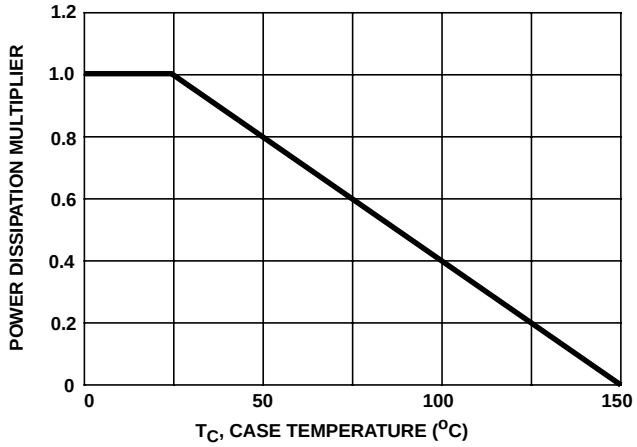


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

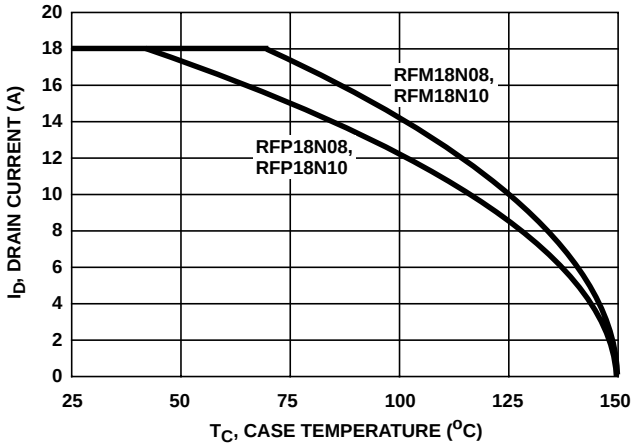


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

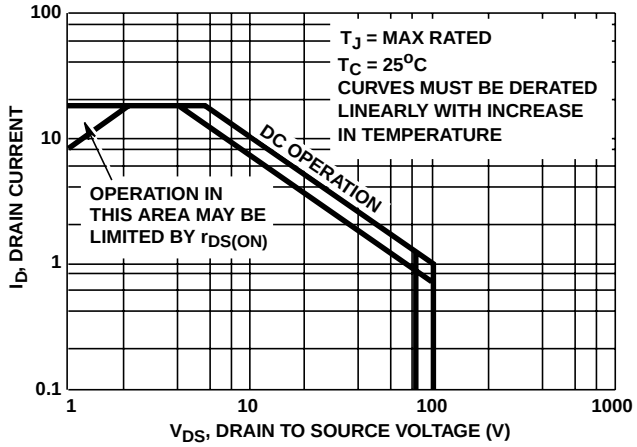


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

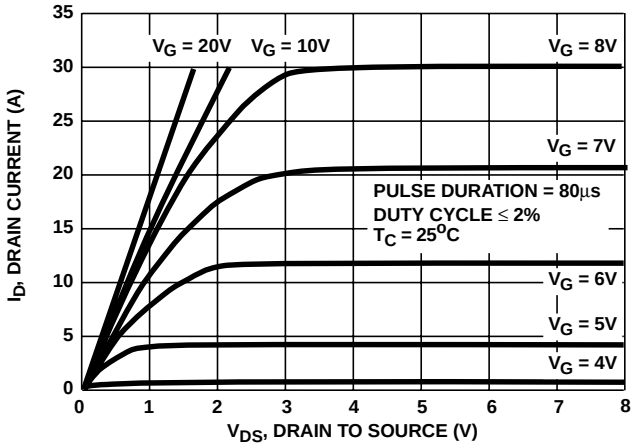


FIGURE 4. SATURATION CHARACTERISTICS

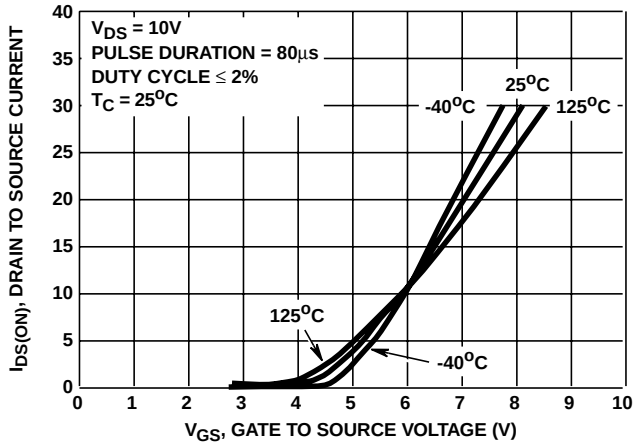


FIGURE 5. TRANSFER CHARACTERISTICS

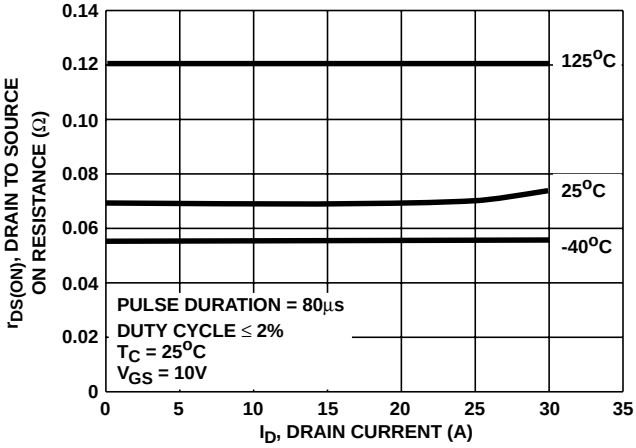


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

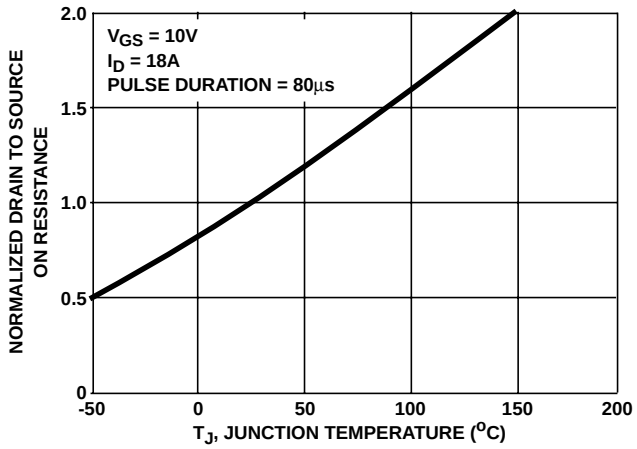


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

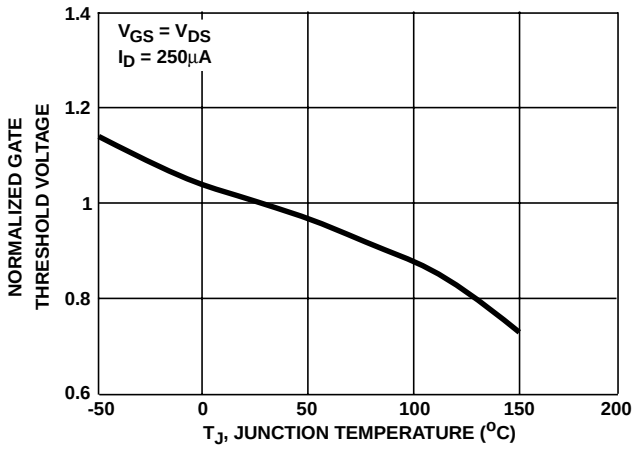


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

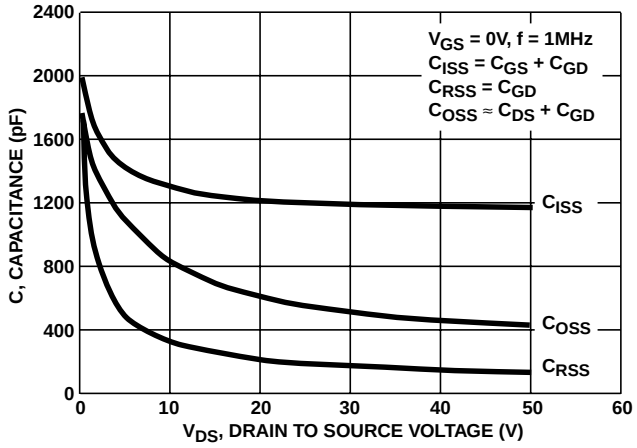
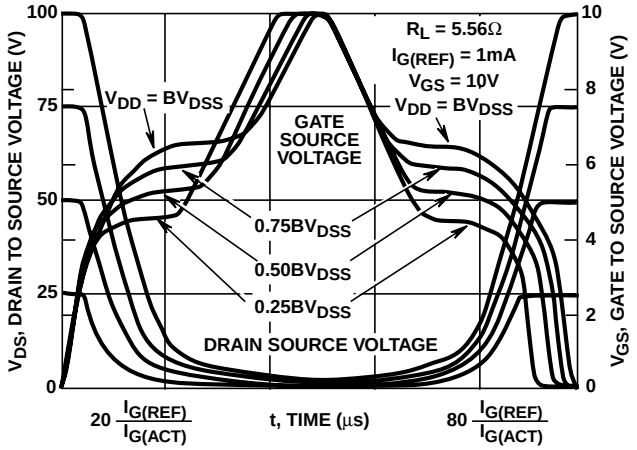


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

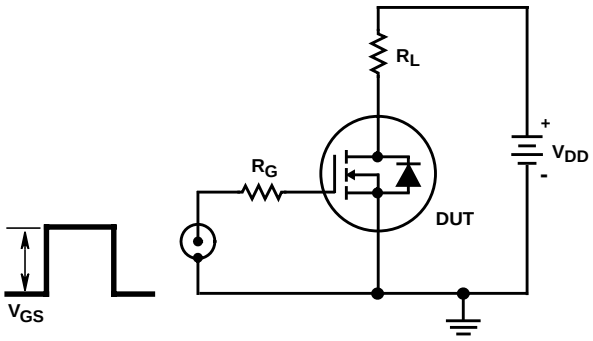


FIGURE 11. SWITCHING TIME TEST CIRCUIT

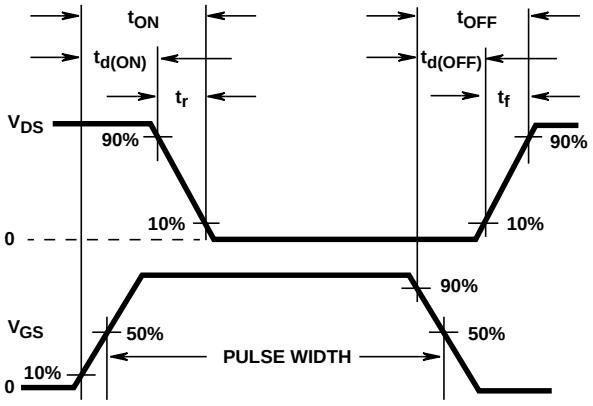


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

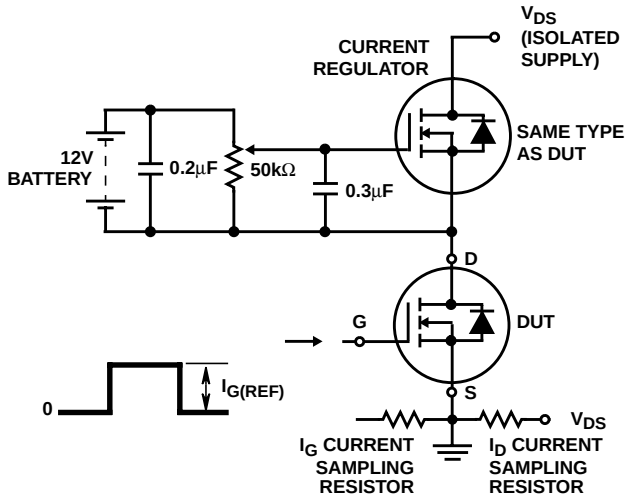


FIGURE 13. GATE CHARGE TEST CIRCUIT

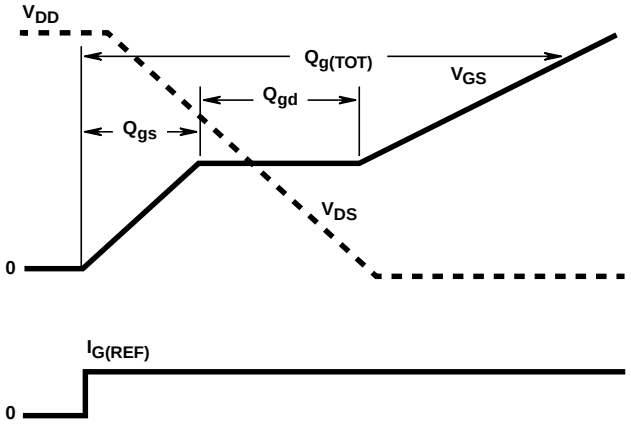


FIGURE 14. GATE CHARGE WAVEFORMS