PLL602-30

750kHz – 800MHz Low Phase Noise XO (for 12 – 25MHz Crystals)

FEATURES

- 750kHz to 800MHz output range.
- Low phase noise output (@ 10kHz frequency offset, -142dBc/Hz for 19.44MHz, -123dBc/Hz for 106.25MHz, -125dBc/Hz for 155.52MHz, -115dBc/Hz for 622.08MHz).
- Selectable CMOS, PECL and LVDS output.
- Selectable High Drive (30mA) or Standard Drive (10mA) output.
- 12MHz to 25MHz crystal input.
- Output Enable selector.
- 3.3V operation.
- Available in DIE (65 mil x 62 mil).

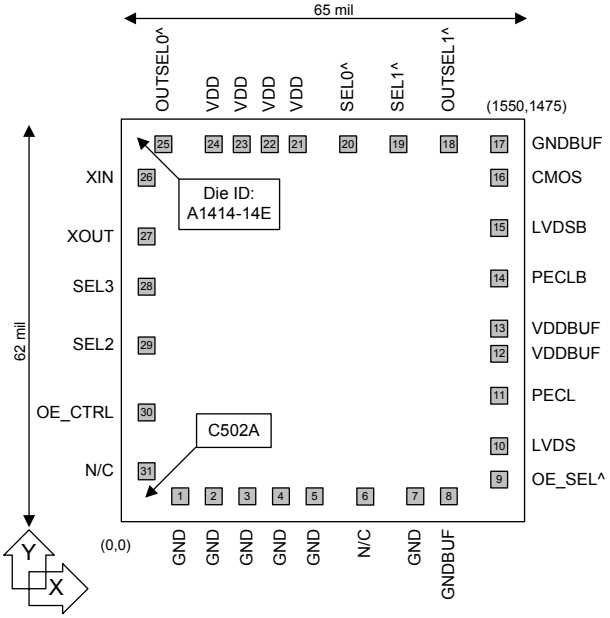
DESCRIPTION

The PLL602-30 is a monolithic low jitter and low phase noise (-142dBc/Hz @ 10kHz offset) XO IC Die, with selectable CMOS, LVDS or PECL output, covering the 750kHz to 800MHz output range, using a low frequency crystal.
This makes the PLL602-30 ideal as a universal die for applications ranging from low frequency to SONET.

DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

DIE CONFIGURATION



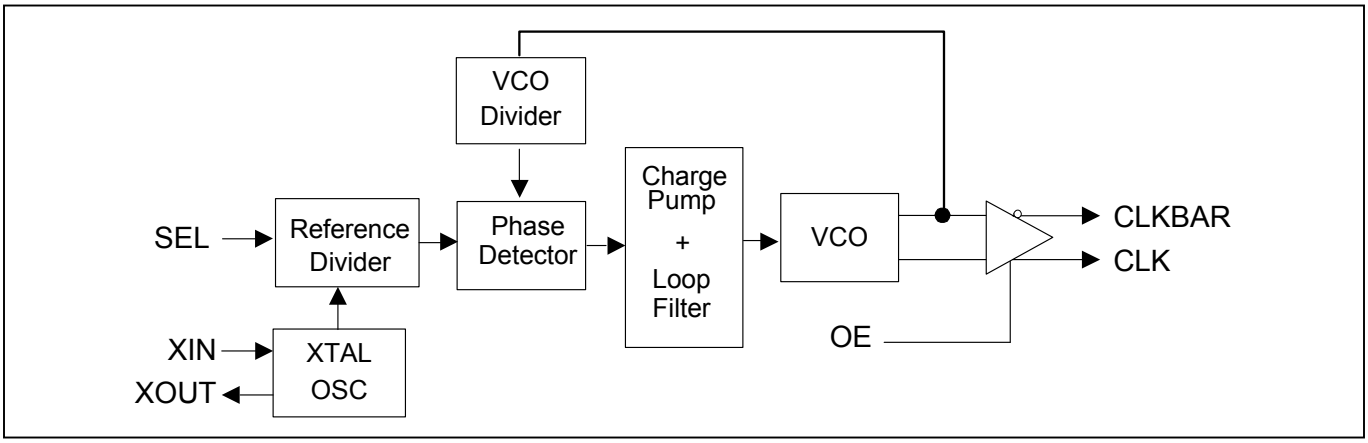
OUTPUT SELECTION AND ENABLE

OUTSEL1 (Pad #18)	OUTSEL0 (Pad #25)	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	PECL
1	1	LVDS

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0 (Default)	Output enabled
	1	Tri-state
1 (Default)	0	Tri-state
	1 (Default)	Output enabled

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"
Pad #30: Logical states defined by PECL levels if OE_SELECT (pad #9) is "0"
Logical states defined by CMOS levels if OE_SELECT is "1"

BLOCK DIAGRAM



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FREQUENCY SELECTION TABLE

SEL3 (Pad #28)	SEL2 (Pad #29)	SEL1 (Pad #19)	SEL0 (Pad #20)	Selected Multiplier
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Fin x 32
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Fin / 8
0	1	1	1	Fin x 2
1	0	0	0	Reserved
1	0	0	1	Fin / 2
1	0	1	0	Fin / 16
1	0	1	1	Fin x 4
1	1	0	0	Fin / 4
1	1	0	1	Fin x 8
1	1	1	0	Fin x 16
1	1	1	1	No multiplication

All pads have internal pull-ups (default value is 1). Bond to GND to set to 0.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			20		pF
Recommended ESR	R_E	AT cut			30	Ω

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3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	PECL/LVDS/CMOS	Fout<24MHz			25/25/15	mA
			24MHz<Fout<96MHz			65/45/30	
			96MHz<Fout<700MHz			100/80/40	
Operating Voltage	V_{DD}			2.97		3.63	V
Output Clock Duty Cycle		@ 50% V_{DD} (CMOS) @ 1.25V (LVDS) @ V_{DD} – 1.3V (PECL)		45 45 45	50 50 50	55 55 55	%
Short Circuit Current					±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS[1]	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	19.44MHz		2.1		ps
		77.76MHz		3.5		
		106.25MHz		4.1		
		155.52MHz		4.3		
		622.08MHz		6.0		
Period jitter Peak-to-Peak[1]	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	19.44MHz		17		ps
		77.76MHz		30		
		106.25MHz		28		
		155.52MHz		27		
		622.08MHz		40		
Integrated jitter RMS[2]	Integrated 12 kHz to 20 MHz	155.52MHz		2.6	4	ps
		622.08MHz		2.5	4	

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise[2] relative to carrier (typical)	19.44MHz	-80	-108	-132	-142	-142	dBc/Hz
	106.25MHz	-70	-98	-122	-123	-117	
	155.52MHz	-60	-90	-115	-125	-119	
	622.08MHz	-50	-77	-102	-115	-108	

1) Jitter analyzer: Wavecrest SIA-3000
2) Phase Noise System: Agilent E5500

6. CMOS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

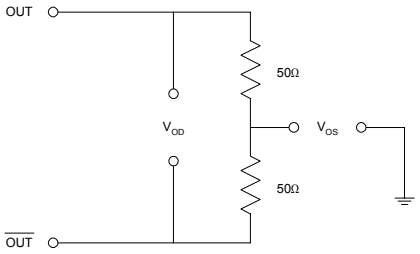
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

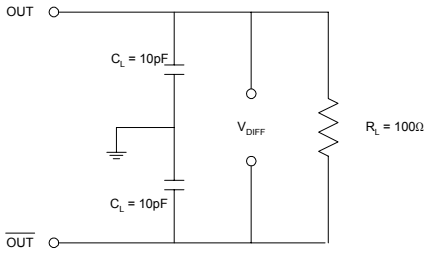
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

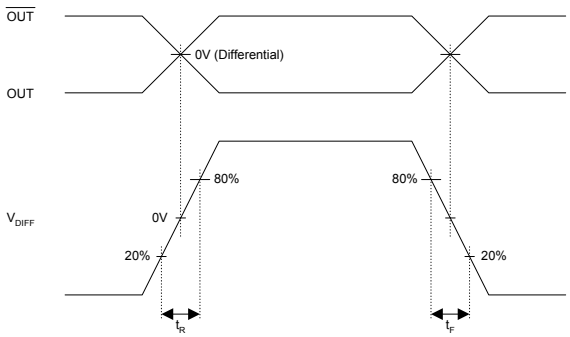
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



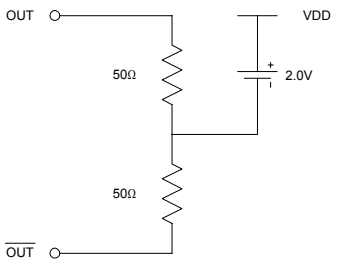
9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

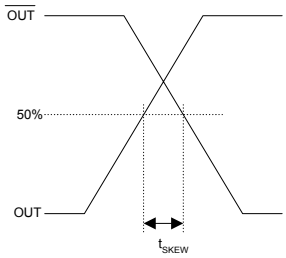
10. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

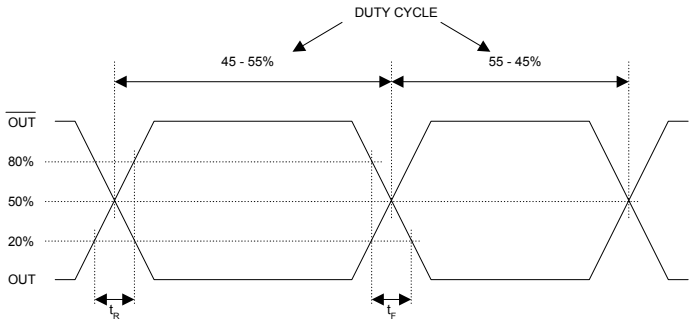
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



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PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)	Description
1	GND	248	109	Ground.
2	GND	361	109	Ground.
3	GND	473	109	Ground.
4	GND	587	109	Ground.
5	GND	702	109	Ground.
6	N/C	874	109	No Connection.
7	GND	1042	109	Ground.
8	GNDBUF	1171	109	Ground, buffer circuitry.
9	OE_SELECT	1400	125	Used to select between PECL or CMOS logic states for OE. Internal pull up.
10	LVDS	1400	259	LVDS Output.
11	PECL	1400	476	PECL Output.
12	VDDBUF	1400	616	3.3V power supply, Buffer circuitry.
13	VDDBUF	1400	716	3.3V power supply, Buffer circuitry.
14	PECLB	1400	871	Complementary PECL Output.
15	LVDSB	1400	1089	Complementary LVDS Output.
16	CMOS	1400	1227	CMOS Output.
17	GNDBUF	1389	1365	Ground, buffer circuitry.
18	OUTSEL1	1232	1365	Used to select CMOS, PECL or LVDS output type. Internal pull up.
19	SEL1	1042	1365	Used to select multiplication factor. Internal pull up.
20	SEL0	854	1365	Used to select multiplication factor. Internal pull up.
21	VDD	659	1365	3.3V power supply.
22	VDD	559	1365	3.3V power supply.
23	VDD	459	1365	3.3V power supply.
24	VDD	358	1365	3.3V power supply.
25	OUTSEL0	194	1365	Used to select CMOS, PECL or LVDS output type. Internal pull up.
26	XIN	109	1223	Crystal input. See crystal specification page 3.
27	XOUT	109	1017	Crystal output. See crystal specification page 3.
28	SEL3	109	858	Used to select multiplication factor. Internal pull up.
29	SEL2	109	646	Used to select multiplication factor. Internal pull up.
30	OE_CTRL	109	397	Used to enable/disable the output(s). See Output Selection and Enable table on page 1.
31	NC	109	181	No Connect

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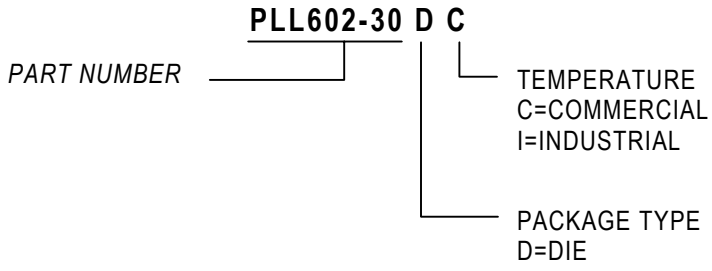
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL602-30DC	PLL602-30DC	Die – Waffle Pack