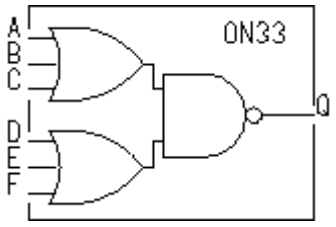
ON33 is an OR / NAND circuit providing the logical function Q = NOT [(A+B+C).(D+E+F)].

Truth Table

A	B	C	D	E	F	Q
0	0	0	X	X	X	1
X	X	X	0	0	0	1
X	X	1	X	X	1	0
X	X	1	X	1	X	0
X	X	1	1	X	X	0
X	1	X	X	X	1	0
X	1	X	X	1	X	0
X	1	X	1	X	X	0
1	X	X	X	X	1	0
1	X	X	X	1	X	0
1	X	X	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.018
B	0.018
C	0.018
D	0.017
E	0.016
F	0.015

Area

0.226 mils^2
146 µm^2

Power

1.234 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.1**		**2**		**0.1**		**2**	
Load [pF]	**0.015**	**0.15**	**0.015**	**0.15**	**0.015**	**0.15**	**0.015**	**0.15**
Delay A => Q	0.29	0.75	0.33	0.76	0.38	0.79	0.6	1.01
Delay B => Q	0.27	0.72	0.39	0.84	0.34	0.74	0.55	0.97
Delay C => Q	0.21	0.66	0.43	0.89	0.28	0.69	0.47	0.91
Delay D => Q	0.23	0.69	0.23	0.7	0.36	0.77	0.71	1.14
Delay E => Q	0.21	0.67	0.3	0.77	0.32	0.72	0.65	1.1
Delay F => Q	0.14	0.61	0.34	0.82	0.26	0.66	0.56	1.04
Slew A => Q	1.09	2.55	1.46	2.72	0.64	1.56	1.01	1.78
Slew B => Q	1.09	2.54	1.51	2.75	0.54	1.46	0.89	1.68
Slew C => Q	1.08	2.54	1.53	2.79	0.46	1.37	0.79	1.58
Slew D => Q	0.99	2.44	1.35	2.61	0.65	1.56	1.1	1.87
Slew E => Q	0.99	2.44	1.41	2.65	0.55	1.47	0.98	1.77
Slew F => Q	0.97	2.45	1.43	2.68	0.45	1.36	0.84	1.67