FET INPUT DIFFERENTIAL OPERATIONAL AMPLIFIER

801

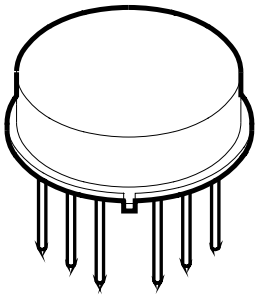
M.S.KENNEDY CORP.

4707 Dey Road Liverpool, N.Y. 13088 (315) 701-6751

MIL-PRF-38534 QUALIFIED

FEATURES:

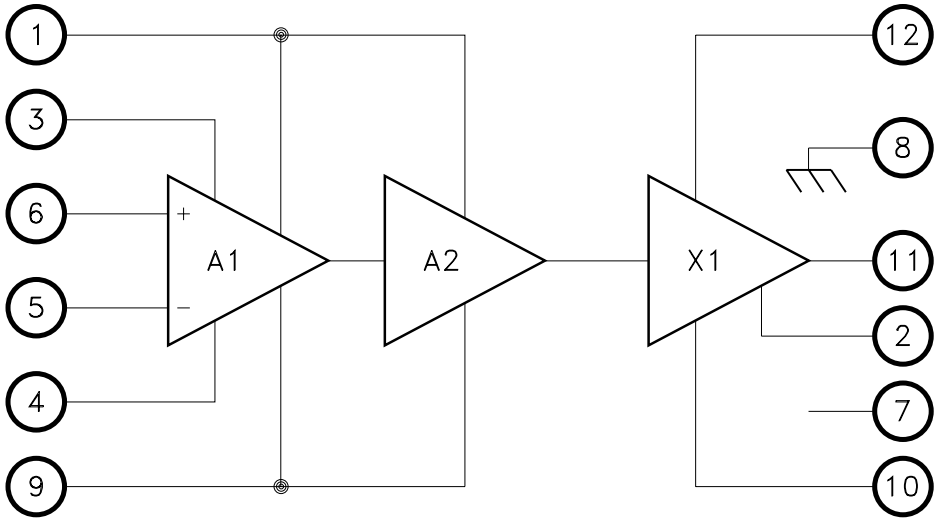
- 10 MHz full power bandwidth min.
- 650 Volts/μs slew rate min.
- 75 ns settling time to 0.1% max.
- ±100 mA output current min.
- Replaces H0S-50
- Fet Input
- Available to DSCC SMD 5962-91574



DESCRIPTION:

The MSK 801 is a high speed, FET input, differential amplifier that exhibits very good DC characteristics. The FET input of the MSK 801 produces low input bias current, input offset voltage and input offset drift specifications. Wide bandwidth, high input impedance, and high output current make it an ideal choice for many high speed/high frequency applications. In addition, the MSK 801 offers the user external compensation, offset null and short circuit protection.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- D/A Converters
- Buffer Amplifiers
- High Speed Integrators
- Sample and Hold Circuits
- Video Drivers

PIN-OUT INFORMATION

1	+Vcc	12	+VC
2	Output Comp.	11	Output
3	Comp./Bal.	10	-VC
4	Comp./Bal.	9	-Vcc
5	Inverting Input	8	Case
6	Non-Inverting Input	7	NC

ABSOLUTE MAXIMUM RATINGS ⑧

$\pm V_{CC}$ Supply Voltage . . . . . $\pm 18V$
V_{IN} Input Voltage . . . . . $\pm V_{CC}$
Differential Input Voltage . . . . . $\pm 30V$
T_C Case Operating Temperature Range
(MSK 801) . . . . . -40°C to +125°C
(MSK801B/E) . . . . . -55°C to +125°C

T_{ST} Storage Temperature Range . . -65°C to +150°C
T_{LD} Lead Temperature Range . . . . . 300°C
(10 Seconds Soldering)
P_D Power Dissipation . . . . . See Curve
I_{OUT} Peak Output Current . . . . . $\pm 200mA$

ELECTRICAL SPECIFICATIONS

$\pm Vcc = \pm 15V$ Unless Otherwise Specified

Parameter	Test Conditions	Group A Subgroup	MSK 801B/E Min.	MSK 801B/E Typ.	MSK 801B/E Max.	MSK 801 Min.	MSK 801 Typ.	MSK 801 Max.	Units
Quiescent Current	$V_{IN} = 0V$	1	-	±25	±30	-	±25	±35	mA
		2,3	-	±27	±32	-	-	-	mA
Input Offset Voltage	$V_{IN} = 0V$	1	-	±0.5	±5	-	±0.5	±10	mV
Input Offset Voltage Drift	$V_{IN} = 0V$	2,3	-	±10	±50	-	±10	-	µV/°C
Input Bias Current		1	-	±50	±500	-	±50	±750	pA
		2,3	-	±0.2	±10	-	-	-	nA
Input Offset Current		1	-	10	500	-	10	750	pA
		2,3	-	0.1	5	-	-	-	nA
Output Current	$R_L = 100\Omega$ $V_{OUT} = \pm 10V$	4	±100	±120	-	±100	±120	-	mA
Output Voltage Swing	$R_L = 100\Omega$ f ≤ 10MHz	4	±10	±11.5	-	±10	±11.5	-	V
Full Power Bandwidth	$R_L = 100\Omega$ $V_O = \pm 10V$	4	10	12	-	8	12	-	MHz
Bandwidth (Small Signal) ②	$R_L = 510\Omega$	4	100	125	-	90	125	-	MHz
Slew Rate Limit (Pulsed)	$R_L = 100\Omega$ $V_O = \pm 10V$	4	650	750	-	550	750	-	V/µS
Large Signal Voltage Gain	$R_L = 1K\Omega$ $V_O \pm 10V$	4	50	70	-	50	70	-	dB
Settling Time to 1% ①	$R_L = 100\Omega$ $V_{IN} = 10V$	4	-	40	55	-	40	65	nS
Settling Time to 0.1% ①②	$R_L = 100\Omega$ $V_{IN} = 10V$	4	-	60	75	-	60	85	nS
Settling Time to 0.01% ①②	$R_L = 100\Omega$ $V_{IN} = 10V$	-	-	200	-	-	200	-	nS
Power Supply Rejection Ratio ②	$\Delta V_{CC} = \pm 5V$	-	60	70	-	55	70	-	dB
Common Mode Rejection Ratio ②	$\Delta V_{IN} = \pm 10V$	-	70	80	-	65	80	-	dB
Input Noise Voltage ②	f = 10Hz to 1KHz	-	-	1.5	-	-	1.5	-	µVRMS
Equivalent Input Noise ②	f = 1KHz	-	-	40	-	-	40	-	$nV/\sqrt{Hz}$
Gain Bandwidth Product ②	$R_L = 510\Omega$ AV = -20	-	200	250	-	200	250	-	MHz
Slew Rate (Sine Wave) ②	$R_L = 100\Omega$ $V_O = \pm 10V$	-	-	700	-	-	700	-	V/µS
Thermal Resistance ②	Junction to Case @ 125°C	-	-	65	75	-	65	80	°C/W

NOTES:

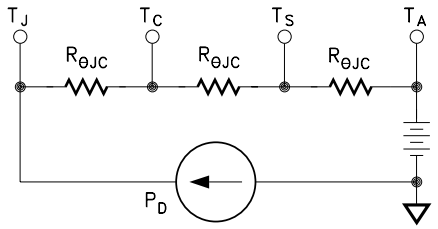
① AV = -1, measured in false summing junction circuit.
② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
③ Industrial grade and "E" suffix devices shall be tested to subgroups 1 and 4 unless otherwise specified.
④ Military grade devices ("B" suffix) shall be 100% tested to subgroups 1,2,3 and 4.
⑤ Subgroups 5 and 6 testing available upon request.
⑥ Subgroup 1,4 $T_A = T_C = +25°C$
Subgroup 2 $T_A = T_C = +125°C$
Subgroup 3 $T_A = T_C = -55°C$
⑦ Consult DSCC SMD 5962-91574 for electrical specifications for devices purchased as such.
⑧ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.

APPLICATION NOTES

Heat Sinking

To determine if a heat sink is necessary for your application and if so, what type, refer to the thermal model and governing equation below.

Thermal Model:



Governing Equation:

$T_J = P_D \times (R_{\theta JC} + R_{\theta CS} + R_{\theta JC}) + T_A$

Where

T_J = Junction Temperature
P_D = Total Power Dissipation
$R_{\theta JC}$ = Junction to Case Thermal Resistance
$R_{\theta CS}$ = Case to Heat Sink Thermal Resistance
$R_{\theta SA}$ = Heat Sink to Ambient Thermal Resistance
T_C = Case Temperature
T_A = Ambient Temperature
T_S = Sink Temperature

Example:

This example demonstrates a worst case analysis for the op-amp output stage. This occurs when the output voltage is 1/2 the power supply voltage. Under this condition, maximum power transfer occurs and the output is under maximum stress.

Conditions:
$V_{CC} = \pm 16$VDC
$V_O = \pm 8$Vp Sine Wave, Freq. = 1KHz
$R_L = 100\Omega$

For a worst case analysis we will treat the +8Vp sine wave as an 8VDC output voltage.

1.) Find Driver Power Dissapation
$P_D = (V_{CC}-V_O)(V_O/R_L)$
$= (16V-8V)(8V/100\Omega)$
$= 0.64W$
2.) For conservative design, set $T_J = +125°C$
3.) For this example, worst case $T_A = +50°C$
4.) $R_{\theta JC} = 65°C/W$ from MSK 801 Data Sheet
5.) $R_{\theta CS} = 0.15°C/W$ for most thermal greases
6.) Rearrange governing equation to solve for $R_{\theta SA}$

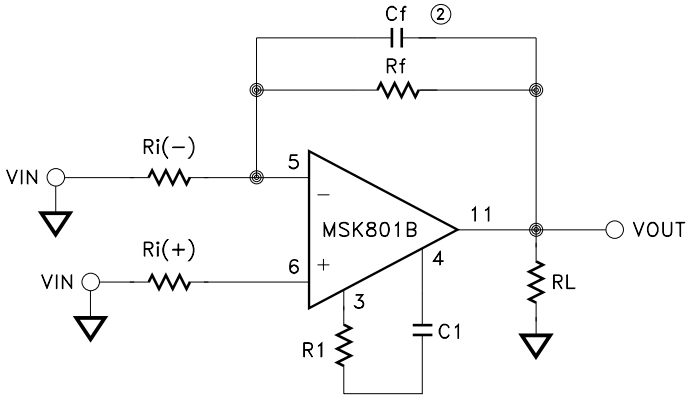
$R_{\theta SA} = ((T_J-T_A)/P_D) - (R_{\theta JC}) - (R_{\theta CS})$
$= ((125°C - 50°C)/0.64W) - 65°C/W - 0.15°C/W$
$= 117.2 - 65.15$
$= 52.0°C/W$

Stability and Layout Considerations

As with all wideband devices, proper decoupling of the power lines is extremely important. The power supplies should be bypassed as near to pins 10 and 12 as possible with a parallel grouping of a 0.01μf ceramic disc and a 4.7μf tantalum capacitor. Wideband devices are also sensitive to printed circuit board layout. Be sure to keep all runs as short as possible, especially those associated with the summing junction, power lines and compensation pins.

Recommended External Component Selection Guide Using External Rf

	APPROXIMATE DESIRED GAIN	RI(+)	RI(-)	Rf	R1	C1
①	-1	500Ω	1KΩ	1KΩ	43Ω	0.01μf
	+1	1KΩ	0Ω	0Ω	43Ω	0.01μf
①	-5	820Ω	1KΩ	4.99KΩ	120Ω	0.01μf
	+5	0Ω	910Ω	3.6KΩ	120Ω	0.01μf
①	-10	910Ω	1KΩ	10KΩ	150Ω	0.01μf
	+10	0Ω	1KΩ	9.1KΩ	150Ω	0.01μf



① The positive input resistor is selected to minimize offset currents. The positve input can be grounded without a resistor if desired.

② This feedback capacitor will help compensate for stray input capacitance. The value of this capacitor can be dependent on individual applications. A 2 to 9 pf capacitor is usually optimum for most applications.

Load Considerations

When determining the load an amplifier will see, the capacative portion must be taken into consideration. For an amplifier that slews at 1000V/μS, each pf will require 1 mA of output current. To minimize ringing with highly capacitive loads, reduce the load time constant by adding shunt resistance.

Case Connection

The MSK 801 has pin 8 internally connected to the case. The case is not electrically connected to the internal circuit. Pin 8 should be tied to a ground plane for shielding. For special applications, consult factory.

Slew Rate vs. Slew Rate Limit

SLEW RATE:

$S = 2\pi fVp$; Slew rate is based upon the sinusoidal linear response of the amplifier and is calculated from the full power bandwidth frequency.

SLEW RATE LIMIT

dv/dt; The slew rate limit is based upon the amplifier's response to a step input and is measured between 10% and 90%. MSK measures Tr or Tf, whichever is greater at $\pm 10V_{OUT}$, $R_L = 100\Omega$.

Definition of Settling Time

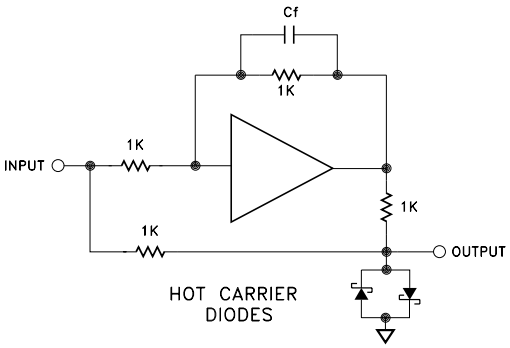
The time required for the output to come within a predetermined error band after application of a full scale step input. This includes the time of delay, slew time and the small signal settling of the amplifier.

Measuring Settling Time

The only accurate method of measuring settling time is by the creation of a false summing junction and observing the error band at that point.

The reasons for not using other methods are as follows: Observation of settling at the actual summing junction adds probe capacitance to the input and changes the entire response of the system. (Probe capacitance almost doubles the capacitance at the summing point.) Observing the output is extremely difficult, as the 3% linearity of oscilloscopes, and reading inaccuracies, lead to a possible 5% error. The false summing junction approach works well bcause the amplifier is subtracting the output from the input, and only 1/2 the actual error appears there.

False Summing Junction Circuit

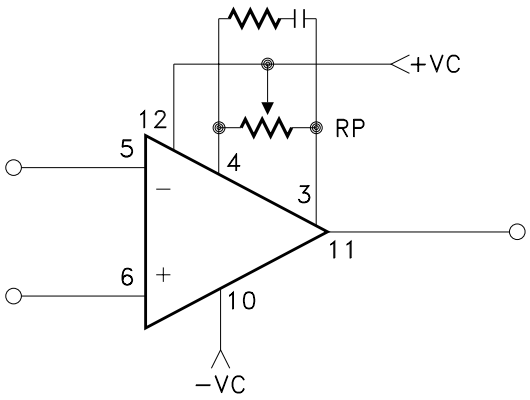


Problems: Because the amplifier is to be overdriven, 1/2 the input voltage can be expected to appear at the false summing junction. Therefore, it is necessary to clamp that point with diodes to limit the voltage excursion to avoid overdriving the oscilloscope with the consequent recovery time of the scope itself. The scope probe has capacitance which significantly affects the settling time measurement. Keep the associated resistors as low as possible to minimize the RC time constants, and take into account the added time created by the false summing junction. On the ranges used for settling time measurement even the best real-time scopes suffer from reduced bandwidth and relatively slow settling; a sampling scope is convenient for these measurements.

Offset Null

Typically the MSK 801 has an input offset voltage of less than ± 1 mV. If it is desirable to "null" the offset voltage, the circuit below is recommended.

$R_P = 10K\Omega$

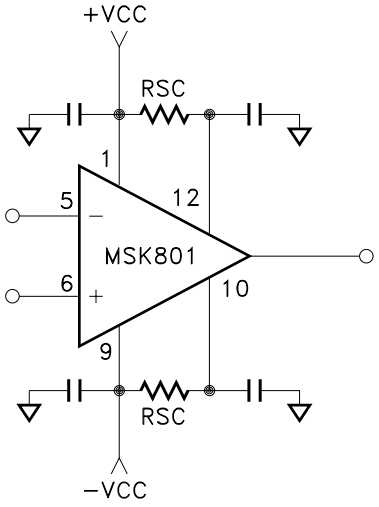


Output Short Circuit Protection

The collectors of the output devices have been brought out to pins 10 and 12 for short circuit protection, if desired. A resistor can be inserted between $+V_C$ and $+V_{CC}$ pins, and $-V_C$ and $-V_{CC}$ respectively. Resistor values can be selected as follows:

$$R_{SC} \cong \frac{(+)V_{CC}}{(+)I_{SC}} = \frac{(-)V_{CC}}{(-)I_{SC}}$$

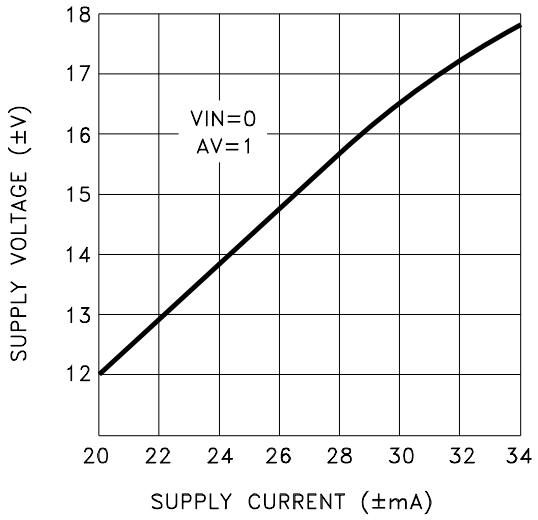
The addition of the these resistors reduces output voltage swing. Decoupling at $\pm V_C$ can help to retain full swing for transient pulses.



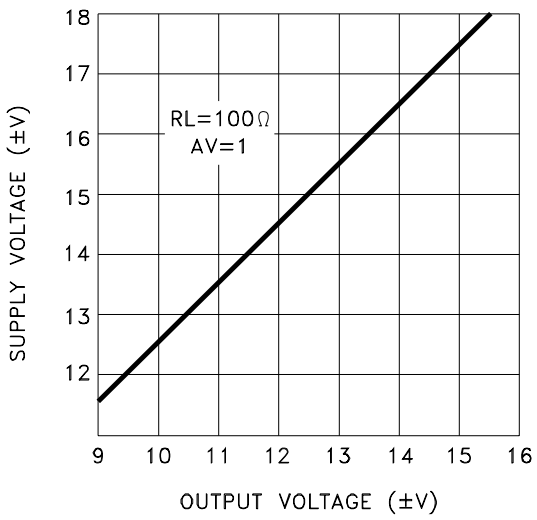
For normal operation and best overall response, short $+V_{CC}$ and $+V_C$ and short $-V_{CC}$ and $-V_C$ together.

TYPICAL PERFORMANCE CURVES

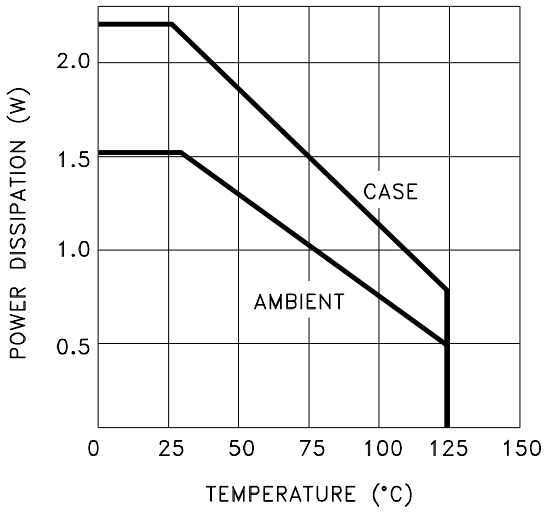
SUPPLY VOLTAGE vs. SUPPLY CURRENT



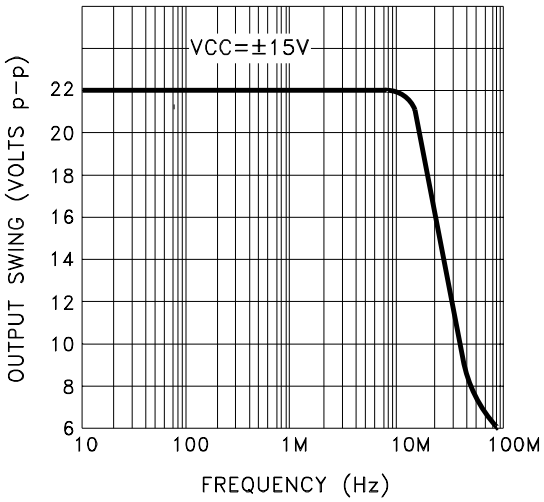
OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



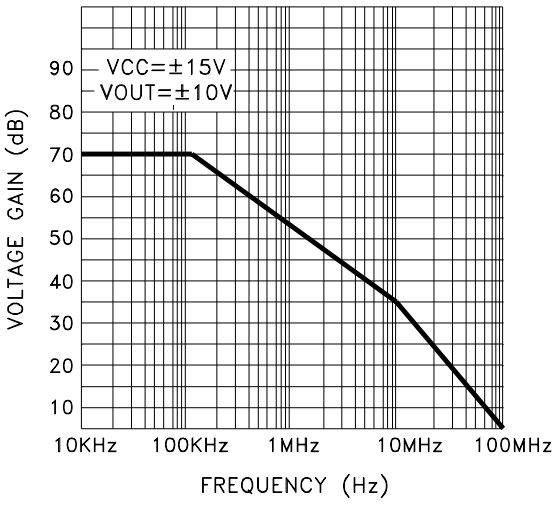
MAXIMUM POWER DISSIPATION



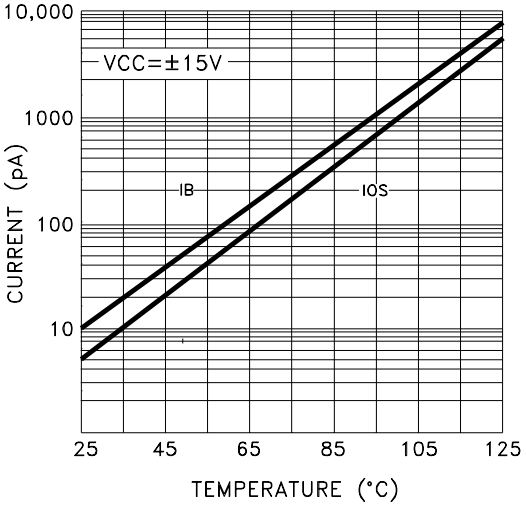
OUTPUT VOLTAGE SWING vs. FREQUENCY



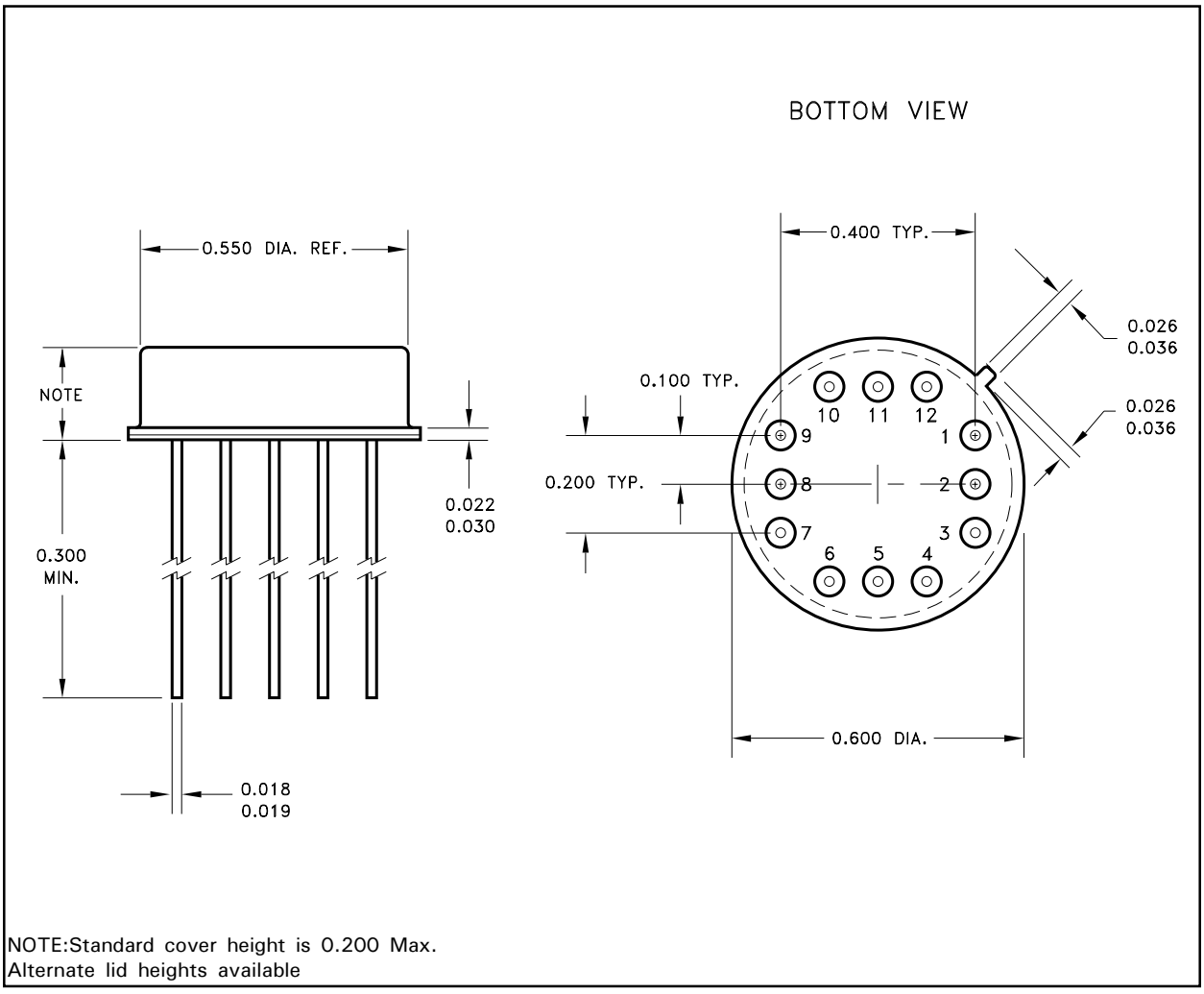
LARGE SIGNAL OPEN LOOP GAIN vs. FREQUENCY



INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



MECHANICAL SPECIFICATIONS



NOTE:Standard cover height is 0.200 Max.
Alternate lid heights available

NOTE: ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED.

ORDERING INFORMATION

Part Number	Screening Level
MSK801	Industrial
MSK801E	Extended Reliability
MSK801B	MIL-PRF-38534 Class H
5962-91574	DSCC-SMD

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