

## Surface Mount Frequency Synthesizer CDMA 738 - 766 MHz



### Features

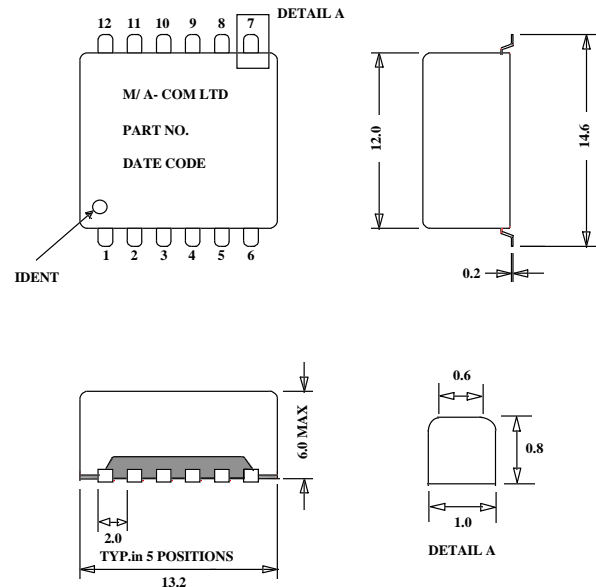
- Integrated VCO/PLL
- Miniature SMT Package
- Low Phase Noise
- +5V Operation

### Description

The MLS9100-00752 synthesizer design integrates a high performance buffered VCO, PLL circuit and discrete loop filter in a surface mount package. The SMT packaging provides electrical shielding, easy PCB assembly and repeatable performance. The synthesizer is designed for use in CDMA base stations and is optimised for coverage of the cellular RX band with 86 MHz IF, 30 kHz step size and low phase noise.

M/A-COM synthesizers are manufactured in an ISO 9001 certified facility, incorporating surface mount assembly and automated electrical testing. This ensures consistent electrical performance and quality over volume production quantities.

### 12 Lead Package



### Electrical Specifications<sup>1</sup>, $T_A = +25^\circ\text{C}$ , $V_{CC} = +5\text{V}$ , $\Delta F = 30\text{ kHz}$ , $F_R = 15\text{ MHz}$ (unless otherwise stated)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency Range ( $F_{OUT}$ ) <sup>2</sup>	Over $T_{OP}$	MHz	738	—	766
RF Output Power ( $P_{OUT}$ ) <sup>3</sup>	Over $T_{OP}$	dBm	-3.0	—	+3.0
Harmonic Output		dBc	—	-18	-15
Spurious Output	Phase comparison frequency ( $F_{OUT} \pm \Delta F$ )	dBc	—	-85	-70
	Reference breakthrough ( $F_{OUT} \pm F_R$ )	dBc	—	-90	—
Phase Noise <sup>4</sup>	SSB at 1 kHz offset from carrier	dBc/Hz	—	-81	-76
	SSB at 10 kHz offset from carrier	dBc/Hz	—	-110	-105
	SSB at 100 kHz offset from carrier	dBc/Hz	—	-130	-125
	SSB at 900 kHz offset from carrier	dBc/Hz	—	-147	—
Integrated Phase Noise	300 Hz to 3 kHz bandwidth	mrad rms	—	8	—
Frequency Switching Time <sup>5,6</sup>	Over $F_{OUT}$ , measured to within $\pm 500\text{ Hz}$	ms	—	30	—
VCO Supply Current ( $I_{CC1}$ )		mA	—	17	20
PLL Supply Current ( $I_{CC2}$ )		mA	—	8	12
VCO Supply Voltage ( $V_{CC1}$ )	Recommended operating limit	V	+4.75	—	+5.25
PLL Supply Voltage ( $V_{CC2}$ )	Recommended operating limit	V	+4.75	—	+5.25
Step Size ( $\Delta F$ ) <sup>7</sup>	Recommended operating limit	kHz	—	30	—
Reference Frequency ( $F_R$ ) <sup>8</sup>	0.5 to 2.0 Vpp sine wave into a.c. coupled CMOS. Recommended operating limit	MHz	3	—	20

1. All specification limits are indicated values and apply over  $F_{OUT}$  and for 50 $\Omega$  load impedance.
2. Programming control is 3 wire serial CMOS or TTL levels, in accordance with National Semiconductor LM511.
3. Output power window includes variation over operating temperature range ( $T_{OP}$ ) -40°C to +85°C and output frequency range ( $F_{OUT}$ ).

4. See plot for typical phase noise at other frequency offsets.
5. See plot for typical full band switching time measured to within other offsets from final frequency.
6. Integral PLL lock monitor output, TTL high locked, TTL low unlocked.
7. Device designed for loop bandwidth of 200Hz.
8. Reference frequency input impedance 10k $\Omega$  min.

V3.00

### Functional Configuration

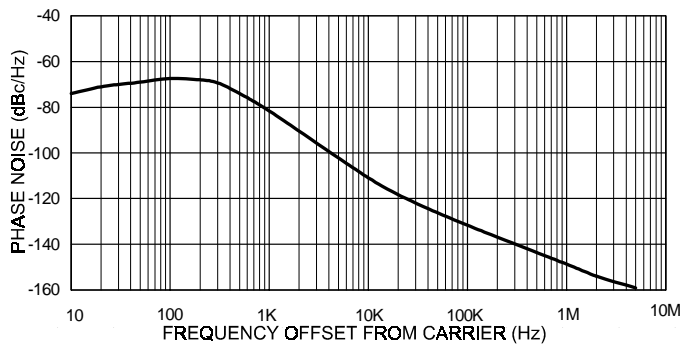
Lead	Function	Lead	Function
1	Ground	7	Ground
2	Clock Input	8	Reference Frequency Input
3	V <sub>CC1</sub> (VCO)	9	V <sub>CC2</sub> (PLL)
4	PLL Lock Monitor Output	10	Data Input
5	RF Output	11	Strobe/Enable Input
6	Ground	12	Ground

### Environmental Specifications

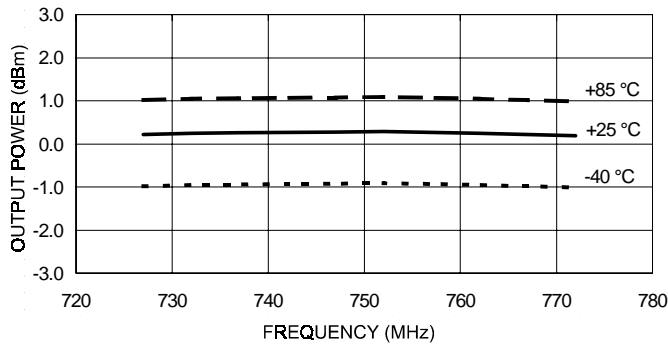
Devices are designed to function over the operating temperature range (T<sub>OP</sub>) of -40°C to +85°C and after exposure to the shock, vibration, thermal shock and moisture conditions typically encountered in base station and other infrastructure environments.

### Typical Performance

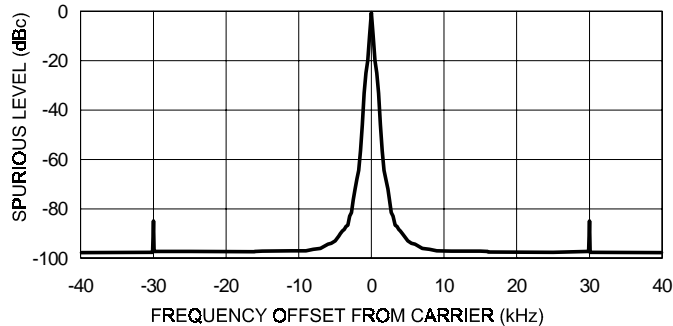
Phase Noise



Output Power vs Temperature



Phase Comparator Spurious



### Absolute Maximum Ratings<sup>1,2</sup>

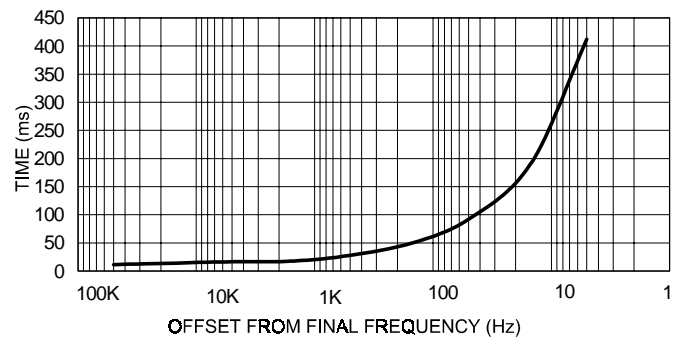
Parameter	Absolute Maximum
VCO Supply Voltage (V <sub>CC1</sub> ) <sup>3</sup>	+6.5V
PLL Supply Voltage (V <sub>CC2</sub> ) <sup>3</sup>	+6.5V
Reference Frequency Voltage	-0.3V to +6.5V
Data, Clock, Strobe Voltages	-0.3V to +6.5V
Storage Temperature (T <sub>STOR</sub> )	-45°C to +125°C
Solder Assembly Temperature	See App Note M2032

1. Exceeding these limits may cause permanent damage.
2. Static sensitive, observe appropriate handling precautions.
3. An external series resistor and bypass capacitor will allow operation at higher supply voltage and will improve power supply decoupling and noise suppression.

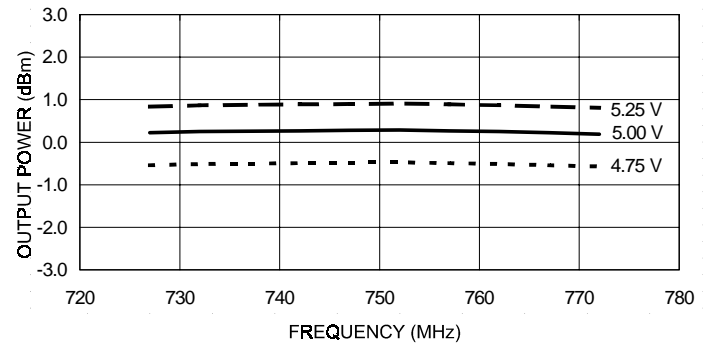
### Ordering Information

Synthesizers are available in either tape and reel or tube packaging. To order devices in tape and reel requires the suffix TR to be added to the part number, i.e. MLS9100-00752TR. Quantity 500 per 13 inch reel, see Application Note M2030.

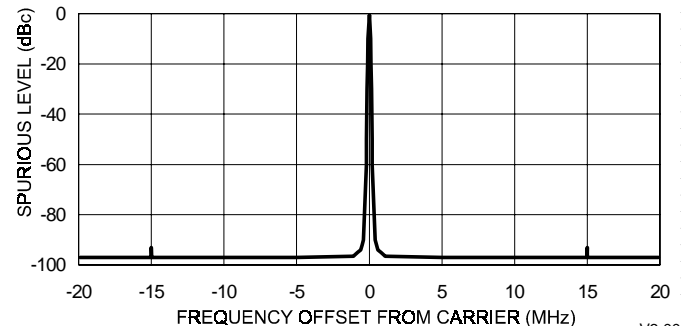
Full Band Switching Time



Output Power vs Supply Voltage (Vcc1)



Reference Breakthrough Spurious



V3.00



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