

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

General Description

The MAX2310/MAX2312/MAX2314/MAX2316 are IF receivers designed for dual-band, dual-mode, and single-mode N-CDMA and W-CDMA cellular phone systems. The signal path consists of a variable gain amplifier (VGA) and I/Q demodulator. The devices feature guaranteed +2.7V operation, a dynamic range of over 110dB, and high input IP3 (-33dBm at 35dB gain, 1.7dBm at -35dB).

Unlike similar devices, the MAX2310 family of receivers includes dual oscillators and synthesizers to form a self-contained IF subsystem. The synthesizer's reference and RF dividers are fully programmable through a 3-wire serial bus, enabling dual-band system architectures using any common reference and IF frequency. The differential baseband outputs have enough bandwidth to suit both N-CDMA and W-CDMA systems, and offer saturated output levels of 2.7Vp-p at a low +2.75V supply voltage. Including the low-noise voltage-controlled oscillator (VCO) and synthesizer, the MAX2310 draws only 26mA from a +2.75V supply in CDMA (differential IF) mode.

The MAX2310/MAX2312/MAX2314/MAX2316 are available in 28-pin QSOP packages.

Applications

Single/Dual/Triple-Mode CDMA Handsets
Globalstar Dual-Mode Handsets
Wireless Data Links
Tetra Direct-Conversion Receivers
Wireless Local Loop (WLL)

Features

- ◆ Complete IF Subsystem Includes VCO and Synthesizer
- ◆ Supports Dual-Band, Triple-Mode Operation
- ◆ VGA with >110dB Gain Control
- ◆ Quadrature Demodulator
- ◆ High Output Level (2.7V)
- ◆ Programmable Charge-Pump Current
- ◆ Supports Any IF Frequency Between 40MHz and 300MHz
- ◆ 3-Wire Programmable Interface
- ◆ Low Supply Voltage (+2.7V)

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------------|----------------|-------------|
| MAX2310EEI | -40°C to +85°C | 28 QSOP |
| MAX2312EEI | -40°C to +85°C | 28 QSOP |
| MAX2314EEI | -40°C to +85°C | 28 QSOP |
| MAX2316EEI | -40°C to +85°C | 28 QSOP |

Pin Configurations appear at end of data sheet.

Block Diagram appears at end of data sheet.

Selector Guide

| PART | MODE | DESCRIPTION | INPUT RANGE |
|---------|-------------------------------------|--|-----------------|
| MAX2310 | AMPS, Cellular CDMA, PCS CDMA | Dual Band, Triple Mode | 40MHz to 300MHz |
| MAX2312 | PCS CDMA | Single Band, Single Mode | 67MHz to 300MHz |
| MAX2314 | AMPS, Cellular CDMA | Single Band, Dual Mode | 40MHz to 150MHz |
| MAX2316 | Cellular CDMA | Single Band, Single Mode or Single Band, Dual Mode with External Discriminator | 40MHz to 150MHz |

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

ABSOLUTE MAXIMUM RATINGS

| | | | |
|--|--|---|-----------------|
| V _{CC} to GND | -0.3V, +6.0V | Digital Input Current $\overline{\text{SHDN}}$, MODE, DIVSEL, BUFEN, DATA, CLK, EN, STBY | ±10mA |
| SHDN to GND | -0.3V to (V _{CC} + 0.3V) | Continuous Power Dissipation (T _A = +70°C) 28-pin QSOP (derate 10mW/°C above T _A = +70°C) | 800mW |
| STBY, BUFEN, MODE, EN, DATA, CLK, DIVSEL | -0.3V to (V _{CC} + 0.3V) | Operating Temperature Range | -40°C to +85°C |
| VGC to GND | -0.3V, the lesser of +4.2V or (V _{CC} + 0.3V) | Junction Temperature | +150°C |
| AC Signals TankH ±, TankL ±, REF, FM ±, CDMA ± | 1.0V peak | Storage Temperature Range | -65°C to +160°C |
| | | Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, MODE = DIVSEL = $\overline{\text{SHDN}}$ = $\overline{\text{STBY}}$ = $\overline{\text{BUFEN}}$ = high, differential output load = 10kΩ, T_A = -40°C to +85°C, registers set to default power-up settings. Typical values are at V_{CC} = +2.75V and T_A = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------------------|-----------------------------------|---------------------------------|-----------------------|------|-------|
| Supply Current (Note 1) | I _{CC} | CDMA mode | T _A = +25°C | 25.9 | 37.5 | mA |
| | | | T _A = -40°C to +85°C | | 41.5 | |
| | | FM IQ mode | T _A = +25°C | 25.4 | 36.7 | |
| | | | T _A = -40°C to +85°C | | 40.6 | |
| | | FM I mode | T _A = +25°C | 24.7 | 35.7 | |
| | | | T _A = -40°C to +85°C | | 39.5 | |
| | | STANDBY (VCO_H) | T _A = +25°C | 12.3 | 18.8 | |
| | | | T _A = -40°C to +85°C | | 20.7 | |
| STANDBY (VCO_L) | T _A = +25°C | 11.5 | 18.4 | | | |
| | T _A = -40°C to +85°C | | 20.3 | | | |
| Addition for LO out ($\overline{\text{BUFEN}}$ = low) | | | 3.5 | | | |
| Shutdown Current | I _{CC} | $\overline{\text{SHDN}}$ = low | | 1.5 | 10 | μA |
| Register Shutdown Current | I _{CC} | | | 3 | 5.8 | mA |
| Logic High | | | 2.0 | | | V |
| Logic Low | | | | | 0.5 | V |
| Logic High Input Current | I _{IH} | | 2 | | | μA |
| Logic Low Input Current | I _{IL} | | | | 2 | μA |
| VGC Control Input Current | | 0.5V < V _{VGC} < 2.3V | -5 | | 5 | μA |
| VGC Control Input Current During Shutdown | | $\overline{\text{SHDN}}$ = low | | | 1 | μA |
| Lock Indicator High (locked) | | 50kΩ load | 2.0 | | | V |
| Lock Indicator Low (unlocked) | | 50kΩ load | | | 0.5 | V |
| DC Offset Voltage | | I+ to I- and Q+ to Q-, PLL locked | -20 | ±1.5 | +20 | mV |
| Common-Mode Output Voltage | | V _{CC} = 2.75V | | V _{CC} - 1.4 | | V |

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316

AC ELECTRICAL CHARACTERISTICS

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $V_{CC} = +2.75V$, registers set to default power-up states, $f_{IN} = 210.88MHz$ for CDMA, $f_{IN} = 85.88MHz$ for FM, $f_{REF} = 19.68MHz$, synthesizer locked with passive 2nd-order lead-lag loop filter, $\overline{SHDN} = high$, VGC set for +35dB voltage gain, differential output load = 10k Ω , all power levels referred to 50 Ω , $T_A = +25^\circ C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------|---|--------------|-----------|-------|-------|
| Input Frequency | f_{IN} | (Note 2) | 40 | | 300 | MHz |
| Reference Frequency | f_{REF} | (Note 2) | | | 39 | MHz |
| Frequency Reference Signal Level | V_{REF} | | 0.2 | | | Vp-p |
| SIGNAL PATH, CDMA MODE | | | | | | |
| Input Third-Order Intercept | IIP3 | Gain = -35dB (Note 3) | | 1.7 | | dBm |
| | | Gain = +35dB (Note 4) | | -33.2 | | |
| Input 1dB Compression | P1dB | Gain = -35dB | -9 | -6.4 | | dBm |
| | | Gain = +35dB | -44 | -38.3 | | |
| Input 0.25dB Desensitization | | (Note 5) | Gain = -35dB | | -14.8 | dBm |
| | | | Gain = +35dB | | -49 | |
| Minimum Voltage Gain | A_V | $V_{GC} = 0.5V$ (Note 6) | | -54.8 | -49 | dB |
| Maximum Voltage Gain | A_V | $V_{GC} = 2.3V$ (Note 6) | 56 | 61.3 | | dB |
| DSB Noise Figure | NF | Gain = -35dB | | 62.9 | | dB |
| | | Gain = +35dB | | 6.36 | | |
| SIGNAL PATH, FM_IQ MODE | | | | | | |
| Input Third-Order Intercept | IIP3 | (Note 7) | Gain = -35dB | | -6.0 | dBm |
| | | | Gain = +35dB | | -31 | |
| Input 1dB Compression | P1dB | (Notes 6, 8) | Gain = -35dB | -20 | -16.2 | dBm |
| | | | Gain = +35dB | -44 | -38.4 | |
| Minimum Voltage Gain | A_V | $V_{GC} = 0.5V$ (Note 6) | | -50.2 | -47.4 | dB |
| Maximum Voltage Gain | A_V | $V_{GC} = 2.3V$ (Note 6) | 58.5 | 63.4 | | dB |
| SIGNAL PATH, CDMA and FM_IQ MODE | | | | | | |
| Maximum Gain Variation Over Temperature | | Normalized to +25 $^\circ C$ | | ± 2.5 | | dB |
| Baseband 0.5dB Bandwidth | | | | 4.2 | | MHz |
| Quadrature Suppression | | $T_A = T_{MIN}$ to T_{MAX} (Note 6) | +28 | +35 | | dB |
| LO to Baseband Leakage | | | | 1 | | mVp-p |
| Saturated Output Level | V_{SAT} | Differential | | 2.7 | | Vp-p |
| PHASE-LOCKED LOOP | | | | | | |
| VCO Tune Range | f_{VCO_L} | (Note 2) | 80 | | 300 | MHz |
| | f_{VCO_H} | | 135 | | 600 | |
| LOOUT Output Power | P_{LO} | $R_L = 50\Omega$, $\overline{BUFEN} = low$ | | -13.7 | | dBm |

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $V_{CC} = +2.75V$, registers set to default power-up states, $f_{IN} = 210.88MHz$ for CDMA, $f_{IN} = 85.88MHz$ for FM, $f_{REF} = 19.68MHz$, synthesizer locked with passive 2nd-order lead-lag loop filter, $\overline{SHDN} = high$, VGC set for +35dB voltage gain, differential output load = $10k\Omega$, all power levels referred to 50Ω , $T_A = +25^\circ C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|---|-------|------|------|---------|
| VCO Minimum Divide Ratio | M1, M2 | | | | 256 | |
| VCO Maximum Divide Ratio | M1, M2 | | 16383 | | | |
| REF Minimum Divide Ratio | R1, R2 | | | | 2 | |
| REF Maximum Divide Ratio | R1, R2 | | 2047 | | | |
| Minimum Phase Detector Comparison Frequency | | (Note 6) | | | 20 | kHz |
| Maximum Phase Detector Comparison Frequency | | (Note 6) | 1500 | | | kHz |
| Base Band Spurious due to PLL | | | | | -50 | dBc |
| LOOUT at 85MHz, VCO_L Enabled (Note 9) | | 1kHz offset | | -72 | | dBc/Hz |
| | | 12.5kHz offset | | -100 | | |
| | | 30kHz offset | | -110 | | |
| | | 120kHz offset | | -119 | | |
| | | 900kHz offset | | -125 | | |
| LOOUT at 210MHz, VCO_H Enabled (Note 9) | | 1kHz offset | | -64 | | dBc/Hz |
| | | 12.5kHz offset | | -91 | | |
| | | 30kHz offset | | -105 | | |
| | | 120kHz offset | | -115 | | |
| | | 900kHz offset | | -125 | | |
| Charge-Pump Source/Sink Current | | Acquisition, CPX = XX, TC = 1 (Note 10) | 1480 | 2100 | 2650 | μA |
| | | Locked, CPX = 00 | 105 | 150 | 190 | |
| | | Locked, CPX = 01 | 150 | 210 | 265 | |
| | | Locked, CPX = 10 | 210 | 300 | 380 | |
| | | Locked, CPX = 11 | 300 | 425 | 530 | |
| Charge-Pump Source/Sink Matching | | Locked, all values of CPX, $0.5V < V_{CP} < V_{CC} - 0.5V$ | | 0.2 | 10 | % |

Note 1: FM_IQ and FM_I modes are not available on MAX2312 and MAX2316.

Note 2: Recommended operating frequency range.

Note 3: $f_1 = 210.88MHz$, $f_2 = 210.89MHz$, $P_{f1} = P_{f2} = -15dBm$.

Note 4: $f_1 = 210.88MHz$, $f_2 = 210.89MHz$, $P_{f1} = P_{f2} = -50dBm$.

Note 5: Small-signal gain at 200kHz below the LO frequency will be reduced by less than 0.25dB when an interfering signal at 1.25MHz below the LO frequency is applied at the specified level.

Note 6: Guaranteed by design and characterization.

Note 7: $f_1 = 85.88MHz$, $f_2 = 85.98MHz$, $P_{f1} = P_{f2} = -15dBm$.

Note 8: $f_1 = 85.88MHz$, $f_2 = 85.98MHz$, $P_{f1} = P_{f2} = -50dBm$.

Note 9: Measured at LOOUT with BD = 0 (+2 selected).

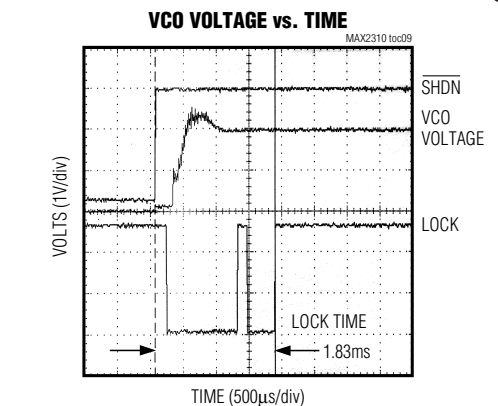
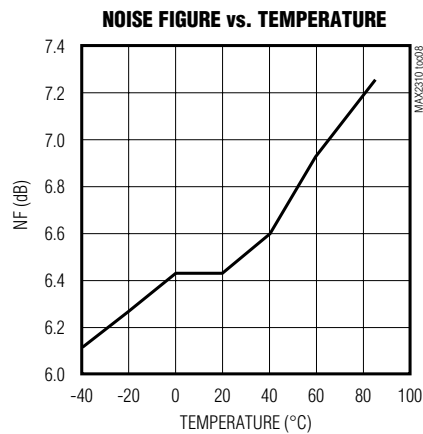
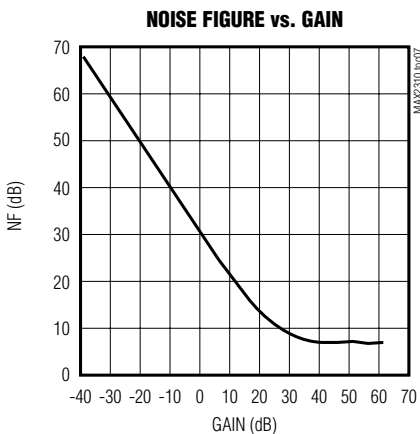
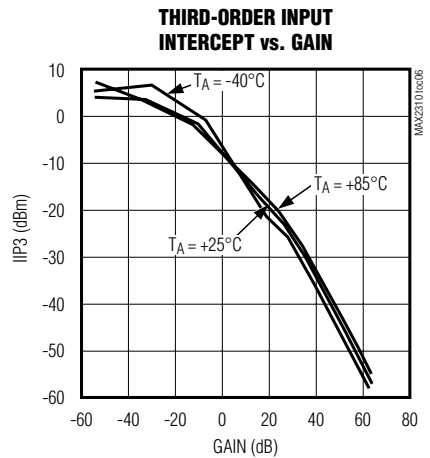
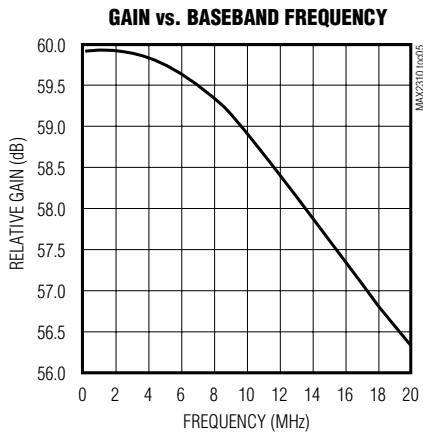
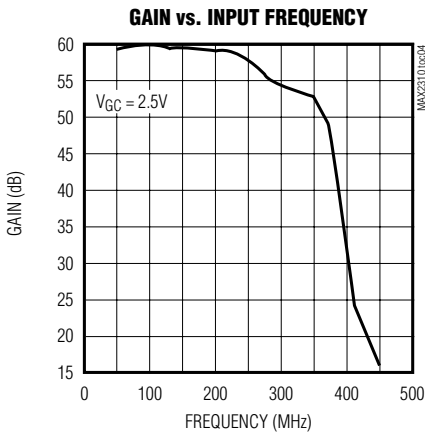
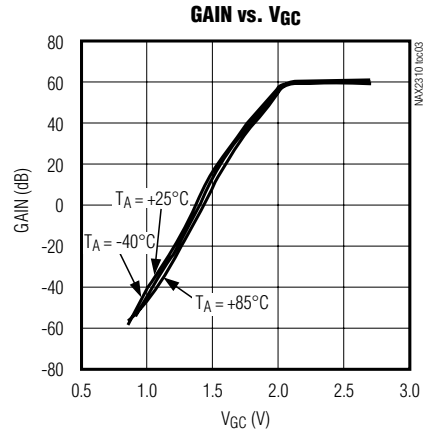
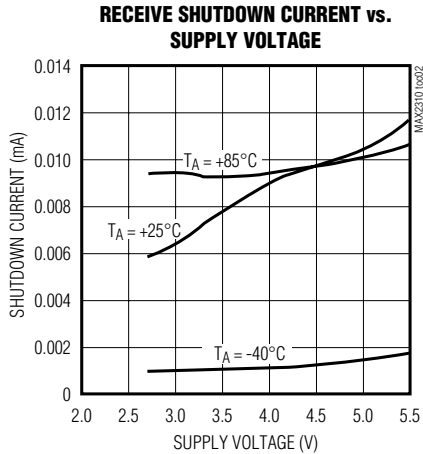
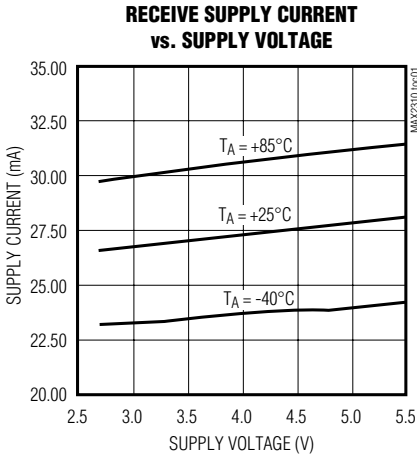
Note 10: Not available on MAX2316.

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Typical Operating Characteristics

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $V_{CC} = +2.75V$, registers set to default power-up states, $f_{IN} = 210.88MHz$ for CDMA, $f_{IN} = 85.88MHz$ for FM, $f_{REF} = 19.68MHz$, synthesizer locked with passive 2nd-order lead-lag loop filter, $\overline{SHDN} = high$, V_{GC} set for +35dB voltage gain, differential output load = $10k\Omega$, all power levels referred to 50Ω , $T_A = +25^\circ C$, unless otherwise noted.)

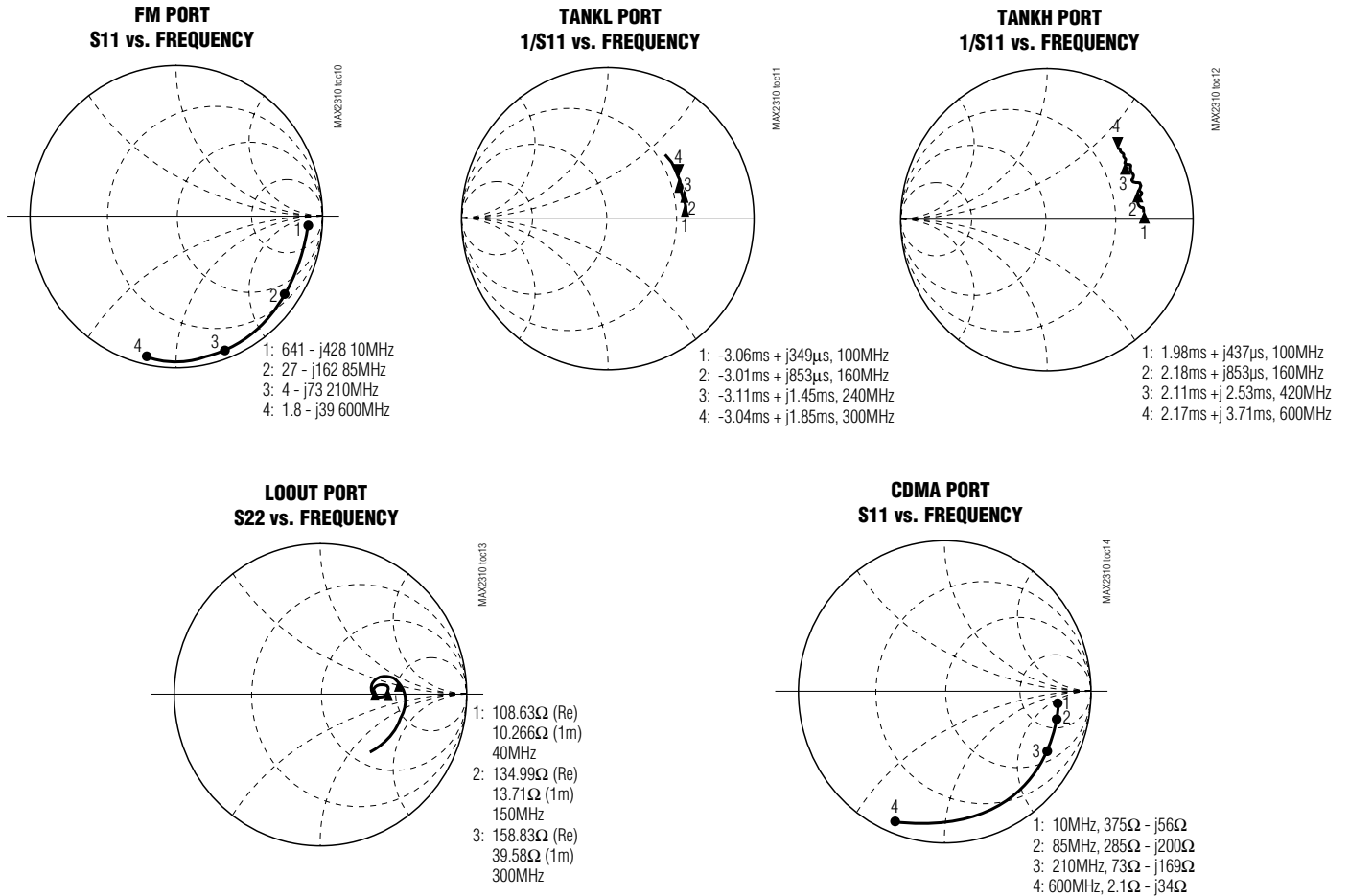
MAX2310/MAX2312/MAX2314/MAX2316



CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Typical Operating Characteristics (continued)

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $V_{CC} = +2.75V$, registers set to default power-up states, $f_{IN} = 210.88MHz$ for CDMA, $f_{IN} = 85.88MHz$ for FM, $f_{REF} = 19.68MHz$, synthesizer locked with passive 2nd-order lead-lag loop filter, $\overline{SHDN} = high$, VGC set for +35dB voltage gain, differential output load = $10k\Omega$, all power levels referred to 50Ω , $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

| PIN | | | | NAME | FUNCTION |
|---------|---------|---------|---------|-------------------|--|
| MAX2310 | MAX2312 | MAX2314 | MAX2316 | | |
| 1 | 1 | 1, 8 | 1 | BYP | Bypass Node. Must be capacitively decoupled (bypassed) to analog ground. |
| 2 | 2 | 2 | 2 | CP_OUT | Charge-Pump Output |
| 3 | 3 | 3 | 3 | GND | Analog Ground Reference |
| 4, 5 | — | 4, 5 | 5, 6 | TANKL+, TANKL- | Differential Tank Input for Low-Frequency Oscillator |
| — | 4 | — | 4 | DIVSEL | High selects M1/R1; low selects M2/R2. |

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Pin Description (continued)

| PIN | | | | NAME | FUNCTION |
|---------|---------|---------|---------|---------------------------|--|
| MAX2310 | MAX2312 | MAX2314 | MAX2316 | | |
| 6, 7 | 5, 6 | — | — | TANKH+, TANKH- | Differential Tank Input for High-Frequency Oscillator |
| — | 7 | — | 7 | $\overline{\text{BUFEN}}$ | LO Buffer Amplifier—active low |
| — | — | 6, 7 | — | N.C. | No Connection. Must be left open-circuit. |
| 8 | — | — | — | MODE | Mode Select. High selects CDMA mode; low selects FM mode. |
| — | 8 | — | 8 | LOOUT | Internal VCO Output. Depending on setting of BD bit, LOOUT is either the VCO frequency (twice the IF frequency) or one-half the VCO frequency (equal to the IF frequency). |
| 9 | 9 | 9 | 9 | V _{CC} | +2.7V to +5.5V Supply for Digital Circuits |
| 10 | 10 | 10 | 10 | GND | Digital Ground |
| 11 | 11 | 11 | 11 | REF | Reference Frequency Input |
| 12 | 12 | 12 | 12 | $\overline{\text{SHDN}}$ | Shutdown Input—active low. Low powers down entire device, including registers and serial interface. |
| 13, 14 | 13, 14 | 13, 14 | 13, 14 | IOUT+, IOUT- | Differential In-Phase Baseband Output, or FM signal output FM_I mode is selected. |
| 15 | 15 | 15 | 15 | LOCK | Lock Output—open-collector pin. Logic high indicates phase-locked condition. |
| 16, 17 | 16, 17 | 16, 17 | 16, 17 | QOUT-, QOUT+ | Differential Quadrature-Phase Baseband Output. Disabled if FM_I mode is selected. |
| 18 | 18 | 18 | 18 | CLK | Clock input of the 3-wire serial bus |
| 19 | 19 | 19 | 19 | $\overline{\text{EN}}$ | Enable Input. When low, input shift register is enabled. |
| 20 | 20 | 20 | 20 | DATA | Data input of the 3-wire serial bus. |
| 21 | 21 | 21 | 21 | V _{CC} | 2.7V to 5.5V Supply for Analog Circuits |
| 22 | 22 | 22 | 22 | VGC | VGA Gain Control Input. Control voltage range is 0.5V to 2.3V. |
| 23, 24 | 23, 24 | 23, 24 | 23, 24 | CDMA-, CDMA+ | Differential CDMA Input. Active in CDMA mode. |
| 25 | — | 25 | — | FM+ | Differential Positive Input. Active in FM mode. |
| — | 25 | — | 25 | N.C. | No Connection. |
| 26 | — | 26 | — | FM- | Differential Negative Input for FM signal. Bypass to GND for single-ended operation. |
| — | 26 | — | 26 | $\overline{\text{STBY}}$ | Standby Input—active low. Low powers down VGA and demodulator while keeping VCO, PLL, and serial bus on. |
| 27, 28 | 27, 28 | 27, 28 | 27, 28 | BYP | Bypass Node. Must be capacitively decoupled (bypassed) to analog V _{CC} . |

MAX2310/MAX2312/MAX2314/MAX2316

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

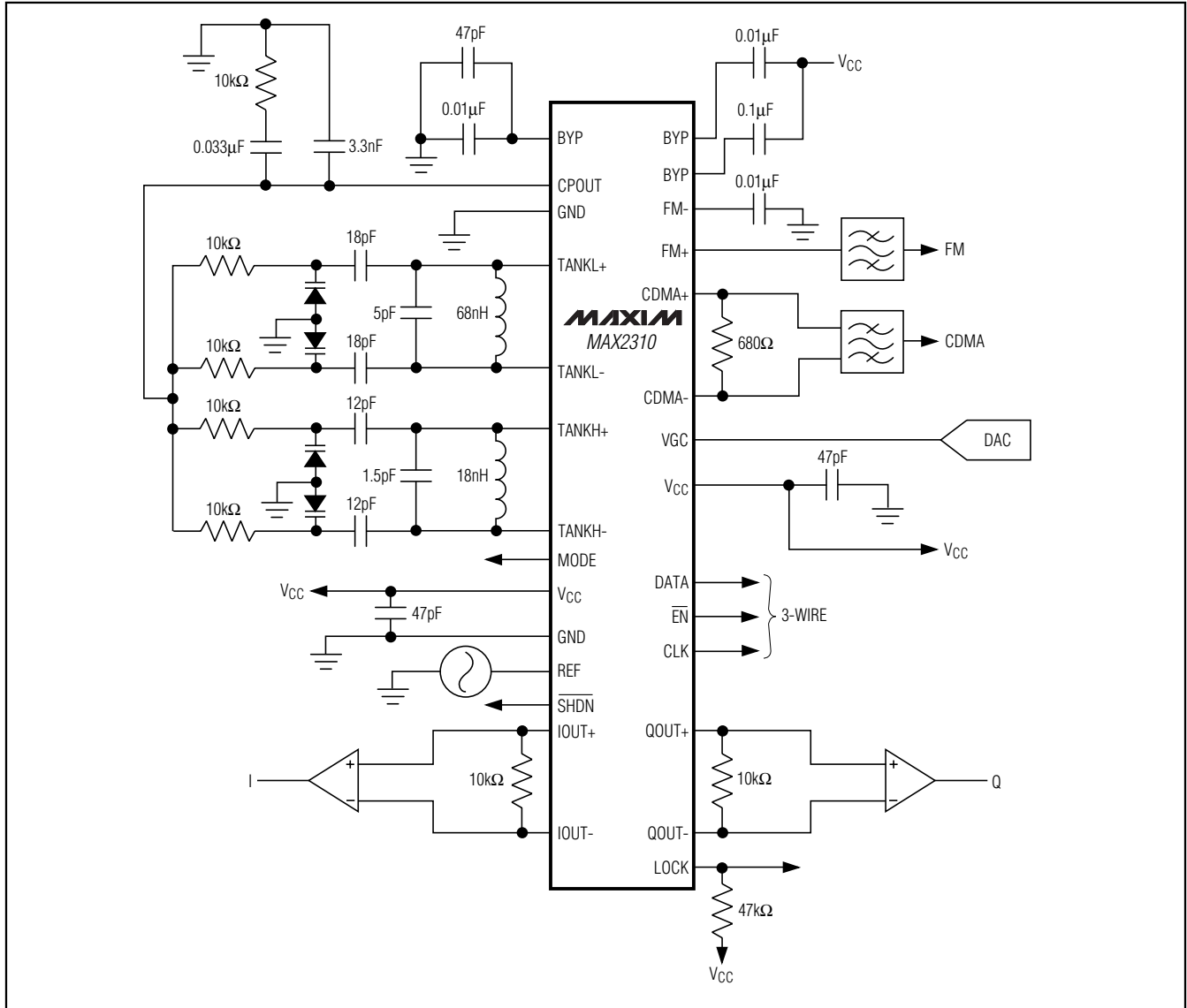


Figure 1. MAX2310 Typical Operating Circuit

Detailed Description

MAX2310

The MAX2310 is intended for dual-band (PCS and cellular) and dual-mode code division multiple access (CDMA) and FM applications (Figure 1). The device includes an IF variable-gain amplifier, quadrature demodulator, dual VCOs, and dual-frequency synthesizers (Figure 7). Dual VCOs are provided for applications using different IF frequencies for each mode or band of operation. The analog FM output signal can be

configured for conversion to the I channel, or it may be converted in quadrature to both the I and Q channels. The MAX2310's operation modes are described in Table 1. These modes are set by programming the control register and setting logic levels on control pins. If MODE is left floating, the internal register controls the operation. If driven high or low, mode will override certain register bits, as shown in Table 1.

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316

Table 1. MAX2310 Control Register States

| OPERATIONAL MODE | ACTION RESULT | PINS | | CONTROL REGISTER | | | | | | | | | | | | | LSB |
|------------------|--|--------|------|------------------|--------|---------|-------------|--------|---------|---------|---------|-------|---------|--------|------|------|-----|
| | | SHDN | MODE | TEST_MODE | CP POL | TEST_EN | TURBOCHARGE | DIVSEL | VCO_BYP | VCO_SEL | BUF_DIV | BUFEN | FM_TYPE | IN_SEL | STBY | SHDN | |
| SHUTDOWN | Shutdown pin completely powers down the chip | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| SHUTDOWN | 0 in shutdown register bit leaves serial port active | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 |
| STANDBY | 0 in standby register bit turns off VGA and modulator only | H | X | X | X | 0 | | | | | | X | X | | | 0 | 1 |
| CDMA | Mode pin overrides VCO_SEL, DIVSEL, and IN_SEL to high | H | H | | | 0 | | X | | X | X | X | X | X | 1 | 1 | |
| CDMA | Floating mode pin returns control to register | H | F | | | 0 | | 1 | | 1 | X | X | X | 1 | 1 | 1 | |
| FM_IQ | Mode pin overrides VCO_SEL, DIVSEL, and IN_SEL to low | H | L | | | 0 | | X | | X | X | X | 0 | X | 1 | 1 | |
| FM_IQ | Floating mode pin returns control to register | H | F | | | 0 | | | | | X | X | 0 | 0 | 1 | 1 | |
| FM_I | Mode pin overrides VCO_SEL, DIVSEL, and IN_SEL to low | H | L | | | 0 | | X | | X | X | X | 1 | X | 1 | 1 | |
| FM_I | Floating pins return control to register | H L | F | | | 0 | | | | | X | X | 1 | 0 | 1 | 1 | |

Note: H = high, L = low, F = floating pin, X = don't care, Blank = independent parameter, 1 = logic high, 0 = logic low.

MAX2312/MAX2316

The MAX2312/MAX2316 quadrature demodulators are simplified versions of the MAX2310 that can be used in single-mode CDMA or dual mode using an external FM discriminator (Figures 2a and 2b). The MAX2312 VCO is optimized for the 67MHz to 300MHz IF frequency range, while the MAX2316 VCO is optimized for the 40MHz to 150MHz IF frequency range.

Both devices include a buffered output for the VCO. The buffered VCO output can be used to support systems implementing traditional limiting IF stages for FM demodulation in dual-mode phones as well as for the transmit LO in TDD systems. This buffered output can

be configured for the VCO frequency (twice the IF frequency) or one-half the VCO frequency (IF frequency). The BUFEN pin enables this feature. A standby mode, in which only the VCO and synthesizer are operational, can be selected through the serial interface or the STBY pin. The MAX2312/MAX2316s' operational modes are described in Table 2. These modes are set by programming the control register and/or setting logic levels on control pins. If the control pins (STBY, BUFEN, DIVSEL) are left floating, the internal register controls the operational mode. If driven high or low, the control pins will override certain register bits, as shown in Table 2.

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

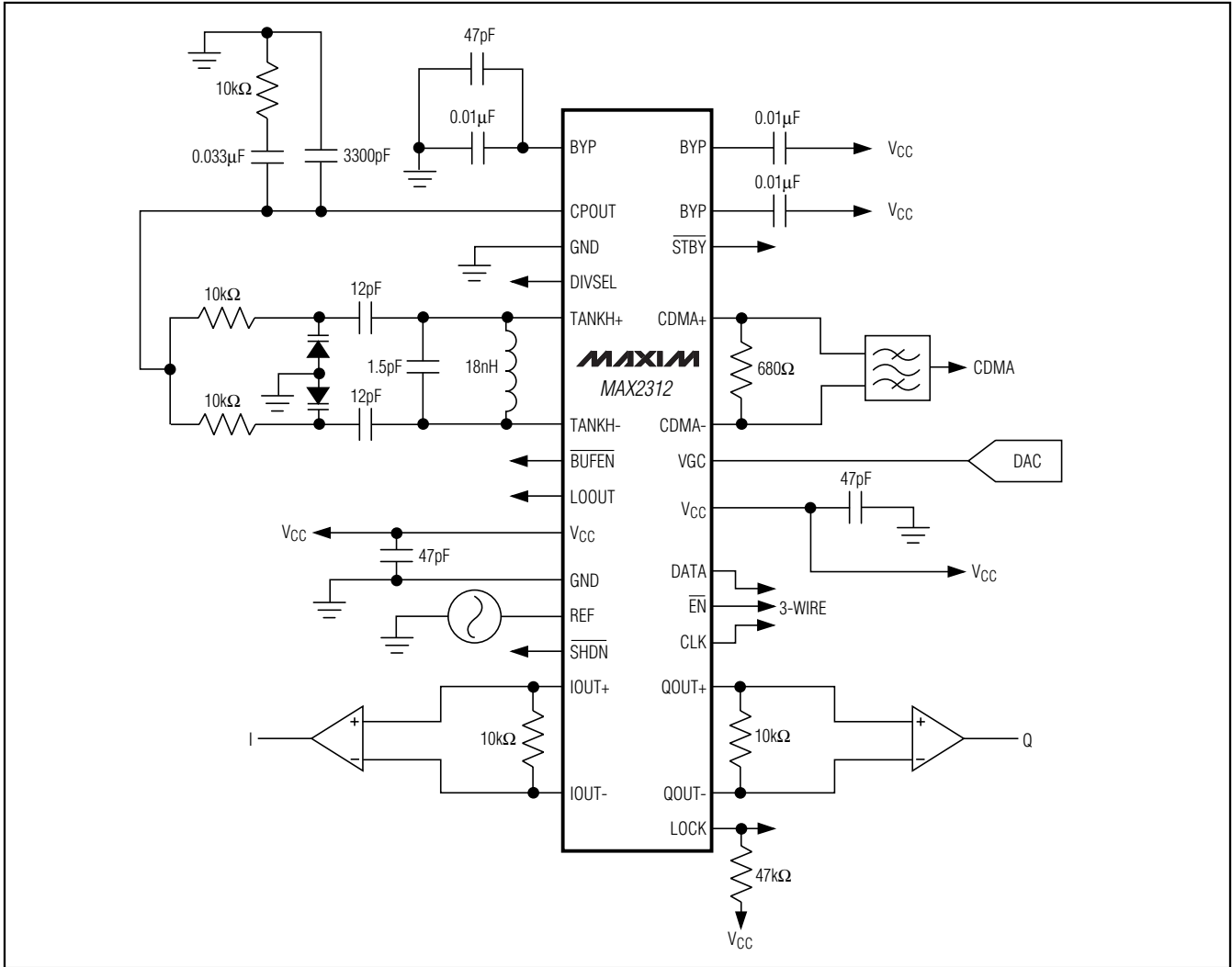


Figure 2a. MAX2312 Typical Operating Circuit

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316

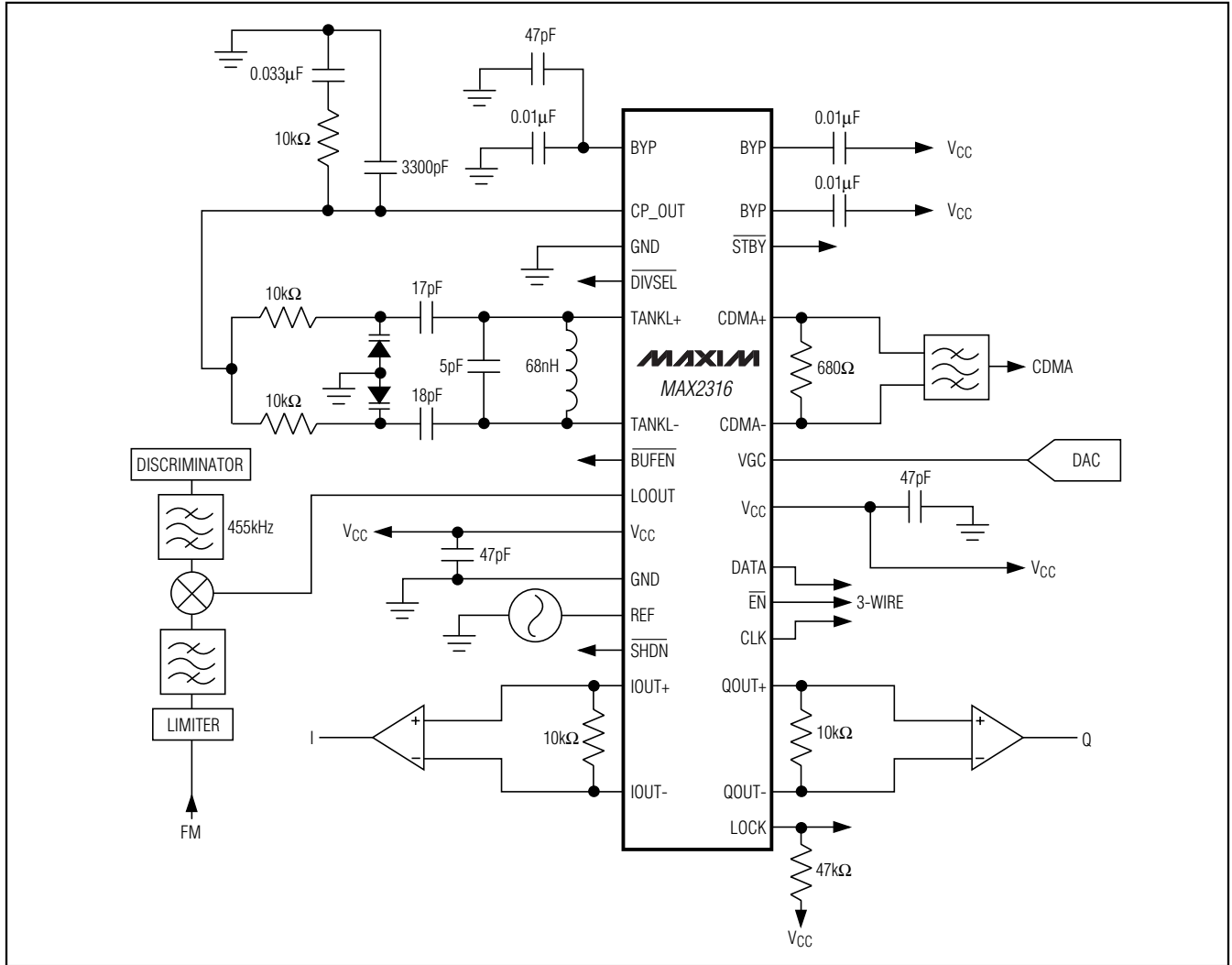


Figure 2b. MAX2316 Typical Operating Circuit

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Table 2. MAX2312/MAX2316 Control Register States

| OPERATIONAL MODE | ACTION RESULT | PINS | | | | CONTROL REGISTER | | | | | | | | | | | | L S B |
|------------------|--|------|--------|-------|------|------------------|--------|---------|-------------|--------|---------|---------|---------|-------|---------|--------|------|-------|
| | | SHDN | DIVSEL | BUFEN | STBY | TEST_MODE | CP_POL | TES_TEN | TURBOCHARGE | DIVSEL | VCO_BYP | VCO_SEL | BUF_DIV | BUFEN | FM_TYPE | IN_SEL | STBY | |
| SHUTDOWN | Shutdown pin completely powers down the chip | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| SHUTDOWN | 0 in shutdown register bit leaves serial bus active | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 |
| STANDBY | 0 in standby pin turns off VGA and modulator only | H | | | L | | | 0 | | | | X | | | | | X | 1 |
| STANDBY | 0 in standby register bit turns off VGA and modulator only | H | H/L | H | | | | 0 | | | | X | | | | | 0 | 1 |
| DIVIDER SELECT | DIV_SEL pin overrides DIV_SEL register bit | H | H/L | | H | | | 0 | | X | | X | | | | | | 1 |
| DIVIDER SELECT | If DIV_SEL pin is floated, then register bit selects divider | H | F | | H | | | 0 | | 1/0 | | X | | | | | | 1 |
| LO BUFFER ENABLE | BUFEN pin controls the LO buffer and overrides the bit | H/L | | H | | | | 0 | | | | X | | X | | | | 1 |
| LO BUFFER ENABLE | If pin is floated, then BUFEN register bit controls buffer | H | | F | | | | 0 | | | | X | | 1/0 | | | | 1 |

Note: H = high, L = low, 1 = logic high, 0 = logic low, X = don't care, blank = independent parameter.

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Table 3. MAX2314 Control Register States

| OPERATIONAL MODE | ACTION RESULT | PIN | CONTROL REGISTER | | | | | | | | | | | | | LSB |
|------------------|--|------|------------------|--------|---------|-------------|--------|---------|---------|---------|-------|---------|--------|------|------|-----|
| | | SHDN | TEST_MODE | CP_POL | TEST_EN | TURBOCHARGE | DIVSEL | VCO_BYP | VCO_SEL | BUF_DIV | BUFEN | FM_TYPE | IN_SEL | STBY | SHDN | |
| SHUTDOWN | Shutdown pin completely shuts down chip | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| SHUTDOWN | 0 in shutdown register bit leaves serial port active | H | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| STANDBY | 0 in standby pin turns off VGA and modulator only | H | | | 0 | | | | 0 | X | X | | | 0 | 1 | |
| CDMA | CDMA operation | H | | | 0 | | | | 0 | X | X | X | 1 | 1 | 1 | |
| FM_IQ | FM IQ quadrature operation | H | | | 0 | | | | 0 | X | X | 0 | 0 | 1 | 1 | |
| FM_I | FM I operation | H | | | 0 | | | | 0 | X | X | 1 | 0 | 1 | 1 | |

Note: H = high, L = low, 1 = logic high, 0 = logic low, X = don't care, blank = independent parameter

the VGC pin. The output of the VGA drives the RF ports of a quadrature demodulator. The MAX2310/MAX2314 provide two types of FM demodulation, controlled by the FM_TYPE (FT) control bit. When FM_TYPE is "1," the signal is passed through both the I and Q signal paths for subsequent lowpass filtering and A/D conversion at baseband. If FM_TYPE is "0," the FM signal is passed through the I mixer only.

Voltage-Controlled Oscillator, Buffers, and Quadrature Generation

The LO signal for downconversion is provided by a voltage-controlled oscillator (VCO) consisting of an on-chip differential oscillator, and an off-chip high-Q resonant network. Figure 4 shows a simplified schematic of the VCO oscillator. Multiband operation is supported by the MAX2310 with dual VCOs. VCO_H and VCO_L are selectable with the MODE pin or the VCO_SEL (VS)

control bit. They oscillate at twice the desired LO frequency. For applications requiring an external LO, the VCOs can be bypassed with the VCO_BYP (VB) control bit.

The MAX2312/MAX2316 buffer the output of the VCO and provide this signal at the LOOUT pin. This signal is enabled by the BUFEN (BE) control bit or by the BUFEN control pin. The frequency of this signal is selected by the BUF_DIV (BD) control bit, and can be either the VCO frequency or half the VCO frequency.

Quadrature downconversion is realized by providing in-phase (I) and quadrature-phase (Q) components of the LO signal to the LO ports of the demodulator described above. The quadrature LO signals are generated by dividing the VCO output frequency using two latches. The appropriate latch outputs provide I and Q signals at the desired LO frequency.

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316

Synthesizer

The VCO's output frequency is controlled by an internal phase-locked-loop (PLL) dual-modulus synthesizer. The loop filter is off-chip to simplify loop design for emerging applications. The tunable resonant network is also off-chip for maximum Q and for system design flexibility. The VCO output frequency is divided down to the desired comparison frequency with the M counter. The M counter consists of a 4-bit A swallow counter and a 10-bit P counter. A reference signal is provided from an external source and is divided down to the comparison frequency with the R counter. The two divided signals are compared with a three-state digital phase-frequency detector. The phase-detector output drives a charge pump as well as lock-detect logic and turbocharge control logic. The charge pump output (CP_OUT) pin is processed by the loop filter and drives the tunable resonant network, altering the VCO frequency and closing the loop.

Multimode applications are supported by two independent programmable registers each for the M counter (M1, M2), the R counter (R1, R2), and the charge-pump output current magnitude (CP1, CP2). The DIVSEL (DS) bit selects which set of registers is used. It can be overridden by the MAX2310's MODE pin or the MAX2312/MAX2316's DIVSEL pin. Programming these registers is discussed in the *3-Wire Interface and Registers* section.

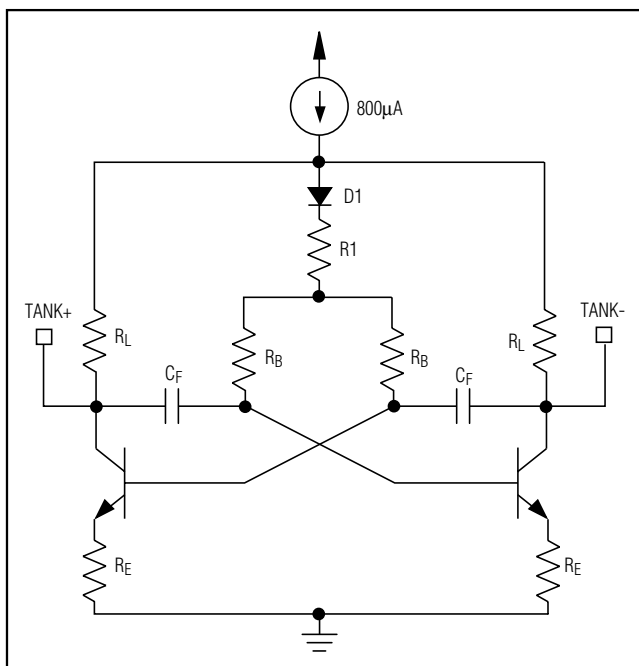


Figure 4. Voltage-Controlled Oscillators

When the part initially powers up or changes state, the synthesizer acquisition time can be reduced by using the Turbo feature, enabled by the TURBOCHARGE (TC) control bit. Turbo functionality provides a larger charge-pump current during acquisition mode. Once the VCO frequency is acquired, the charge-pump output current magnitude automatically returns to the pre-programmed state to maintain loop stability and minimize spurs in the VCO output signal.

The lock detect output indicates when the PLL is locked with a logic high.

3-Wire Interface and Registers

The MAX2310 family incorporates a 3-wire interface for synthesizer programming and device configuration (Figure 5). The 3-wire interface consists of a clock, data, and $\overline{\text{ENABLE}}$. It controls the VCO dividers (M1 and M2), reference frequency dividers (R1 and R2), and a 13-bit control register. The control register is used to set up the operational modes (Table 4). The input shift is 17 data bits long and requires a total of 18 clock bits (Figure 6). A single clock pulse is required before enable drops low to initialize the data bus.

Whenever the M or R divide register value is programmed and downloaded, the control register must also be subsequently updated. This prevents turbolock from going active when not desired.

The $\overline{\text{SHDN}}$ control bit is notable because it differs from the SHDN pin. When the $\overline{\text{SHDN}}$ control bit is low, the registers and serial interface are left active, retaining the values stored in the latches, while the rest of the device is shut off. In contrast, the SHDN pin, when low, shuts down everything, including the registers and serial interface. See the functional diagram in Figure 7.

Registers

Figure 8 shows the programming logic. The 17-bit shift register is programmed by clocking in data at the rising edge of CLK. Before the shift register is able to accept data, it must be initialized by driving it with at least one full clock cycle at the CLK input with $\overline{\text{EN}}$ high (see Figure 6). Pulling enable low will allow data to be clocked into the shift register; pulling enable high loads the register addressed by A0, A1, and A2, respectively (Figure 8). Table 5 lists the power-on default values of all registers. Table 6 lists the charge-pump current, depending on CP0 and CP1.

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

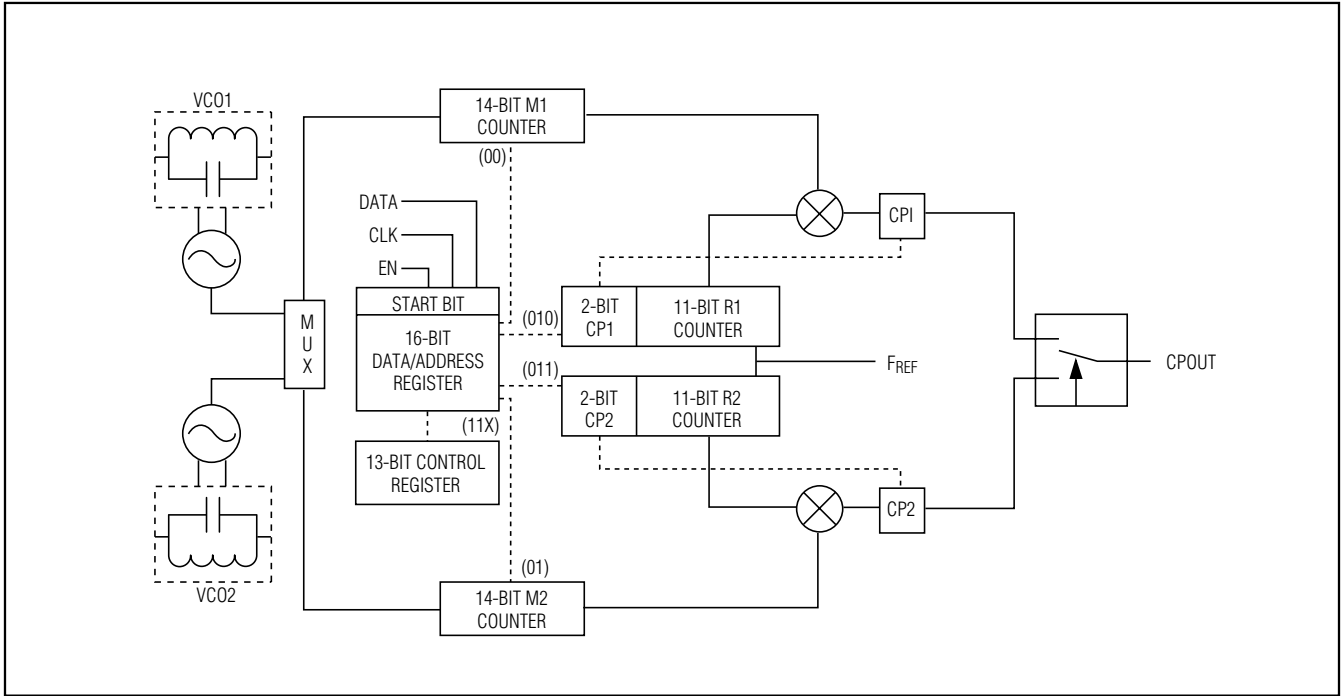


Figure 5. 3-Wire Control Block Diagram

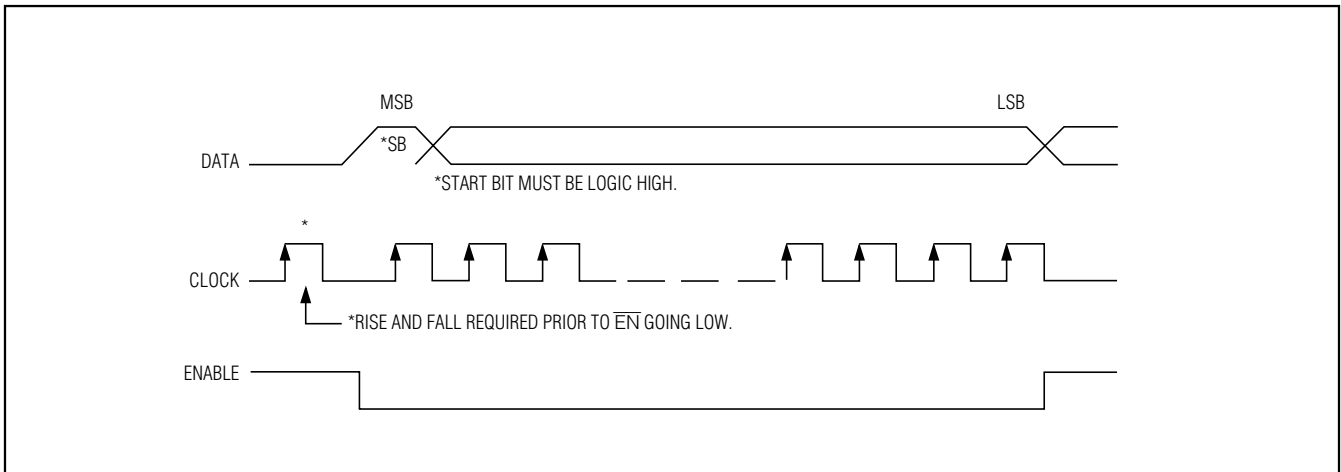


Figure 6. 3-Wire Interface Timing Diagram

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316

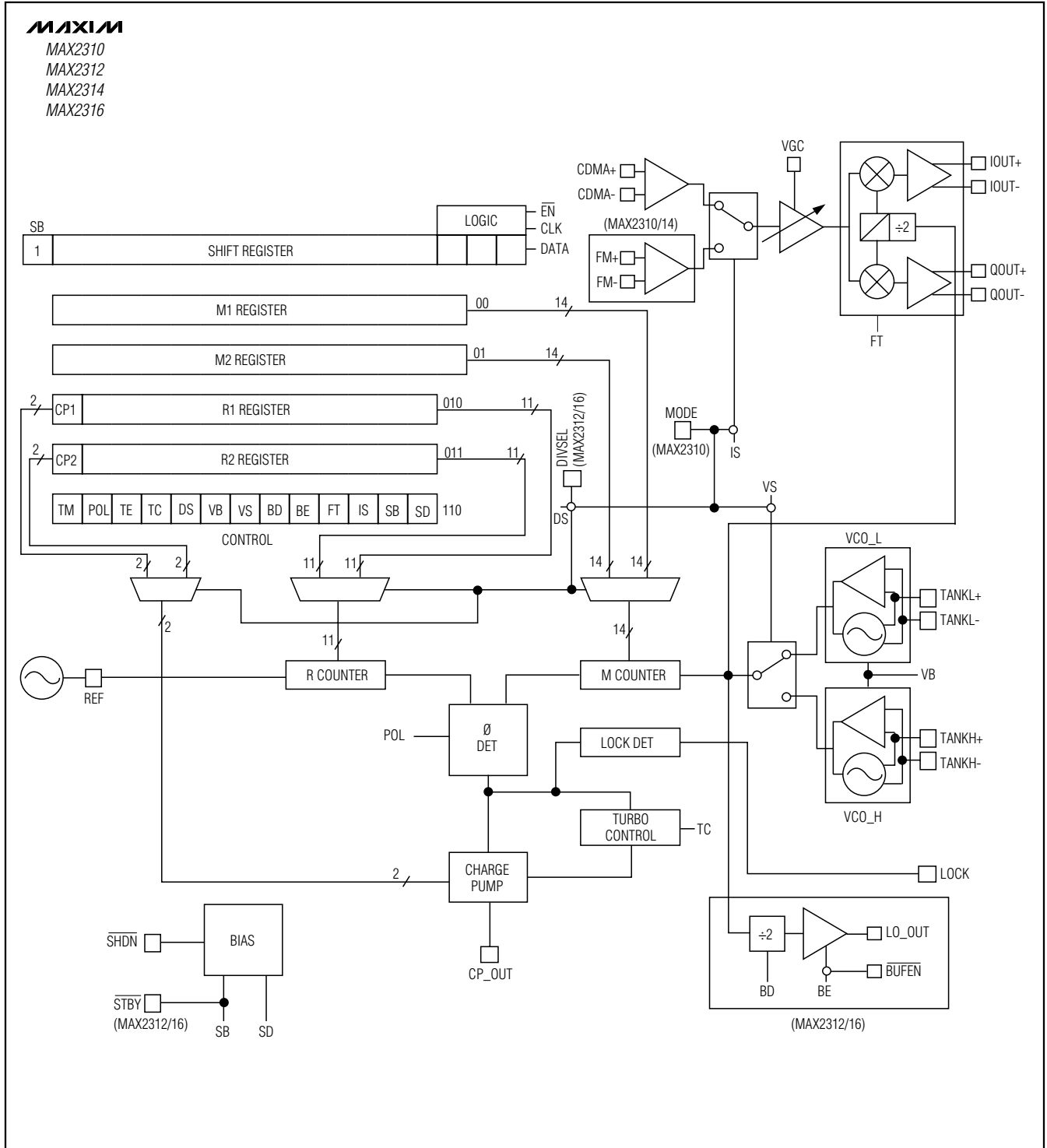


Figure 7. Functional Diagram

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Table 4. Control Register, Default State: 0B57h, Address: 110b

| BIT ID | BIT NAME | POWER-UP STATE | BIT LOCATION 0 = LSB | FUNCTION |
|--------|---------------------------|----------------|-------------------------|---|
| TM | TEST_MODE | 0 | 12 | Must be 0 for normal operation. |
| POL | CP_POL | 1 | 11 | Logic "1" causes the charge-pump output CP_OUT to source current when $f_{REF}/R > f_{VCO}/M$. This state is used when the VCO tune polarity is such that increasing voltage produces increasing frequency. Logic "0" causes CP_OUT to source current when $f_{VCO}/M > f_{REF}/R$. This state is used when increasing tune voltage causes the VCO frequency to decrease. |
| TE | TEST_ENABLE | 0 | 10 | Must be 0 for normal operation. |
| TC | TURBO_CHARGE | 1 | 9 | Logic "1" activates turbocharge mode, which provides rapid frequency acquisition in the PLL. Not available on MAX2316. |
| DS | DIV_SEL | 1 | 8 | Logic "1" selects M1/R1 divide ratios. Logic "0" selects M2/R2. |
| VB | VCO_BYP | 0 | 7 | Logic "1" bypasses the VCO inputs for external VCO operation. |
| VS | VCO_SEL | 1 | 6 | Logic "1" selects VCO_H. Logic "0" selects VCO_L. |
| BD | BUF_DIV | 0 | 5 | Logic "1" selects divide-by-2 on LOOUT port. Logic "0" bypasses divider. |
| BE | $\overline{\text{BUFEN}}$ | 1 | 4 | Logic "1" disables LOOUT. Logic "0" enables LOOUT. |
| FT | FM_TYPE | 0 | 3 | Active in FM mode. Logic "0" selects quadrature demodulator for FM mode. Logic "1" selects downconversion to I port. |
| IS | IN_SEL | 1 | 2 | Logic "0" selects FM input port. Logic "1" selects CDMA input. |
| SB | $\overline{\text{STBY}}$ | 1 | 1 | Logic "0" enables standby mode, which shuts down the VGA and demodulator stages, leaving the VCO locked and the registers active. |
| SD | $\overline{\text{SHDN}}$ | 1 | 0 | Logic "0" enables register-based shutdown. This mode shuts down everything except the M and R latches and the serial bus. |

Table 5. Register Defaults

| REGISTER | DEFAULT |
|----------|----------|
| M1 | 10519DEC |
| M2 | 4269DEC |
| R1 | 492DEC |
| R2 | 492DEC |
| CTRL | 0B57HEX |
| CP0 | 11 BIN |
| CP1 | 11 BIN |

Table 6. Charge-Pump Control Bits

| CP1 | CP0 | CHARGE-PUMP CURRENT AFTER ACQUISITION (μA) |
|-----|-----|---|
| 0 | 0 | 150 |
| 0 | 1 | 210 |
| 1 | 0 | 300 |
| 1 | 1 | 425 |

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

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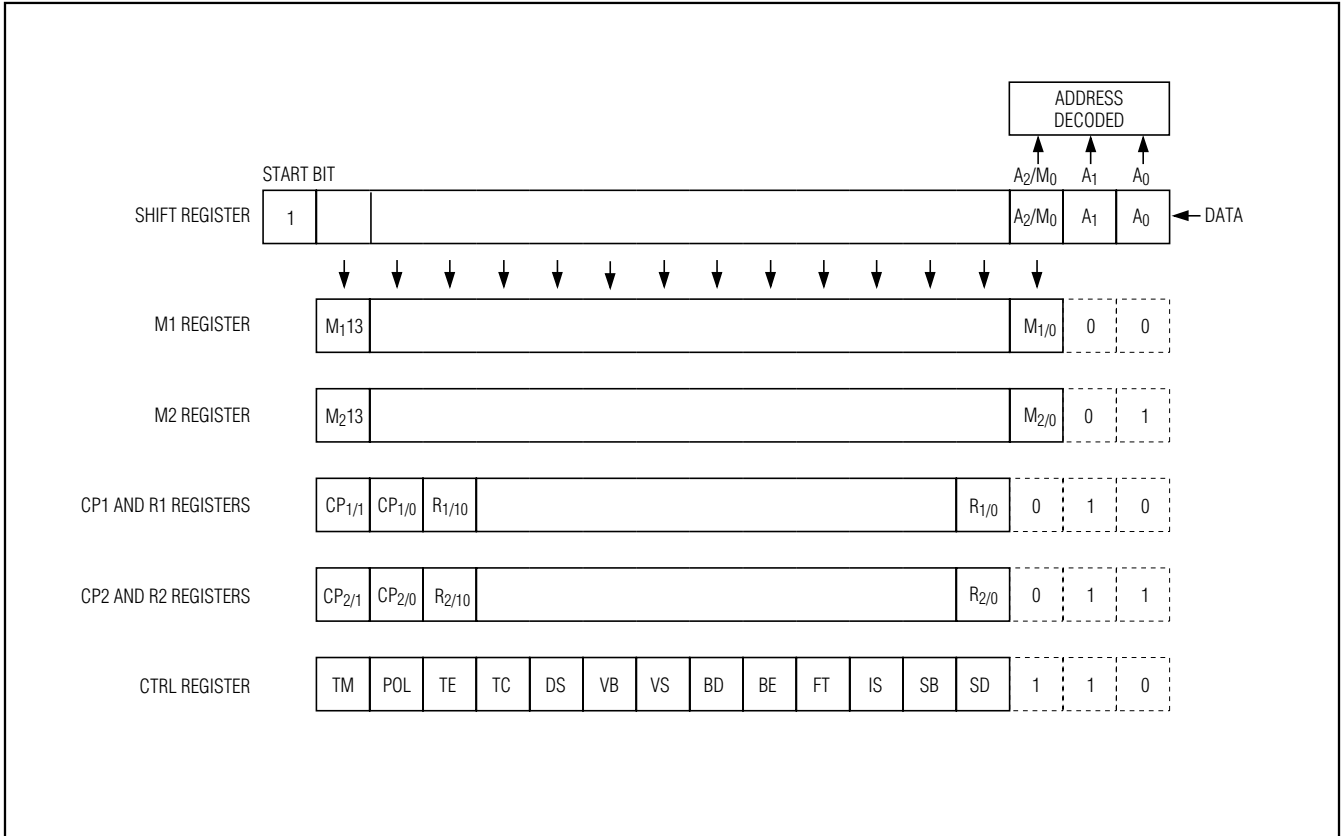
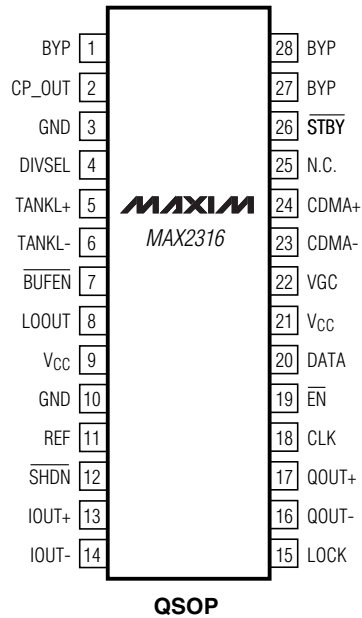
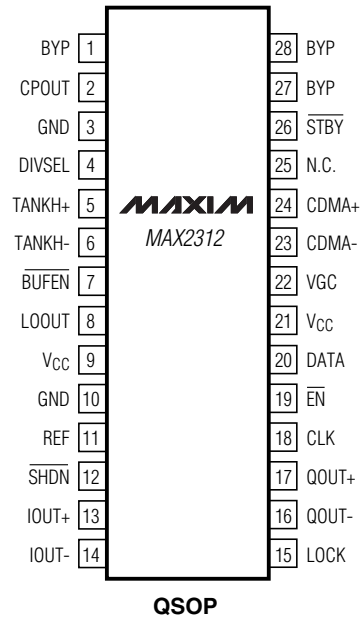
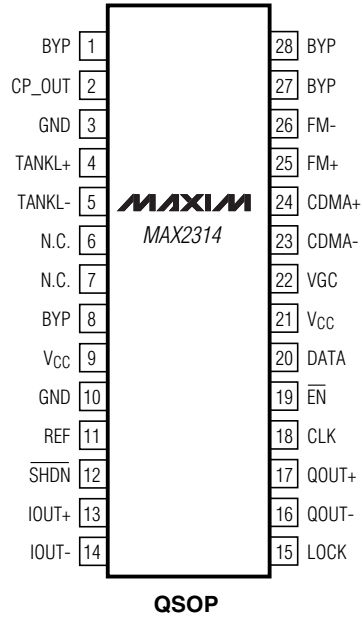
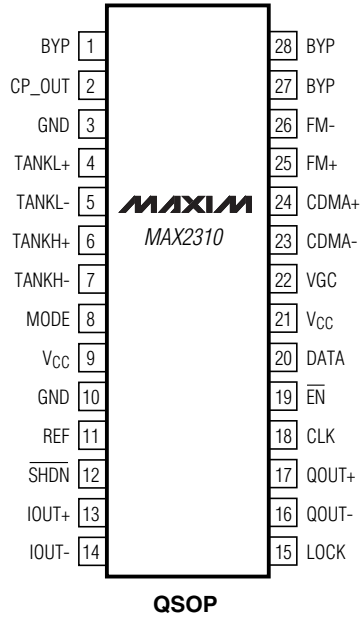


Figure 8. Programming Logic

CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Pin Configurations

TOP VIEW

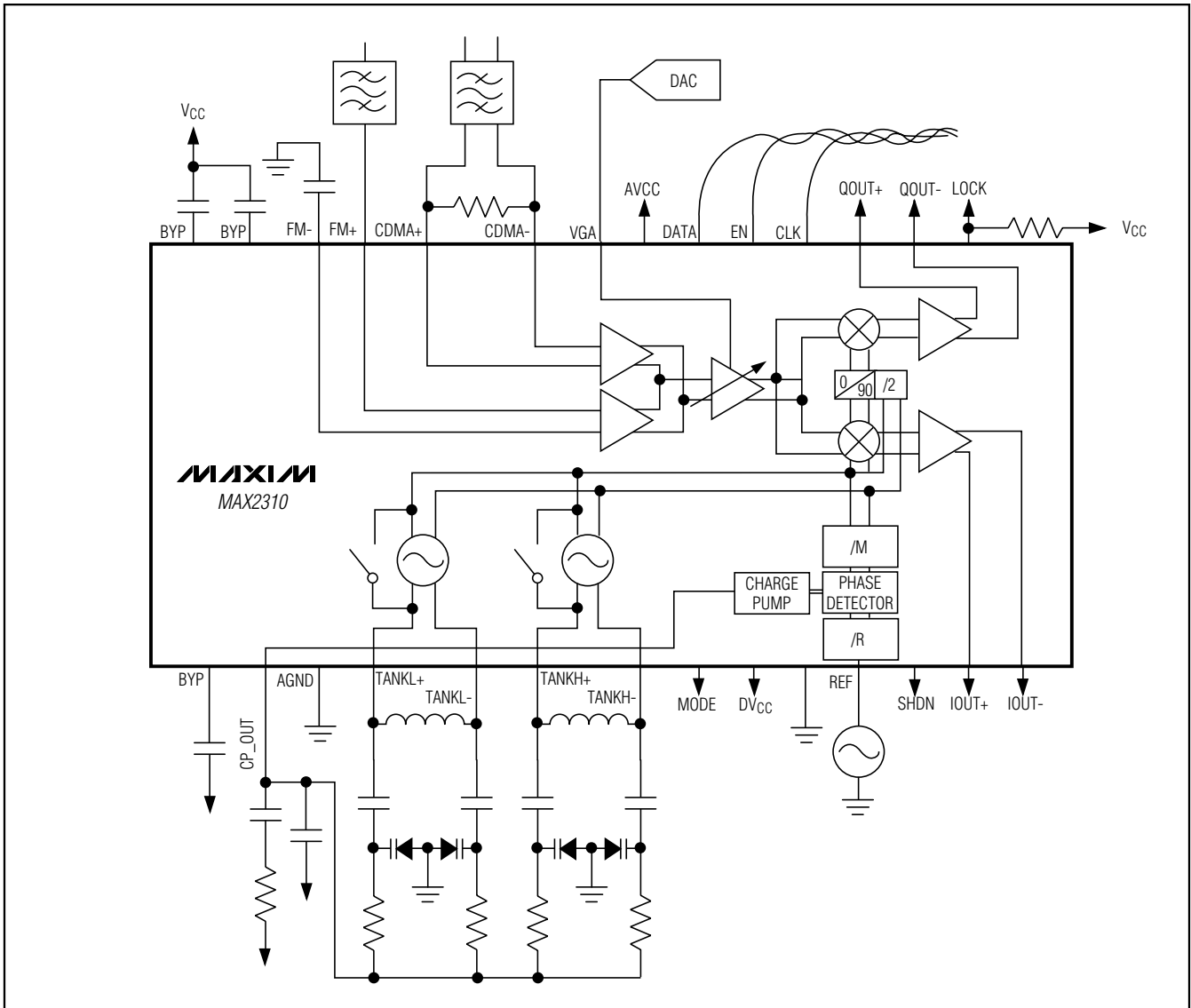


CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Chip Information

TRANSISTOR COUNT: 6422

Block Diagram

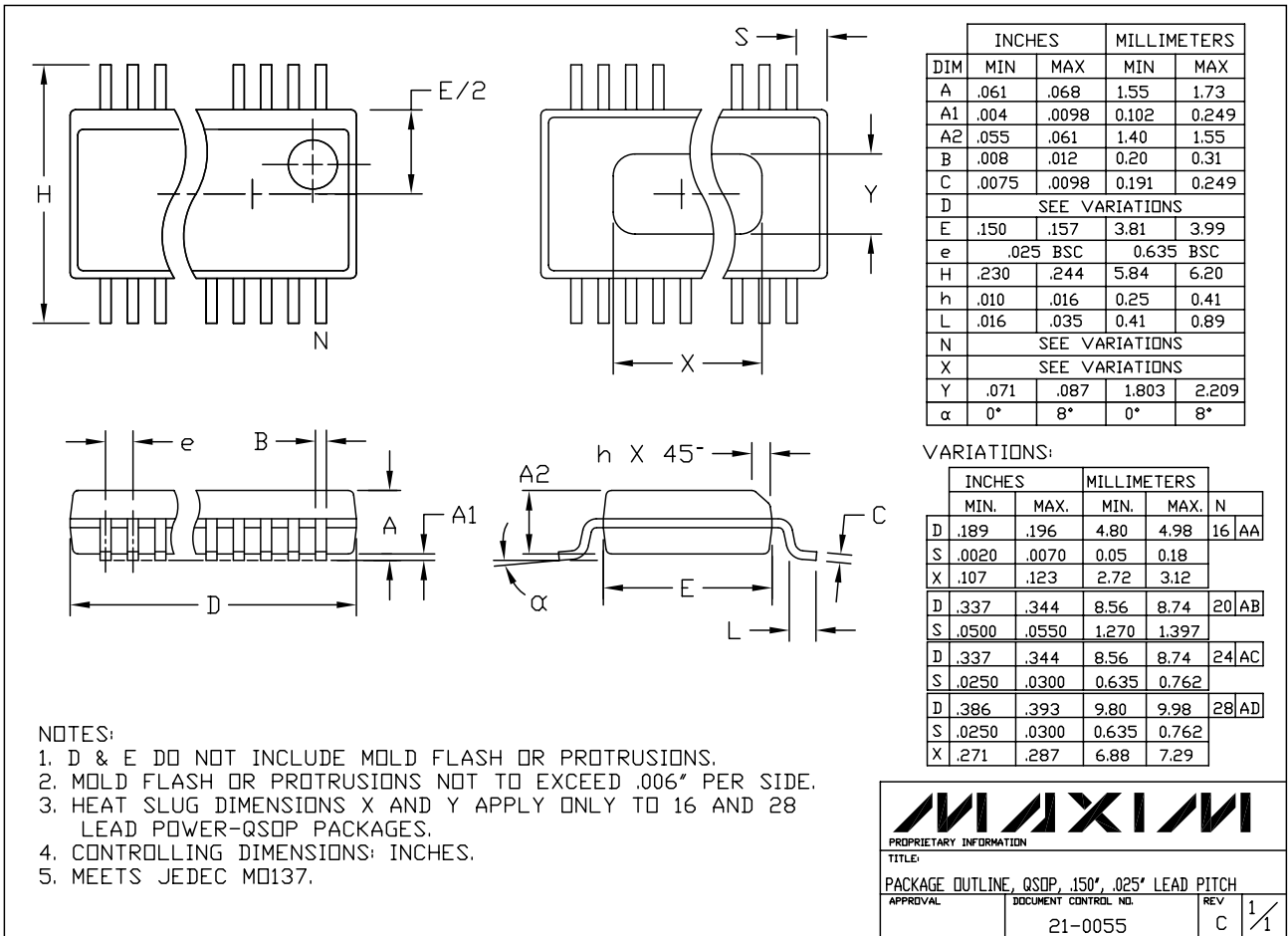


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CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



Revision History

Pages changed at Rev 2: 1, 4, 18, 22

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