

4Byte 4Mx32 SIMM

(4Mx16 base)

Revision 0.0

June 1999

Revision History

Version 0.0 (June 1999)

- The 4th. generation of 64Mb DRAM components are applied for this module.

DRAM MODULE

KMM5324004CSW/CSWG

KMM5324004CSW/CSWG EDO Mode

4M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5324004C is a 4Mx32bits Dynamic RAM high density memory module. The Samsung KMM5324004C consists of two CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5324004C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

| Speed | t _{RAC} | t _{CAC} | t _{RC} | t _{HPC} |
|-------|------------------|------------------|-----------------|------------------|
| -5 | 50ns | 13ns | 84ns | 20ns |
| -6 | 60ns | 15ns | 104ns | 25ns |

FEATURES

- Part Identification
 - KMM5324004CSW(4K cycles/64ms Ref, TSOP, Solder)
 - KMM5324004CSWG(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- $\overline{\text{CAS}}$ -before-RAS & Hidden Refresh capability
- $\overline{\text{RAS}}$ -only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

| Pin | Symbol | Pin | Symbol |
|-----|-----------------|-----|--------------------------|
| 1 | V _{ss} | 37 | NC |
| 2 | DQ0 | 38 | NC |
| 3 | DQ18 | 39 | $\overline{\text{Vss}}$ |
| 4 | DQ1 | 40 | $\overline{\text{CAS0}}$ |
| 5 | DQ19 | 41 | $\overline{\text{CAS2}}$ |
| 6 | DQ2 | 42 | $\overline{\text{CAS3}}$ |
| 7 | DQ20 | 43 | $\overline{\text{CAS1}}$ |
| 8 | DQ3 | 44 | RAS0 |
| 9 | DQ21 | 45 | NC |
| 10 | V _{cc} | 46 | NC |
| 11 | NC | 47 | W |
| 12 | A0 | 48 | NC |
| 13 | A1 | 49 | DQ9 |
| 14 | A2 | 50 | DQ27 |
| 15 | A3 | 51 | DQ10 |
| 16 | A4 | 52 | DQ28 |
| 17 | A5 | 53 | DQ11 |
| 18 | A6 | 54 | DQ29 |
| 19 | A10 | 55 | DQ12 |
| 20 | DQ4 | 56 | DQ30 |
| 21 | DQ22 | 57 | DQ13 |
| 22 | DQ5 | 58 | DQ31 |
| 23 | DQ23 | 59 | V _{cc} |
| 24 | DQ6 | 60 | DQ32 |
| 25 | DQ24 | 61 | DQ14 |
| 26 | DQ7 | 62 | DQ33 |
| 27 | DQ25 | 63 | DQ15 |
| 28 | A7 | 64 | DQ34 |
| 29 | A11 | 65 | DQ16 |
| 30 | V _{cc} | 66 | NC |
| 31 | A8 | 67 | PD1 |
| 32 | A9 | 68 | PD2 |
| 33 | NC | 69 | PD3 |
| 34 | RAS2 | 70 | PD4 |
| 35 | NC | 71 | NC |
| 36 | NC | 72 | V _{ss} |

PIN NAMES

| Pin Name | Function |
|---|-----------------------|
| A0 - A11 | Address Inputs |
| DQ0-7, DQ9-16 DQ18-25, DQ27-34 | Data In/Out |
| $\overline{\text{W}}$ | Read/Write Enable |
| $\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$ | Row Address Strobe |
| $\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$ | Column Address Strobe |
| PD1 - PD4 | Presence Detect |
| V _{cc} | Power(+5V) |
| V _{ss} | Ground |
| NC | No Connection |

PRESENCE DETECT PINS (Optional)

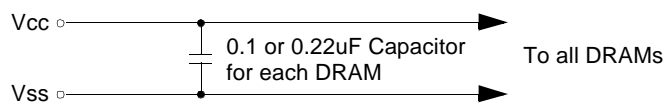
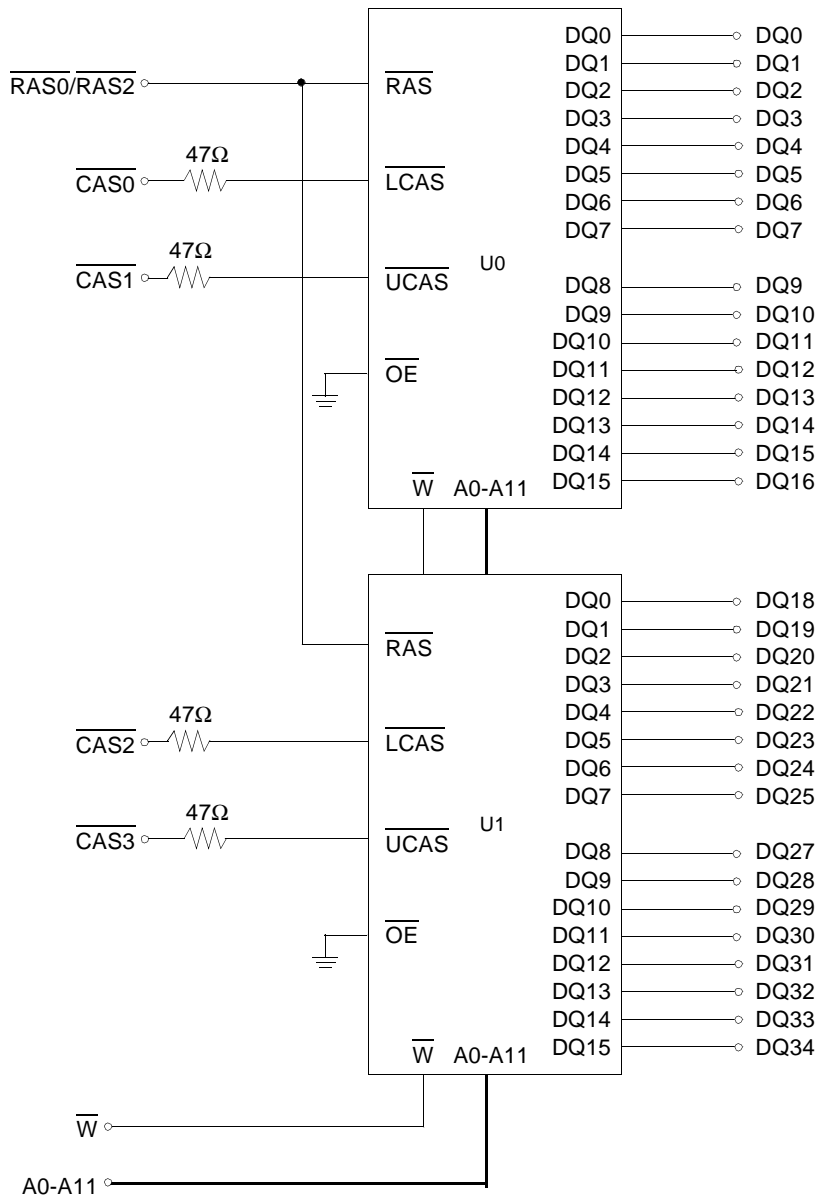
| Pin | 50NS | 60NS |
|-----|-----------------|-----------------|
| PD1 | V _{ss} | V _{ss} |
| PD2 | NC | NC |
| PD3 | V _{ss} | NC |
| PD4 | V _{ss} | NC |

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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---------------------------------------|------------------------------------|-------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | V _{CC} | -1 to +7.0 | V |
| Storage Temperature | T _{stg} | -55 to +125 | °C |
| Power Dissipation | P _d | 2 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to VSS, TA = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------|-----|-------------------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | V _{CC} ^{*1} | V |
| Input Low Voltage | V _{IL} | -1.0 ^{*2} | - | 0.8 | V |

*1 : V_{CC}+2.0V at pulse width ≤ 20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width ≤ 20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | KMM5324004CSW/CSWG | | Unit |
|-------------------|------------|--------------------|-----|------|
| | | Min | Max | |
| I _{CC1} | -5 | - | 240 | mA |
| | -6 | - | 220 | mA |
| I _{CC2} | Don't care | - | 4 | mA |
| I _{CC3} | -5 | - | 240 | mA |
| | -6 | - | 220 | mA |
| I _{CC4} | -5 | - | 220 | mA |
| | -6 | - | 200 | mA |
| I _{CC5} | Don't care | - | 2 | mA |
| I _{CC6} | -5 | - | 240 | mA |
| | -6 | - | 220 | mA |
| I _{I(L)} | Don't care | -10 | 10 | µA |
| I _{O(L)} | | -5 | 5 | µA |
| V _{OH} | Don't care | 2.4 | - | V |
| V _{OL} | | - | 0.4 | V |

I_{CC1} : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$)

I_{CC3} : $\overline{\text{RAS}}$ Only Refresh Current * ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ cycling @trc=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$)

I_{CC6} : $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0 \leq \text{V}_{\text{IN}} \leq \text{V}_{\text{CC}}+0.5\text{V}$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0\text{V} \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{CC}}$)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{\text{RAS}}=\text{V}_{\text{IL}}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

DRAM MODULE

KMM5324004CSW/CSWG

CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|---|--------|-----|-----|------|
| Input capacitance[A0-A11] | CIN1 | - | 20 | pF |
| Input capacitance[W] | CIN2 | - | 24 | pF |
| Input capacitance[RAS0/RAS2] | CIN3 | - | 24 | pF |
| Input capacitance[CAS0 - CAS3] | CIN4 | - | 17 | pF |
| Input/Output capacitance[DQ0-7, 9-16, 18-25, 27-34] | CDQ | - | 17 | pF |

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : VIH/VIIL=2.6/0.8V, VOH/VOIL=2.0/0.8V, output loading CL=100pF

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|---|--------|-----|-----|-----|-----|------|--------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 84 | | 104 | | ns | |
| Access time from RAS | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from CAS | tCAC | | 13 | | 15 | ns | 3,4,5 |
| Access time from column address | tAA | | 25 | | 30 | ns | 3,10 |
| CAS to output in Low-Z | tCLZ | 3 | | 3 | | ns | 3 |
| Output buffer turn-off delay from CAS | tCEZ | 3 | 13 | 3 | 13 | ns | 6,12 |
| Transition time(rise and fall) | tT | 1 | 50 | 1 | 50 | ns | 2 |
| RAS precharge time | tRP | 30 | | 40 | | ns | |
| RAS pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| RAS hold time | tRSH | 13 | | 15 | | ns | |
| CAS hold time | tCSH | 38 | | 45 | | ns | |
| CAS pulse width | tCAS | 8 | 10K | 10 | 10K | ns | 4 |
| RAS to CAS delay time | tRCD | 20 | 37 | 20 | 45 | ns | 9 |
| RAS to column address delay time | tRAD | 15 | 25 | 15 | 30 | ns | |
| CAS to RAS precharge time | tCRP | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 8 | | 10 | | ns | |
| Column address to RAS lead time | tRAL | 25 | | 30 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referenced to CAS | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to RAS | tRRH | 0 | | 0 | | ns | 8 |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| Write command hold time | tWCH | 10 | | 10 | | ns | |
| Write command pulse width | tWP | 10 | | 10 | | ns | |
| Write command to RAS lead time | tRWL | 13 | | 15 | | ns | |
| Write command to CAS lead time | tCWL | 8 | | 10 | | ns | |
| Data set-up time | tDS | 0 | | 0 | | ns | 9 |
| Data hold time | tDH | 8 | | 10 | | ns | 9 |
| Refresh period | tREF | | 64 | | 64 | ms | |
| CAS setup time (CAS-before-RAS refresh) | tCSR | 5 | | 5 | | ns | |
| CAS hold time (CAS-before-RAS refresh) | tCHR | 10 | | 10 | | ns | |
| RAS to CAS precharge time | tRPC | 5 | | 5 | | ns | |
| Access time from CAS precharge | tCPA | | 28 | | 35 | ns | 3 |



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AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%. See notes 1,2.)

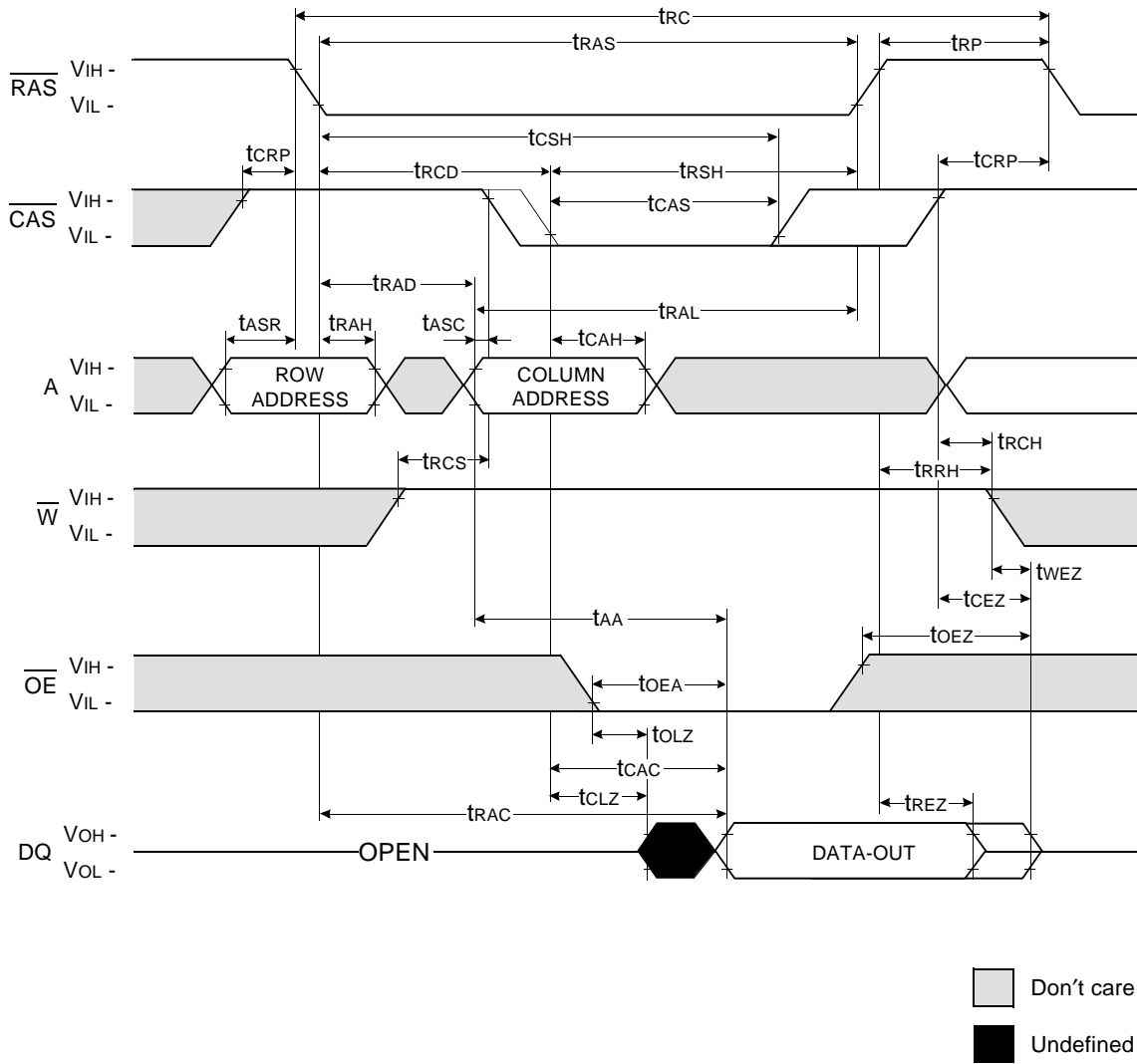
Test condition : V_{ih}/V_{il} = 2.6/0.8V, V_{oh}/V_{ol} = 2.0/0.8V, output loading CL = 100pF

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|---|--------|-----|------|-----|------|------|------|
| | | Min | Max | Min | Max | | |
| Hyper page mode cycle time | tHPC | 20 | | 25 | | ns | 11 |
| CAS precharge time (Hyper page cycle) | tCP | 8 | | 10 | | ns | |
| RAS pulse width (Hyper page cycle) | tRASP | 50 | 200K | 60 | 200K | ns | |
| RAS hold time from $\overline{\text{CAS}}$ precharge | tRHCP | 30 | | 35 | | ns | |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time (C-B-R refresh) | tWRP | 10 | | 10 | | ns | |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time (C-B-R refresh) | tWRH | 10 | | 10 | | ns | |
| Output data hold time | tDOH | 5 | | 5 | | ns | |
| Output buffer turn off delay from $\overline{\text{RAS}}$ | tREZ | 3 | 13 | 3 | 15 | ns | 6,12 |
| Output buffer turn off delay from $\overline{\text{W}}$ | tWEZ | 3 | 13 | 3 | 15 | ns | 6 |
| $\overline{\text{W}}$ to data delay | tWED | 15 | | 15 | | ns | |
| $\overline{\text{W}}$ pulse width | tWPE | 5 | | 5 | | ns | |

NOTES

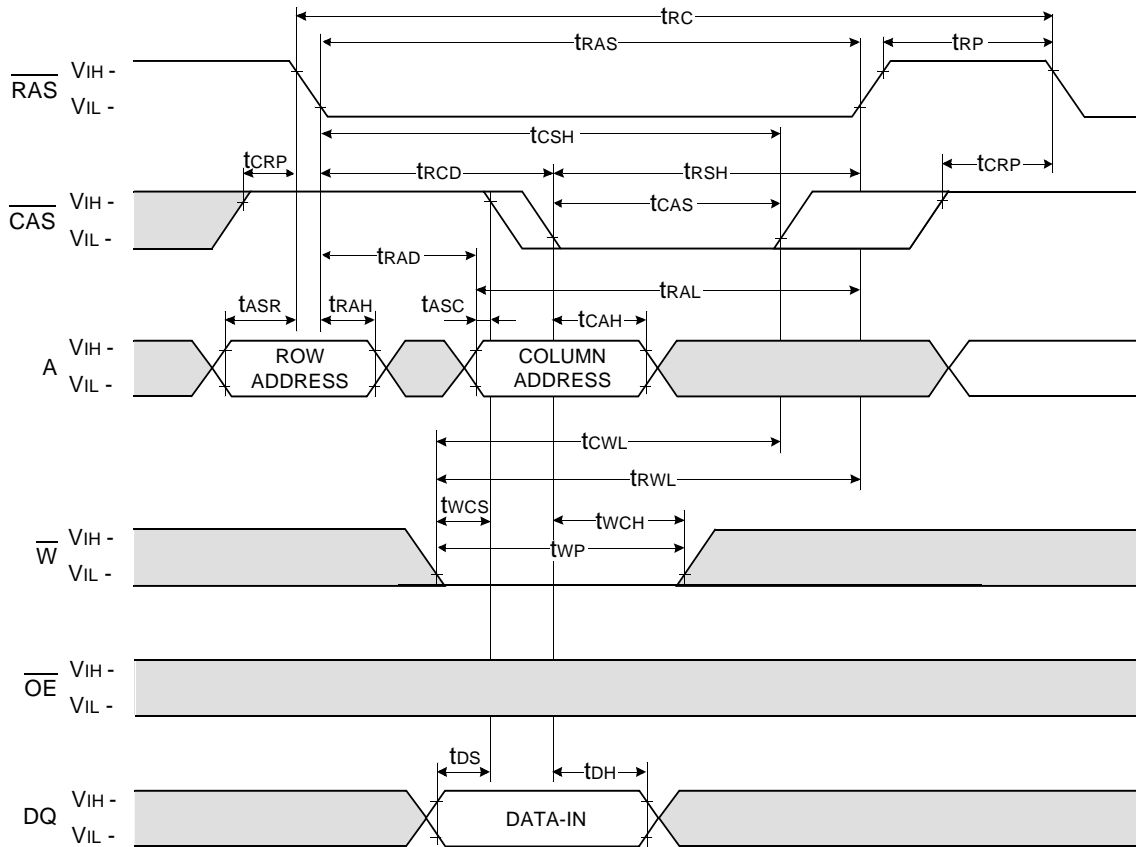
- An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
- Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RCD} ≥ t_{RCD}(max).
- This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.
- t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
- Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.
- t_{ASC} ≥ 6ns, Assume t_T = 2.0ns.
- If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

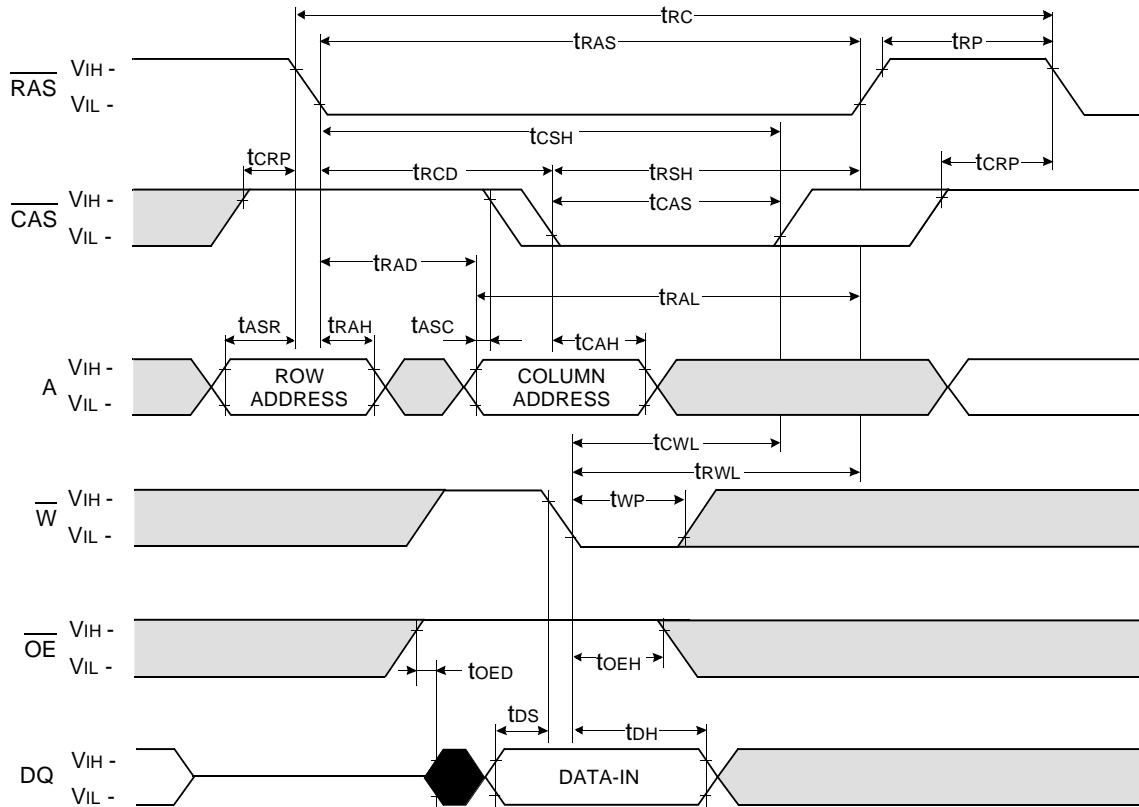
NOTE : DOUT = OPEN



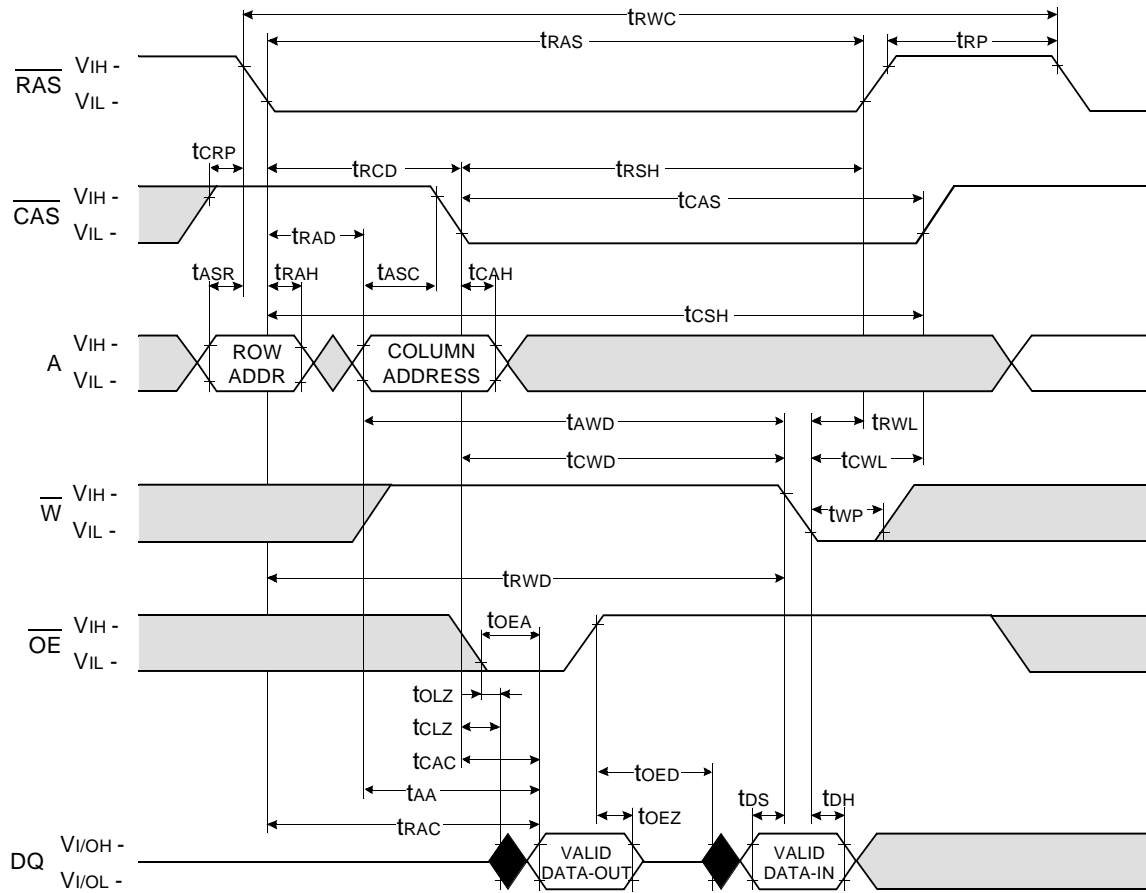
Don't care
 Undefined

WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



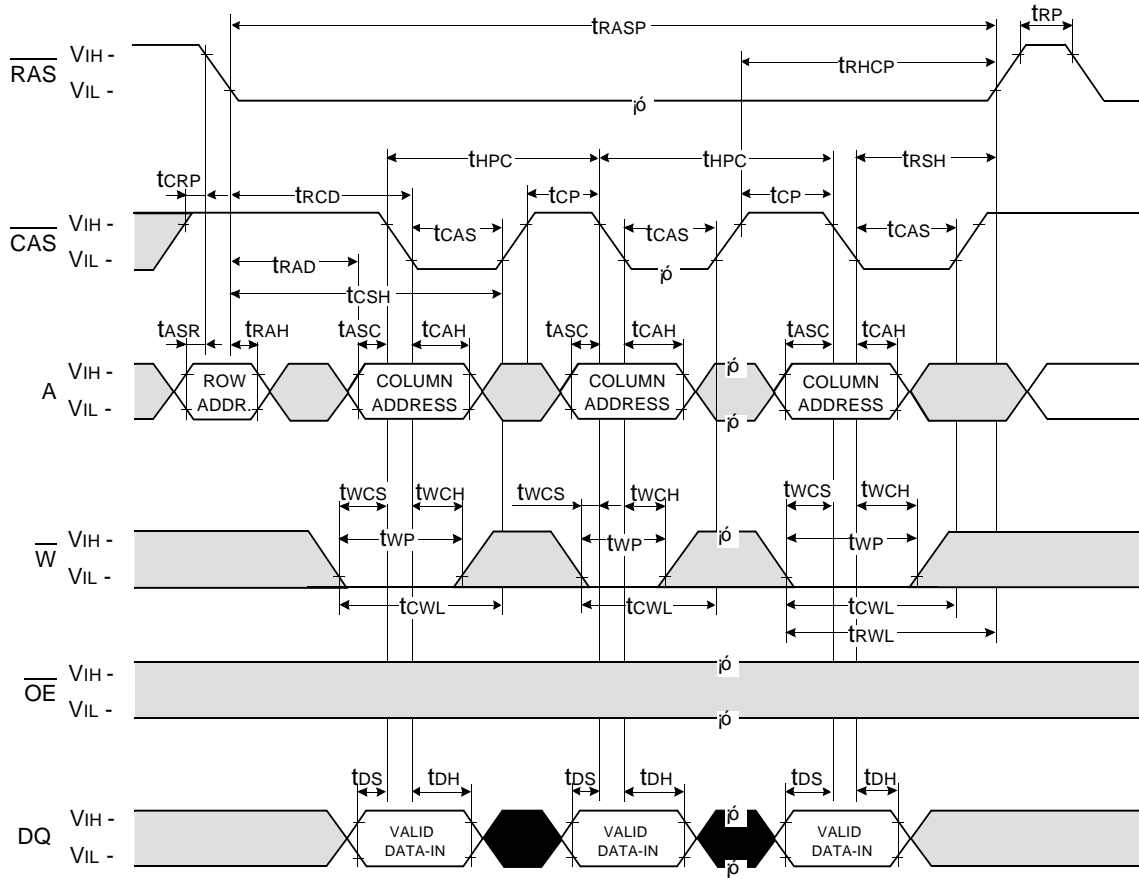
READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

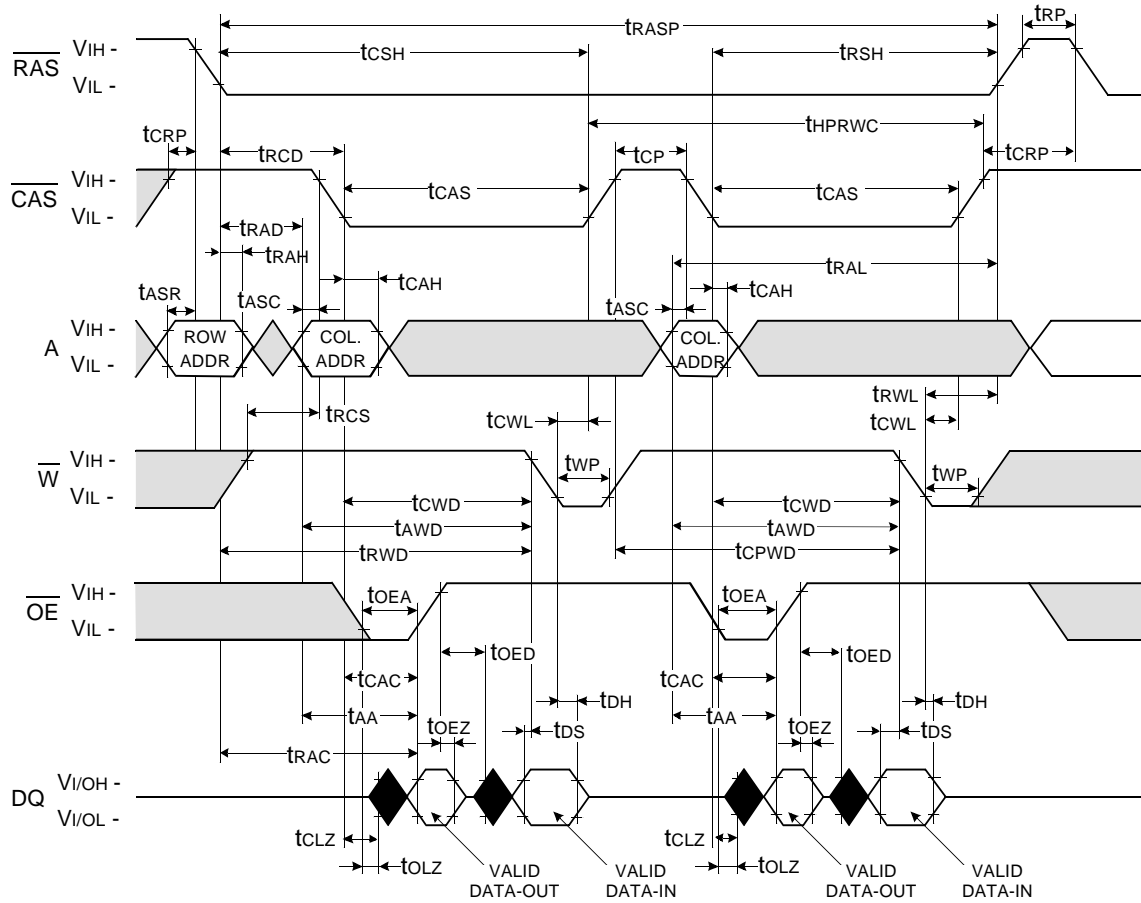
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

HYPER PAGE READ-MODIFY-WRITE CYCLE

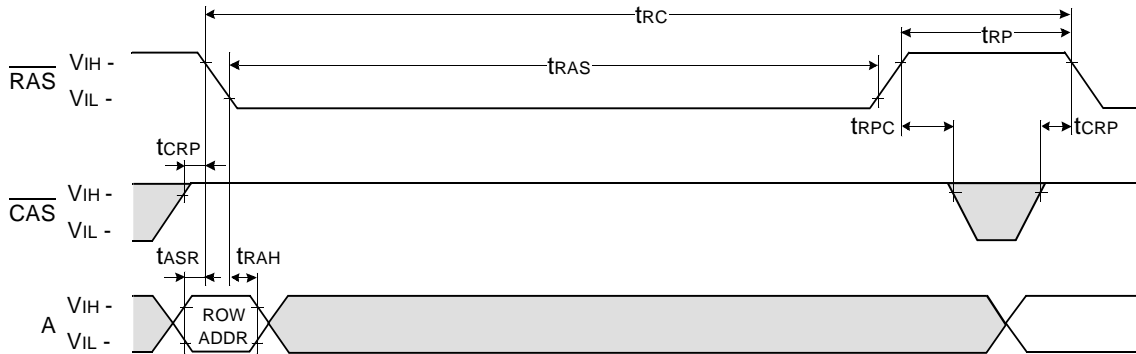


Don't care
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

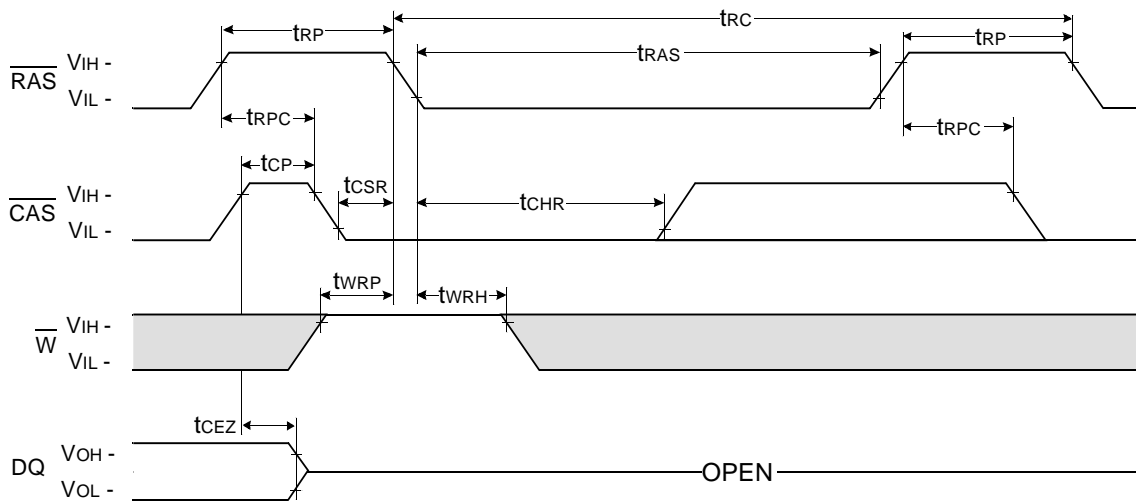
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

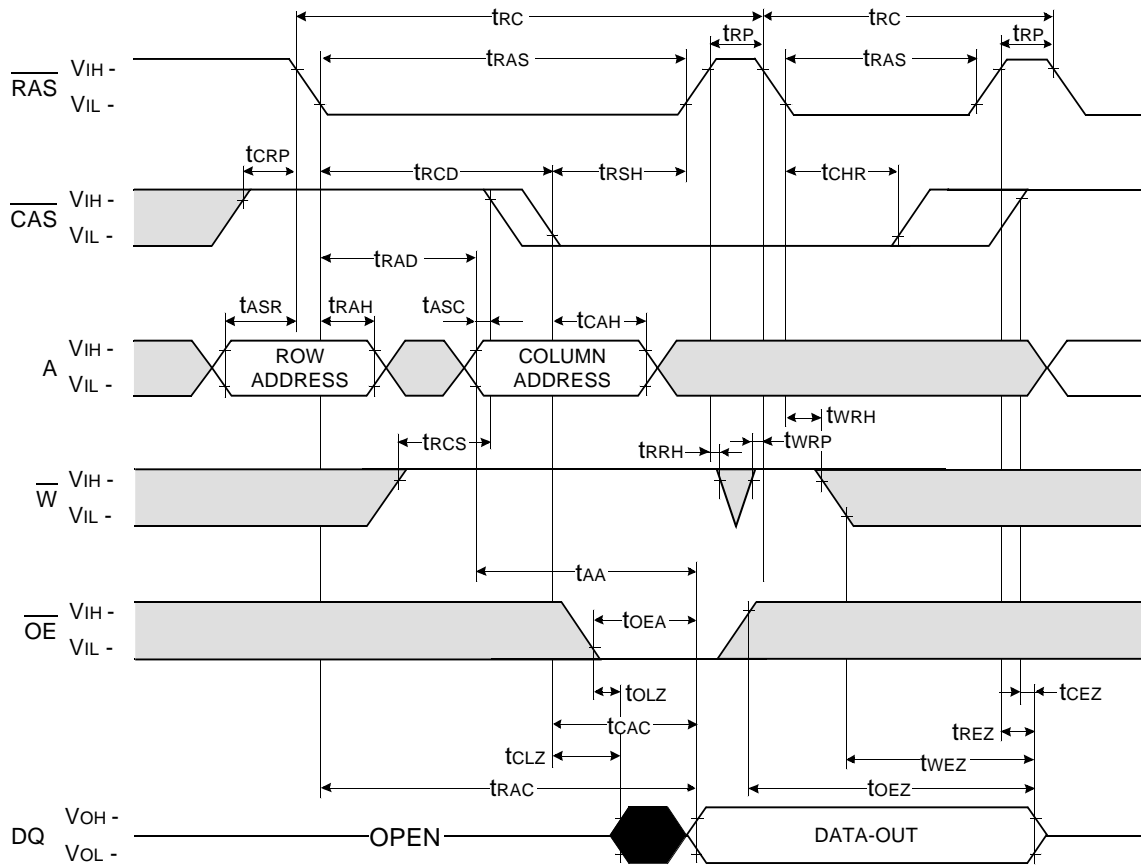
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

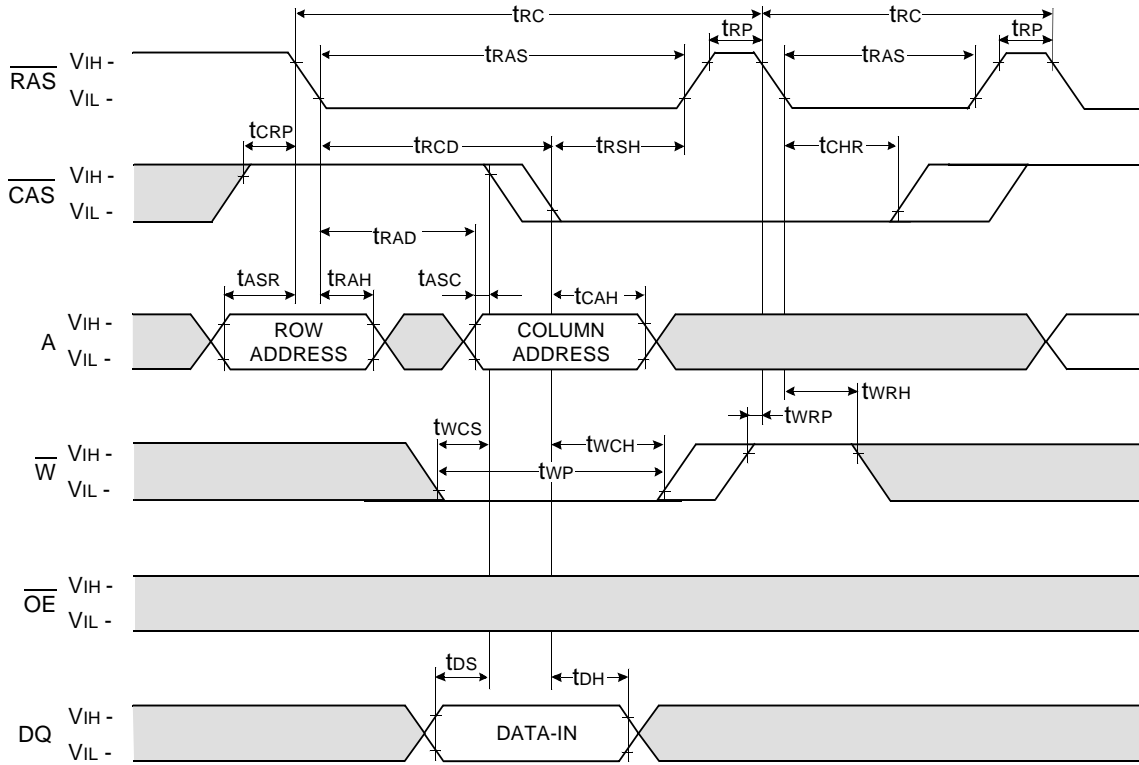
HIDDEN REFRESH CYCLE (READ)



Don't care
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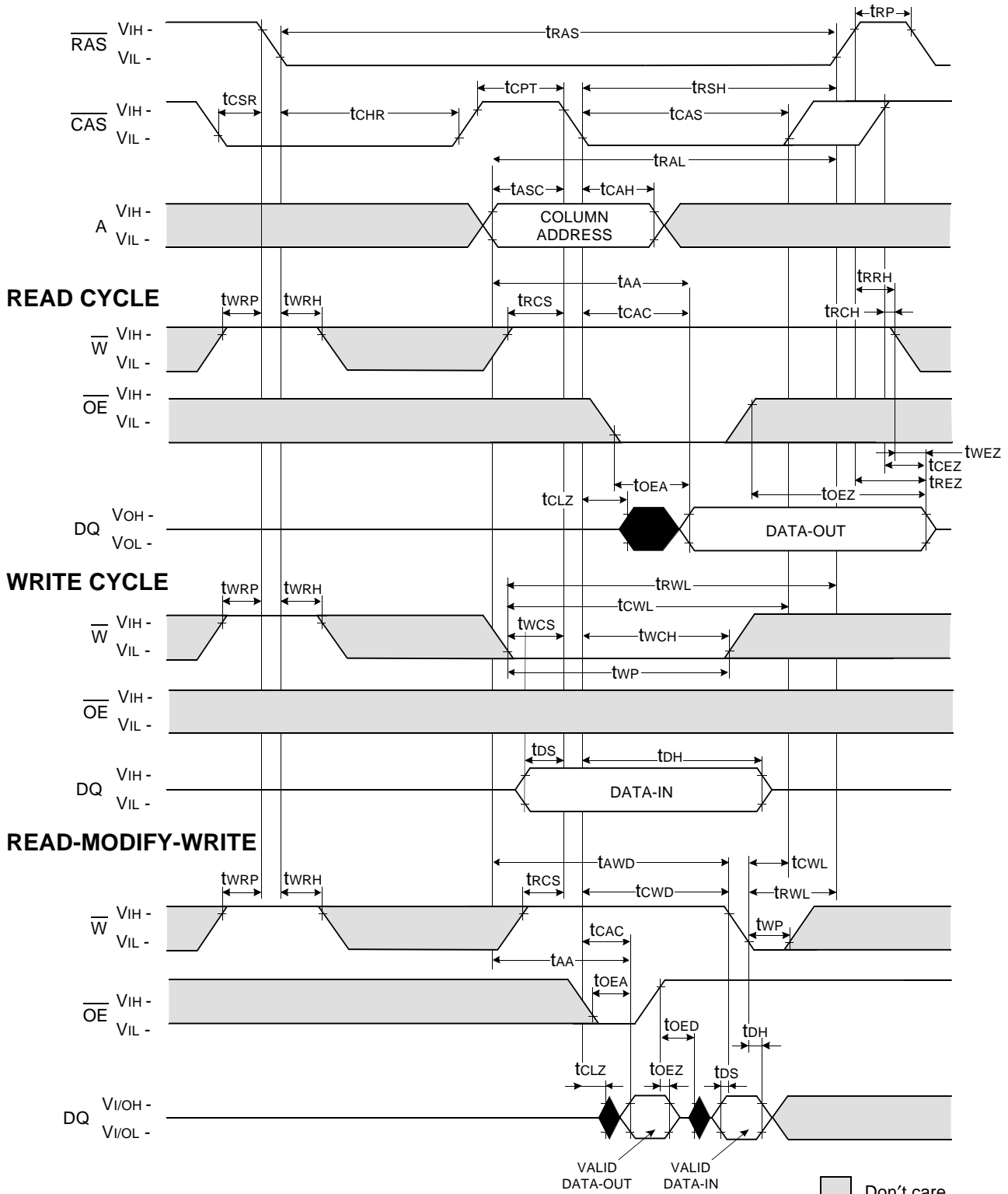
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

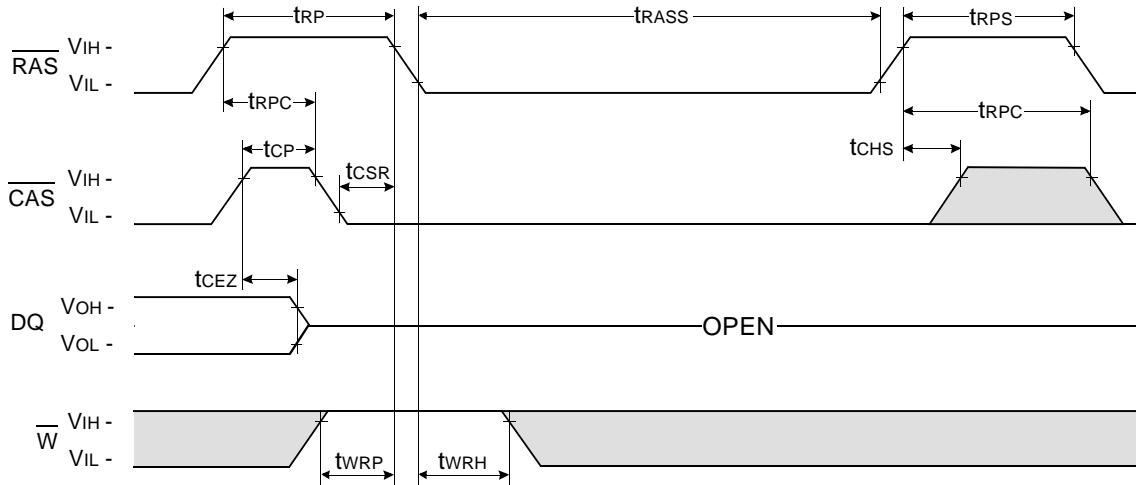
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

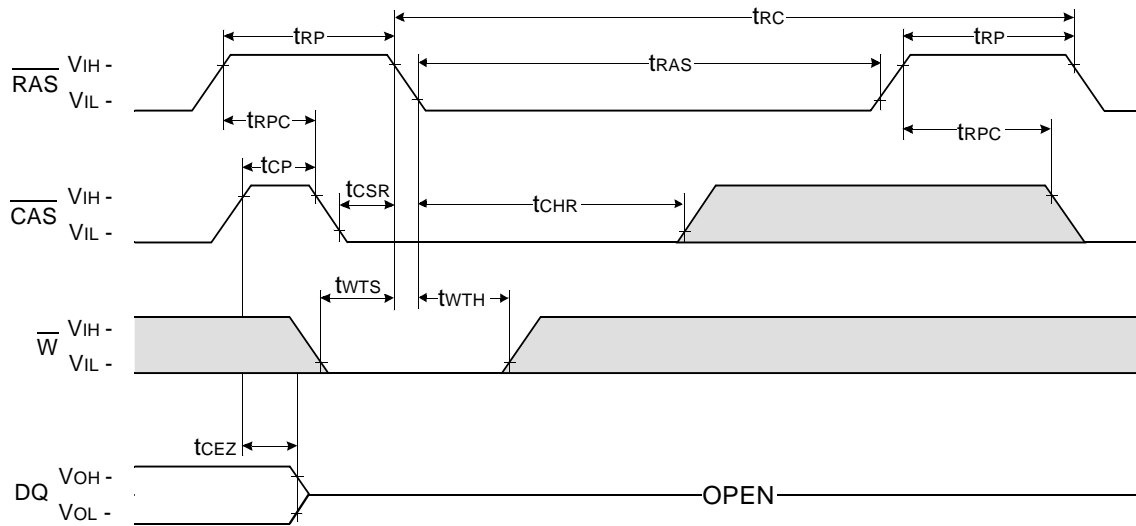
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



□ Don't care

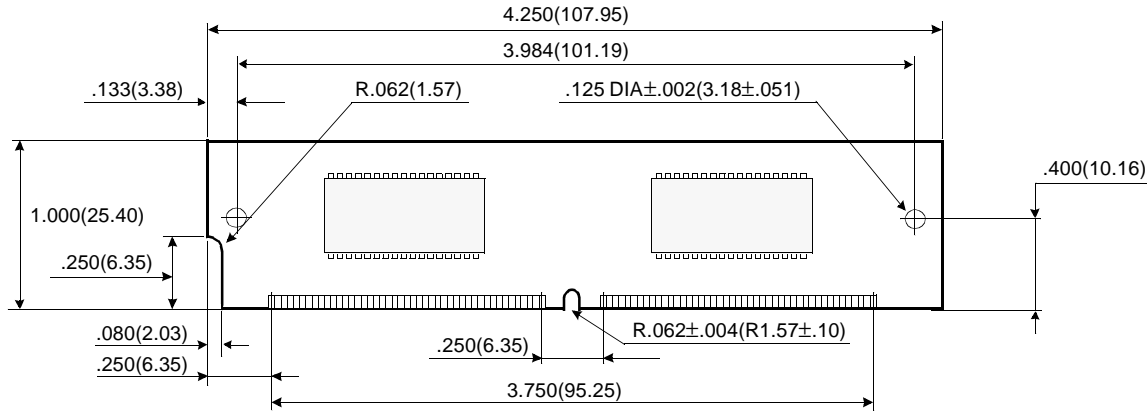
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DRAM MODULE

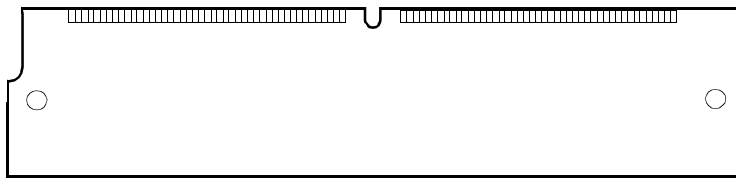
KMM5324004CSW/CSWG

PACKAGE DIMENSIONS

Units : Inches (millimeters)

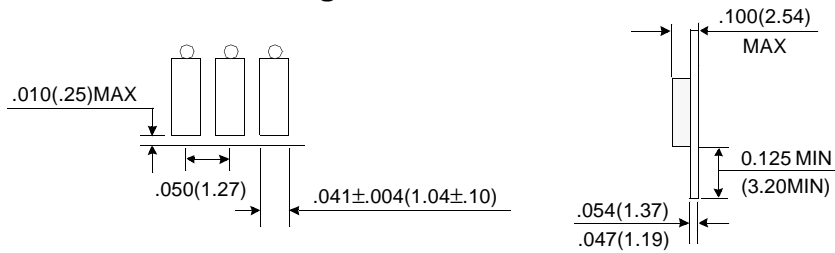


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII

DRAM Part No. : KMM5324004CSW/CSWG -- KM416C4104CS (400 mil)