8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH PARALLEL I/O

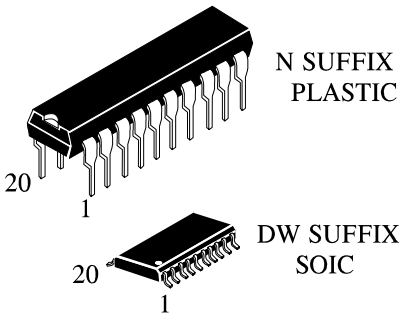
High-Performance Silicon-Gate CMOS

The IN74HC299 is identical in pinout to the LS/ALS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The IN74HC299features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S_1 and S_2, high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other inputs.

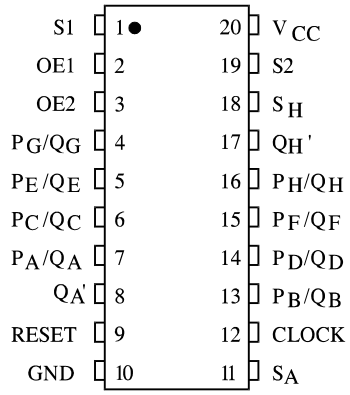
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices



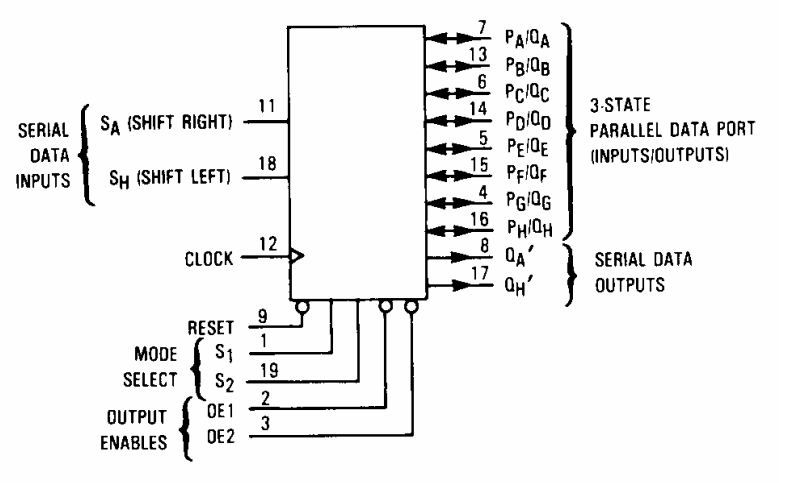
ORDERING INFORMATION

IN74HC299N Plastic
IN74HC299DW SOIC
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA (P/Q) $\|I_{OUT}\| \leq 7.8$ mA (P/Q)	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA (Q') $\|I_{OUT}\| \leq 5.2$ mA (Q')	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IL} or V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA (P/Q) $\|I_{OUT}\| \leq 7.8$ mA (P/Q)	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA (Q') $\|I_{OUT}\| \leq 5.2$ mA (Q')	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current (Q_A thru Q_H)	Output in High-Impedance State V_{IN}= V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	8.0	80	160	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125° C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q_A' or Q_H' (Figures 1 and 5)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q_A thru Q_H (Figures 1 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q_A' or Q_H' (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q_A thru Q_H (Figures 2 and 5)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay , OE1, OE2, S1, or S2 to Q_A thru Q_H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , OE1, OE2, S1, or S2 to Q_A thru Q_H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A thru Q_H (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A' thru Q_H' (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance)	-	10	10	10	pF
C_{OUT}	Maximum Three-State I/O Capacitance (I/O in High-Impedance State), Q_A thru Q_H	-	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Package), Output Enable Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 240	pF

TIMING REQUIREMENTS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Data Inputs S_A, S_H, P_A thru P_H to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_h	Minimum Hold Time, Clock to Data Inputs, S_A, S_H, P_A thru P_H (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

FUNCTION TABLE

Inputs									Response									
Mode	Reset	Mode Select		Output Enables		Clock	Serial Inputs		P_A/Q_A	P_B/Q_B	P_C/Q_C	P_D/Q_D	P_E/Q_E	P_F/Q_F	P_G/Q_G	P_H/Q_H	Q_A'	Q_H'
		S_2	S_1	OE1↑	OE2↑		D_A	D_H										
Reset	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	Q_A through Q_H=Z								L	L
Shift Right	H	L	H	H	X	⎍	D	X	Shift Right: Q_A through Q_H=Z; $D_A \rightarrow F_A$; $F_A \rightarrow F_B$; etc								D	Q_G
	H	L	H	X	H	⎍	D	X	Shift Right: Q_A through Q_H=Z; $D_A \rightarrow F_A$; $F_A \rightarrow F_B$; etc								D	Q_G
	H	L	H	L	L	⎍	D	X	Shift Right: $D_A \rightarrow F_A = Q_A$; $F_A \rightarrow F_B = Q_B$; etc								D	Q_G
Shift Left	H	H	L	H	X	⎍	X	D	Shift Left: Q_A through Q_H=Z; $D_H \rightarrow F_H$; $F_H \rightarrow F_G$; etc								Q_B	D
	H	H	L	X	H	⎍	X	D	Shift Left: Q_A through Q_H=Z; $D_H \rightarrow F_H$; $F_H \rightarrow F_G$; etc								Q_B	D
	H	H	L	L	L	⎍	X	D	Shift Left: $D_H \rightarrow F_H = Q_H$; $F_H \rightarrow F_G = Q_G$; etc								Q_B	D
Parallel Load	H	H	H	X	X	⎍	X	X	Parallel Load: $P_N \rightarrow F_N$								P_A	P_H
Hold	H	L	L	H	X	X	X	X	Hold: Q_A through Q_H=Z; F_N=F_N								P_A	P_H
	H	L	L	X	H	X	X	X	Hold: Q_A through Q_H=Z; F_N=F_N								P_A	P_H
	H	L	L	L	L	X	X	X	Hold: $Q_N = Q_H$								P_A	P_H

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

↑ When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

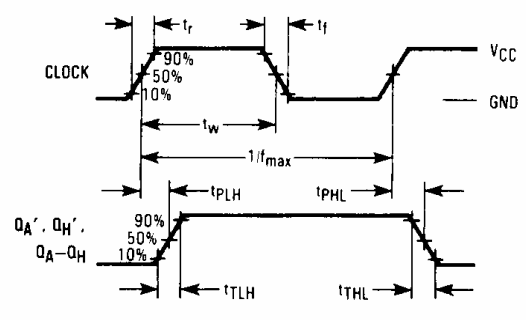


Figure 1. Switching Waveforms

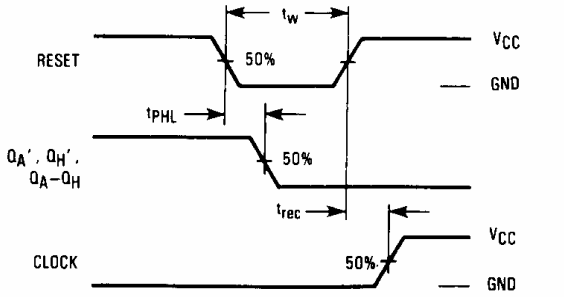


Figure 2. Switching Waveforms

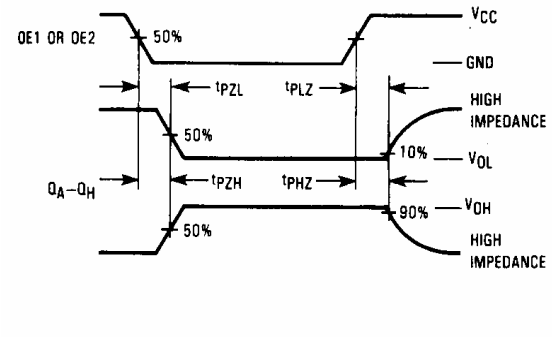


Figure 3a. Switching Waveforms

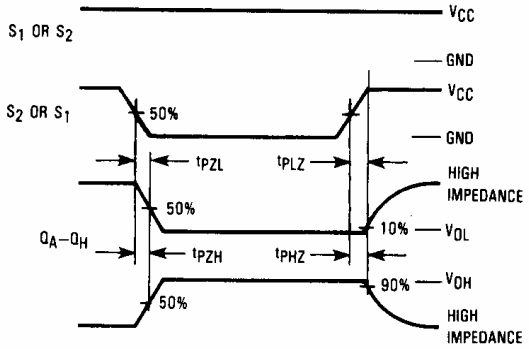


Figure 3b. Switching Waveforms

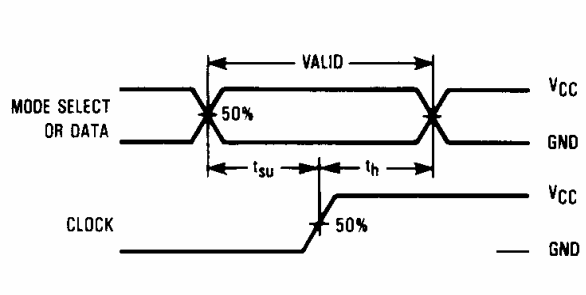
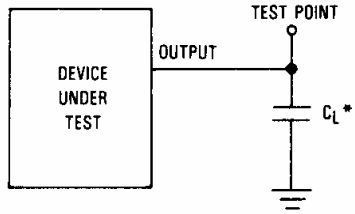
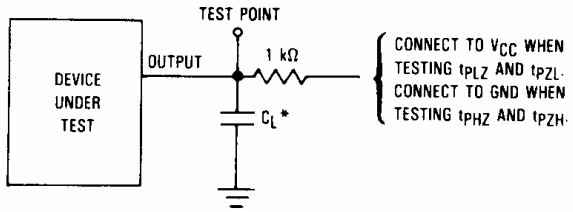


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

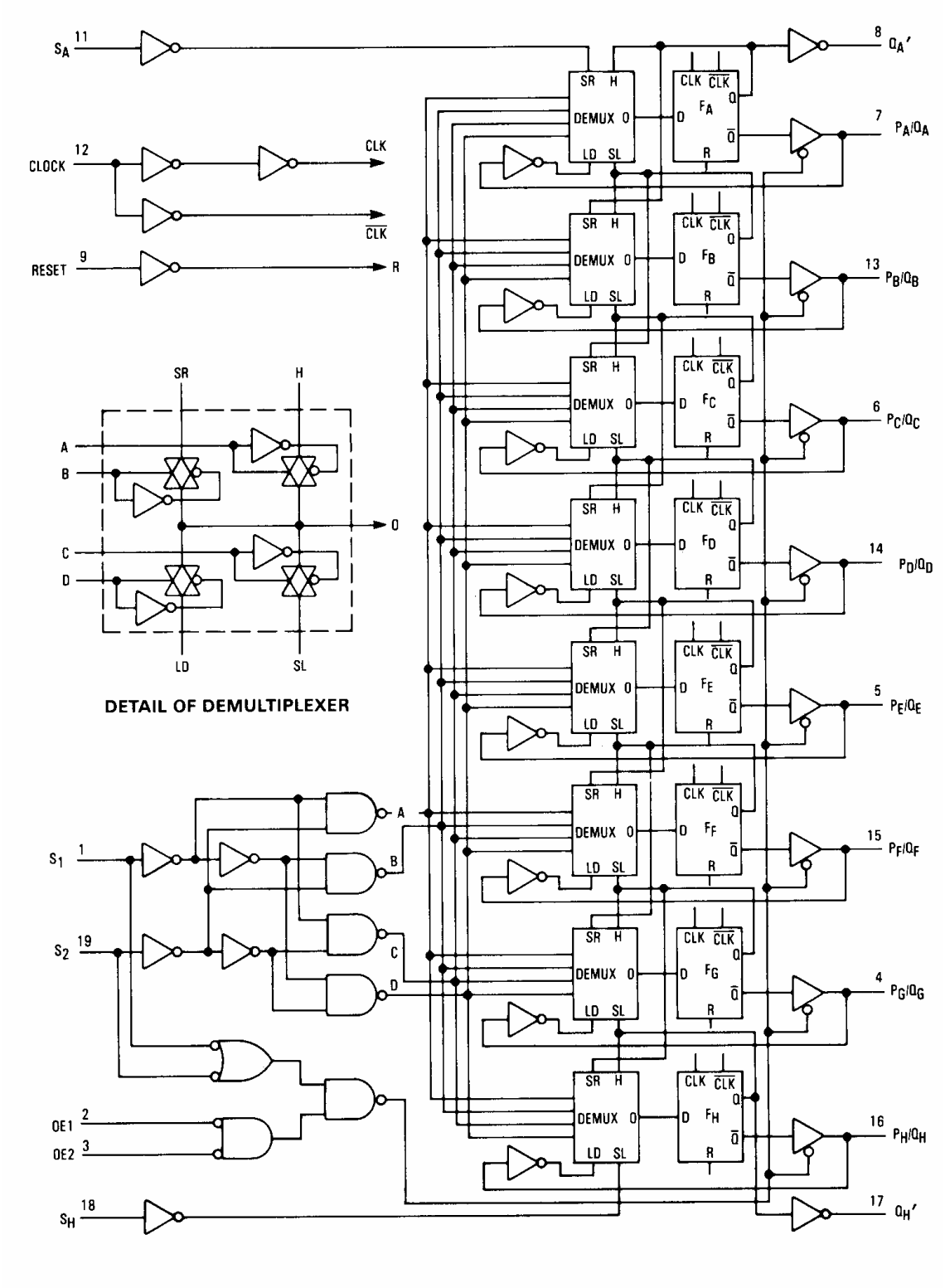


*Includes all probe and jig capacitance.

Figure 6. Test Circuit

INTEGRAL

EXPANDED LOGIC DIAGRAM



INTEGRAL