Integrated
Circuit
Systems, Inc.

ICS8520I-02

Low Skew, 1-to-16 Differential-to-LVHSTL Fanout Buffer

General Description

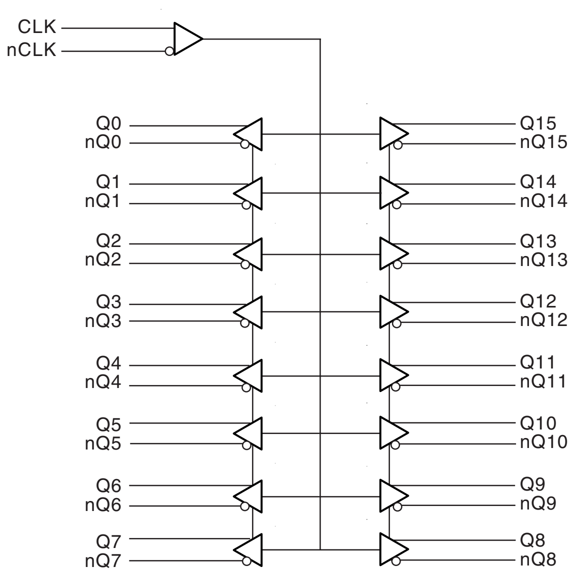
The ICS8520I-02 is a low skew, high performance 1-to-16 Differential-to-LVHSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8520I-02 has 1 differential clock input pair. The CLK, nCLK pair can accept most standard differential input levels.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS8520I-02 ideal for nterfacing to today's most advanced microprocessor and static RAMs.

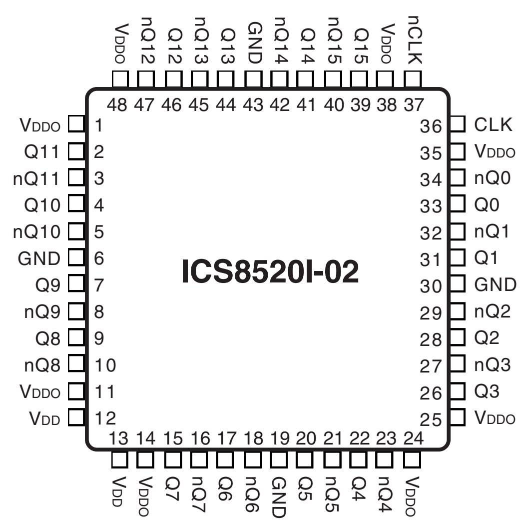
Features

- Sixteen differential LVHSTL compatible outputs each with the ability to drive 50Ω to ground
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 500MHz
- Translates single ended input levels to LVHSTL levels with resistor bias nCLK input
- V_{OH}: 1.3V (maximum)
- 40% of V_{OH} ≤ Vcrossover ≤ 60% of V_{OH}
- Output skew: 110ps (maximum)
- Part-to-Part skew: 450ps (maximum)
- 3.3V core, 1.8V output operating supply voltages
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

Block Diagram



Pin Assignment



48-Lead TQFP, E-Pad
7mm x 7mm x 1.0mm body package
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11, 14, 24, 25, 35, 38, 48	V_{DDO}	Power		Output supply pins.
2, 3	Q11, nQ11	Output		Differential output pair. LVHSTL interface levels.
4, 5	Q10, nQ10	Output		Differential output pair. LVHSTL interface levels.
6, 19, 30, 43	GND	Power		Power supply ground.
7, 8	Q9, nQ9	Output		Differential output pair. LVHSTL interface levels.
9, 10	Q8, nQ8	Output		Differential output pair. LVHSTL interface levels.
12, 13	V_{DD}	Power		Power supply pins.
15, 16	Q7, nQ7	Output		Differential output pair. LVHSTL interface levels.
17, 18	Q6, nQ6	Output		Differential output pair. LVHSTL interface levels.
20, 21	Q5, nQ5	Output		Differential output pair. LVHSTL interface levels.
22, 23	Q4, nQ4	Output		Differential output pair. LVHSTL interface levels.
26, 27	Q3, nQ3	Output		Differential output pair. LVHSTL interface levels.
28, 29	Q2, nQ2	Output		Differential output pair. LVHSTL interface levels.
31, 32	Q1, nQ1	Output		Differential output pair. LVHSTL interface level
33, 34	Q0, nQ0	Output		Differential output pair. LVHSTL interface level
36	CLK	Input	Pulldown	Non inverting differential clock input.
37	nCLK	Input	Pullup	Inverting differential clock input.
39, 40	Q15, nQ15	Output		Differential output pair. LVHSTL interface levels.
41, 42	Q14, nQ14	Output		Differential output pair. LVHSTL interface levels.
44, 45	Q13, nQ13	Output		Differential output pair. LVHSTL interface levels.
46, 47	Q12, nQ12	Output		Differential output pair. LVHSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information Section, "Wiring the Differential input to accept single ended levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	27.6°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				190	mA
I_{DDO}	Output Supply Current				10	µA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{IN} = V_{DD} = 3.465V			150	µA
		nCLK	V_{IN} = V_{DD} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		nCLK	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Voltage Range; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 4C. LVHSTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		0.9		1.3	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		40% x (V_{OH}–V_{OL}) + V_{OL}		60% x (V_{OH}–V_{OL}) + V_{OL}	V

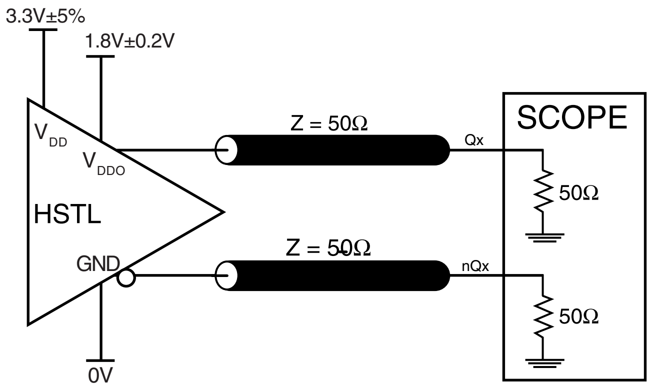
NOTE 1: Outputs terminated with 50Ω to ground.

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

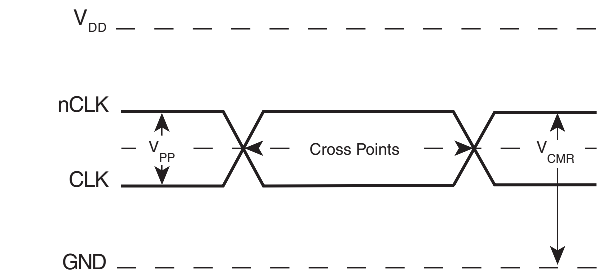
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay, Low-to-High; NOTE 1		1.1	1.35	1.6	ns
*t*sk(o)	Output Skew; NOTE 2, 4				110	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				450	ps
t_R/t_F	Output Rise/Fall Time	$f \le$ 300MHz	200		900	ps
		$f >$ 300MHz	200		600	ps
odc	Output Duty Cycle	$f \le$ 133MHz	48		52	%
		133 < $f \le$ 300MHz	46		54	%
		$f >$ 300MHz	45		55	%

NOTE 1: Measured from the differential input crossing point to the differential ouput crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

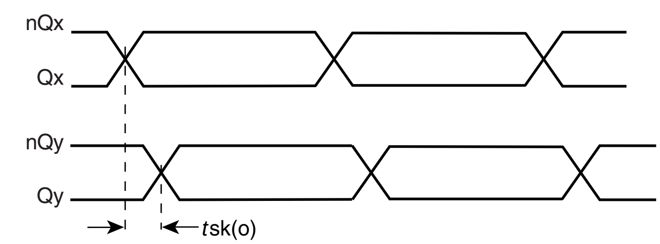
PARAMETER MEASUREMENT INFORMATION



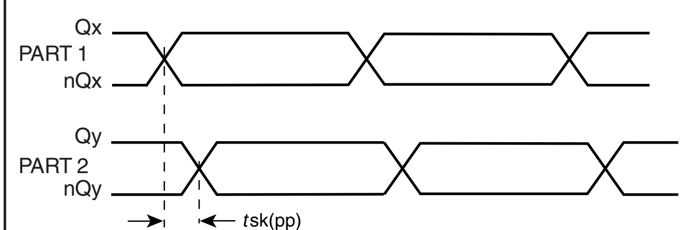
3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT



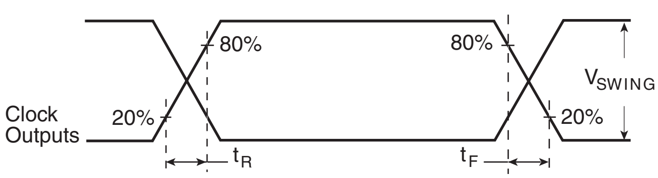
DIFFERENTIAL INPUT LEVEL



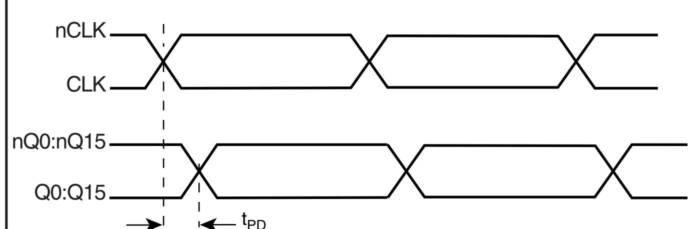
OUTPUT SKEW



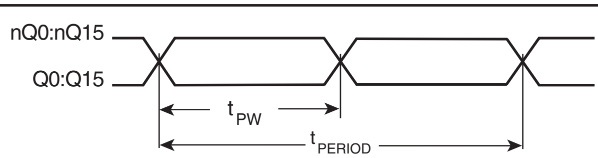
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLKx /nCLKx accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A* to *1E* show interface examples for the HiPerClockS CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 1A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

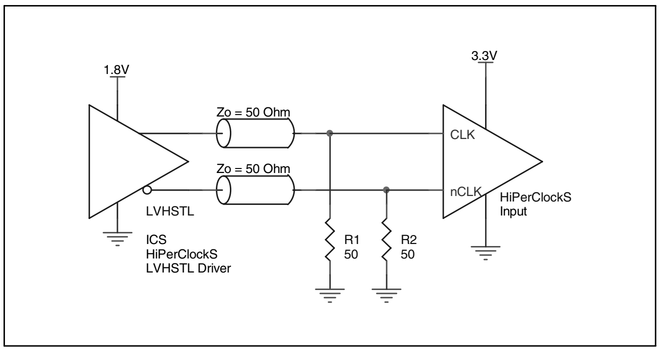


FIGURE 1A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

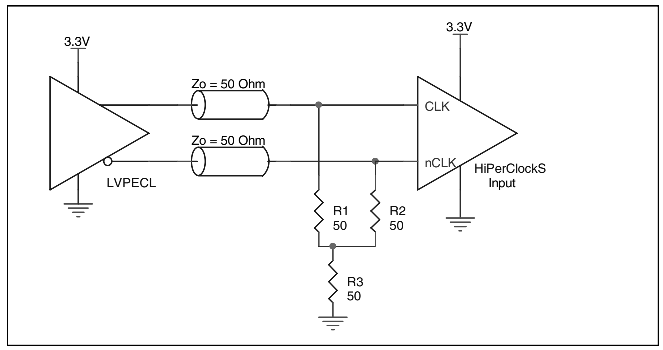


FIGURE 1B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

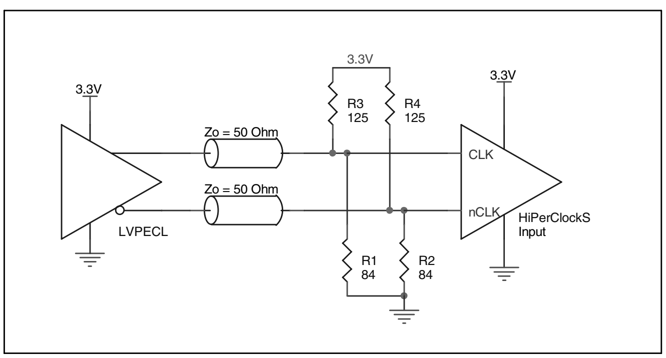


FIGURE 1C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

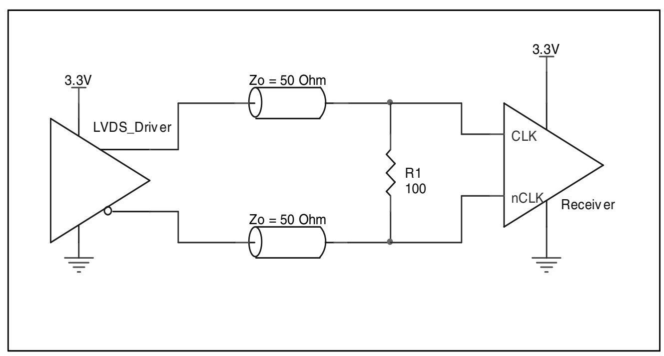


FIGURE 1D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

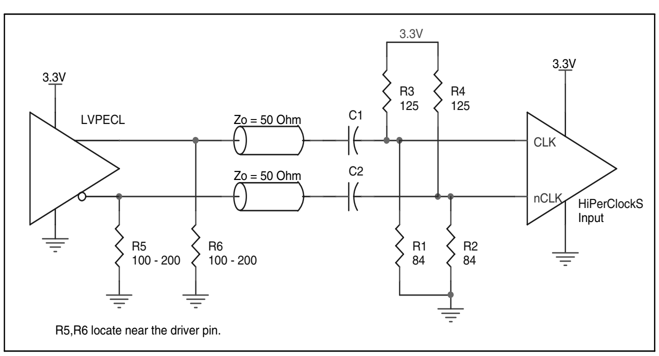


FIGURE 1E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVHSTL OUTPUT
All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8520I-02. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8520I-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 190mA = **658.4mW**
- Power (outputs)$_{MAX}$ = **32.6mW/Loaded Output pair**
  If all outputs are loaded, the total power is 16 * 32.6mW = **521.6mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 658.4mW + 521.6mW = **1180mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 22.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.18W * 22.6°C/W = 111.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	27.6°C/W	22.6°C/W	20.7°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 2.*

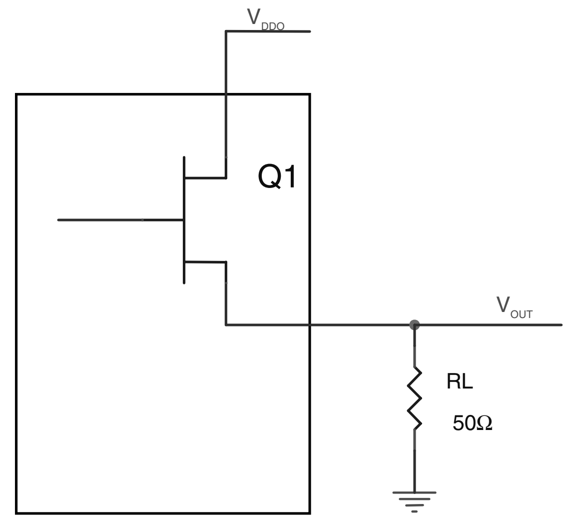


FIGURE 2. LVHSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DDO\_MAX} - V_{OH\_MIN})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$

Pd_H = (0.9V/50Ω) * (2V - 0.9V) = **19.8mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.6mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD TQFP, E-PAD

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	27.6°C/W	22.6°C/W	20.7°C/W

TRANSISTOR COUNT

The transistor count for ICS8520I-02 is: 1563

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD TQFP, E-PAD

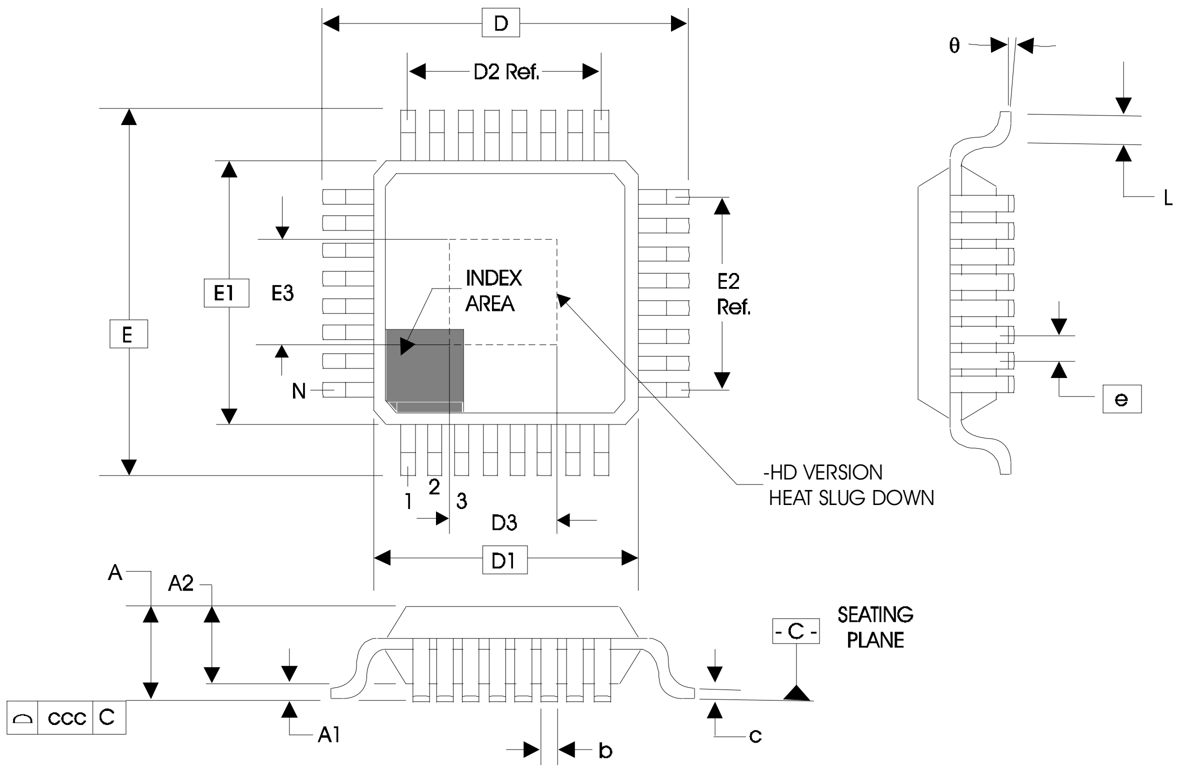


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABC - HD		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 BASIC		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 BASIC		
e	0.5 BASIC		
L	0.45	0.60	0.75
θ	0°		7°
ccc	--	--	0.08
D3 & E3	2.00		7.00

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8520DYI-02	ICS8520DYI-02	48 Lead TQFP, E-Pad	tray	-40°C to 85°C
ICS8520DYI-02T	ICS8520DYI-02	48 Lead TQFP, E-Pad	1000 tape & reel	-40°C to 85°C
ICS8520DYI-02LF	TBD	48 Lead "Lead-Free" TQFP, E-Pad	tray	-40°C to 85°C
ICS8520DYI-02LFT	TBD	48 Lead TQFP, E-Pad	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T2	2 10	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Corrected Package Dimensions and Package Outline.	11/19/04
B	 T9	1 7 9 12	Added lead-free bullet. Added *Recommendations for Unused Input and Output Pins.* Corrected Power Considerations, Power Dissipation calculation. Ordering Information Table - added lead-free part number and note. Updated layout of datasheet.	11/16/05