High Speed ±100V 3.0A Ultrasound Pulser

Features

- HVCMOS technology for high performance
- High density integration ultrasound transmitter
- Bipolar ±100V or unipolar 0 to 200V output voltage
- ±3A source and sink peak current
- Up to 10MHz operation frequency
- Matched delay times
- 1.8V to 5.0V CMOS logic interface
- Over temperature sensing
- Under voltage protections

Applications

- NDT ultrasound equipment
- Piezoelectric transducer drivers
- Sonar, ranger and flow metering

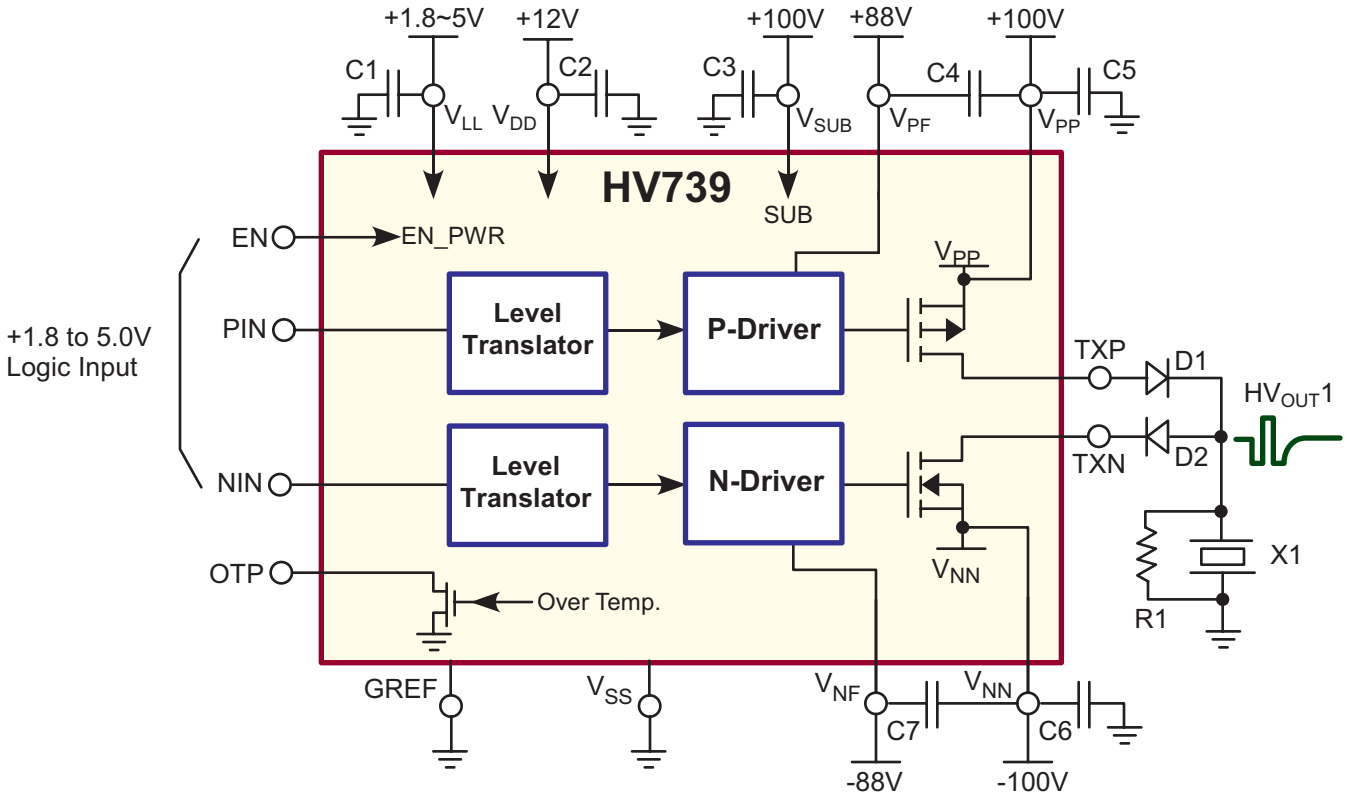
General Description

The Supertex HV739 is a single channel monolithic 200V 3.0A high-speed pulser. It is designed for NDT and medical ultrasound applications. This high voltage and high-current integrated circuit can also be used for other piezoelectric, capacitive or MEMS sensor in ultrasonic transducer and sonar ranger applications.

HV739 consists of controller logic interface circuit, voltage level translators, MOSFET gate drives and high current power P-channel and N-channel power MOSFETs as the output stage.

The output stage of HV739 is designed to provide output peak currents over 3.3A with up to 200V swing. The P- and N-channel power FETs gate drivers are supplied by two floating 10 to 12VDC power supplies referenced to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

Typical Application Circuit



Ordering Information

Device	Package Options
	32-Lead QFN *5x5mm body, 1.0mm height (max), 0.5mm pitch*
HV739	HV739K6-G

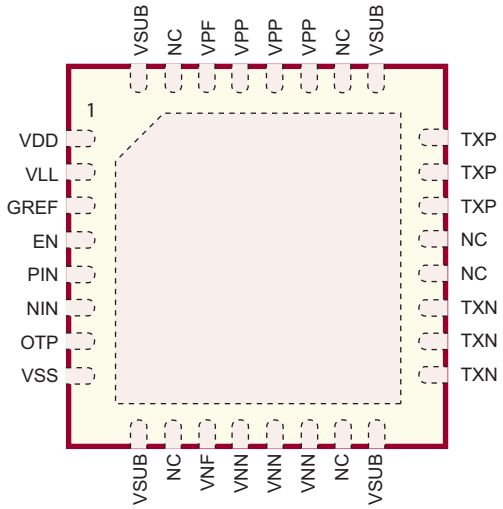
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{SS}, Power supply reference	0V
V_{LL}, Positive logic supply	-0.5V to +7V
V_{DD}, Positive logic and level translator supply	-0.5V to +14V
(V_{PP} -V_{PF}) Positive floating gate drive supply	-0.5V to +14V
(V_{NF}- V_{NN}) Negative gate floating drive supply	-0.5V to +14V
(V_{PP}-V_{NN}) Differential high voltage supply	-0.5V to +220V
V_{PP}, High voltage positive supply	-0.5V to +220V
V_{NN}, High voltage negative supply	-220V to +0.5V
All logic input PIN, NIN and EN pin voltages	-0.5V to +7V
Open drain output OPT pin voltage	-0.5V to +14V
(V_{SUB} - V_{PP}) Substrate to V_{PP} voltage difference	+220V
(V_{PP} –TXP_X) V_{PP} to TXP_X voltage difference	+220V
(V_{SUB}- TXP_X) Substrate to TXP_X voltage difference	+220V
(TXN_X-V_{NN}) TXN_X to V_{NN} voltage difference	+220V
Storage temperature	-65°C to 150°C
Thermal resistance, θ_{JA} *(4-layer,1oz, 4x3in. 9-via PCB)*	25°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



32-Lead QFN
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

32-Lead QFN

Power-Up Sequence

1	V_{SUB}
2	V_{LL} with logic signal low
3	V_{DD}
4	V_{PF} and V_{NF}
5	V_{PP} and V_{NN}
6	Logic control signals

Power-Down Sequence

1	All logic signals go to low
2	V_{PP} and V_{NN}
3	V_{PF} and V_{NF}
4	V_{DD}
5	V_{LL}
6	V_{SUB}

Operating Supply Voltages and Current (4 Channel Active)

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +12V, V_{PP}-V_{PF} = +12V, V_{NN}-V_{NF} = -12V, V_{PP} = +100V, V_{NN} = -100V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic voltage reference	1.8	3.3	5.0	V	---
V_{DD}	Internal voltage supply	10	12	12.5	V	---
V_{PF}	Positive gate driver supply	(V_{PP}-12)	-	(V_{PP}-10)	V	Floating driver voltage supplies.
V_{NF}	Negative gate drive supply	(V_{NN}+10)	-	(V_{NN}+12)	V	
V_{SUB}	IC substrate voltage	V_{DD}	V_{PP}	+220	V	Must connect to the most positive potential of the IC.
V_{PP}	Positive HV supply	0	-	+220	V	---
V_{NN}	Negative HV supply	-220	-	0	V	---
I_{LL}	V_{LL} Current EN = Low	-	-	250	µA	---
I_{DDQ}	V_{DD} Current EN = Low	-	100	-	µA	---
I_{DDEN}	V_{DD} Current EN = High	0.1	0.3	0.7	mA	f = 0MHz
	V_{DD} Current at 5.0MHz	-	0.5	-	mA	f = 5.0MHz, no loads
I_{PPQ}	V_{PP} Current EN = Low	-	1.0	5.0	µA	---
I_{PPEN}	V_{PP} Current at 5.0MHz	-	5.6	-	mA	f = 5.0MHz, no loads
I_{NNQ}	V_{NN} Current EN = Low	-	1.0	5.0	µA	---
I_{NNEN}	V_{NN} Current at 5.0MHz	-	5.6	-	mA	f = 5.0MHz, no loads
I_{PFQ}	V_{PF} Current EN = Low	-	10	20	µA	---
I_{PFEN}	V_{PF} Current at 5.0MHz	-	12.2	-	mA	f = 5.0MHz, no loads
I_{NFQ}	V_{NF} Current EN = Low	-	10	20	µA	---
I_{NFEN}	V_{NF} Current at 5.0MHz	-	6.4	-	mA	f = 5.0MHz, no loads

DC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +12V, V_{PP}-V_{PF} = +12V, V_{NN}-V_{NF} = -12V, V_{PP} = +100V, V_{NN} = -100V, T_A = 25°C)

Output P-Channel MOSFET, TXP

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	3.0	3.3	-	A	1.0Ω load to ground, V_{DS}= 12V
R_{ON}	Channel resistance	-	6.9	-	Ω	I_{SD} = 500mA
C_{OSS}	Output capacitance	-	87	-	pF	V_{DS} = 25V, f = 1.0MHz

Output N-Channel MOSFET, TXN

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	3.0	3.3	-	A	1.0Ω load to ground, V_{DS}= 12V
R_{ON}	Channel resistance	-	7.0	-	Ω	I_{SD} = 500mA
C_{OSS}	Output capacitance	-	87	-	pF	V_{DS} = 25V, f = 1.0MHz

Logic Inputs

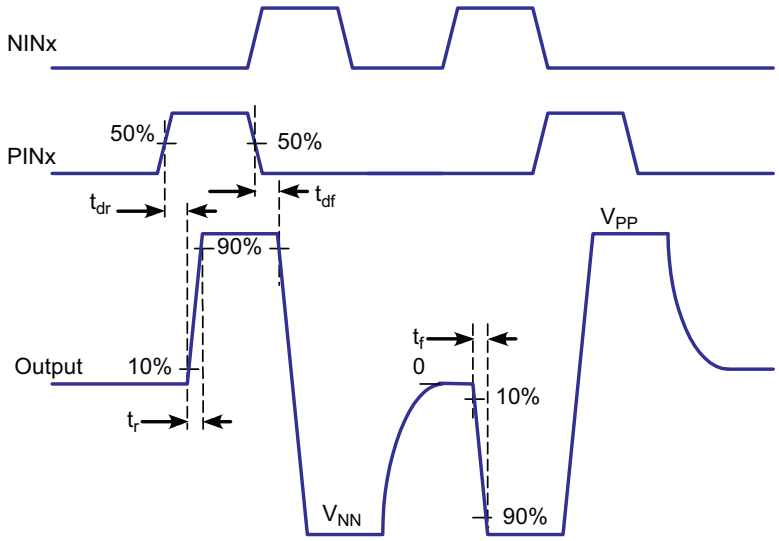
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	0.8V_{LL}	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	0.2V_{LL}	V	---
I_{IH}	Input logic high current	-	-	10	µA	---
I_{IL}	Input logic low current	-10	-	-	µA	---
C_{IN}	Input logic capacitance	-	-	5.0	pF	---

AC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS}= 0V, V_{LL}= +3.3V, V_{DD}= +12V, V_{PP}-V_{PF} = +12V, V_{NN}-V_{NF}= -12V, V_{PP} = +100V, V_{NN} =-100V,T_A= 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{OUT}	Output frequency range	-	-	35	MHz	100Ω resistor load
HD2	Second harmonic distortion	-	-35	-	dB	
t_{EN}	Power enable time	-	70	250	µs	
t_{DIS}	Power disable time	-	1.0	10	µs	
t_{drp}	Delay time on rise time P-ch	-	15	35	ns	
t_{dfp}	Delay time on fall time P-ch	-	15	35	ns	
t_{drn}	Delay time on rise time N-ch	-	18	35	ns	
t_{dfn}	Delay time on fall time N-ch	-	18	35	ns	
t_r	Output rise time	-	50	65	ns	220pF//1.0kΩ load
t_f	Output fall time	-	50	65	ns	

Switching Time Diagram

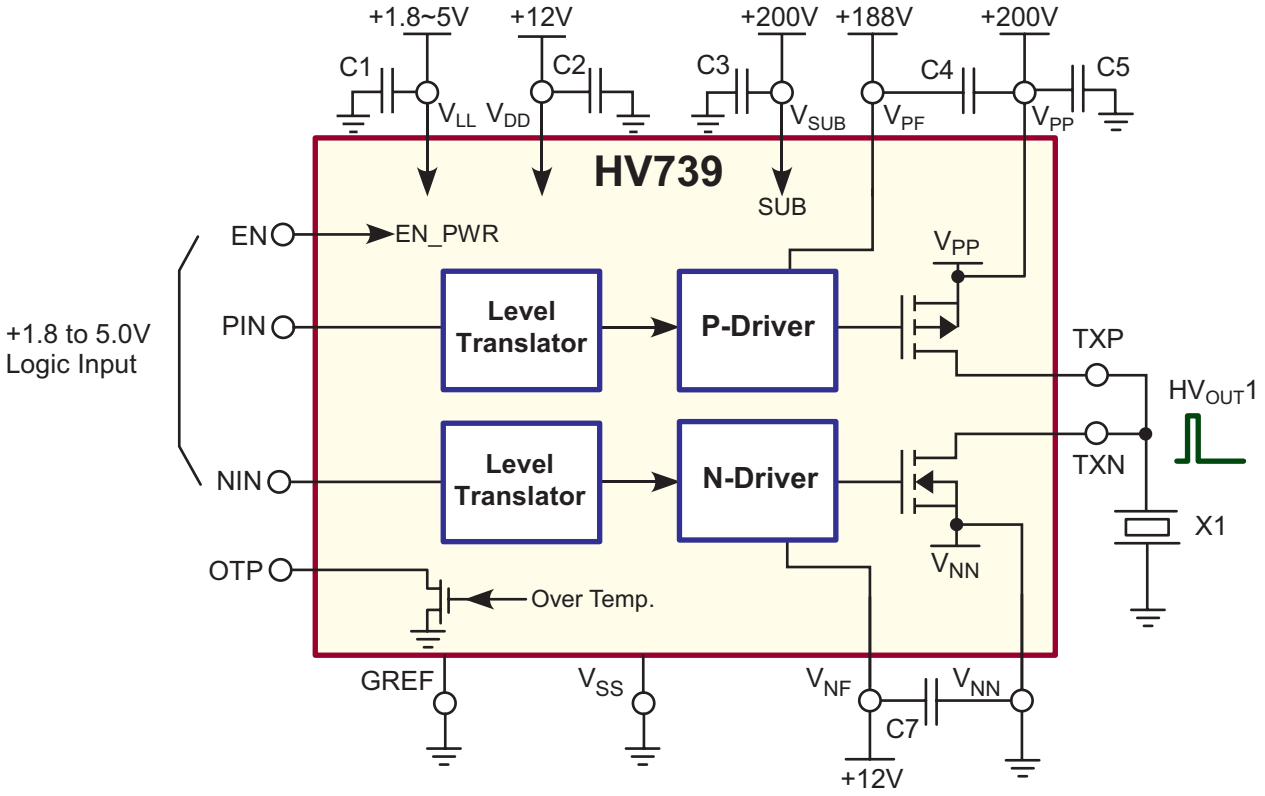


Truth Table

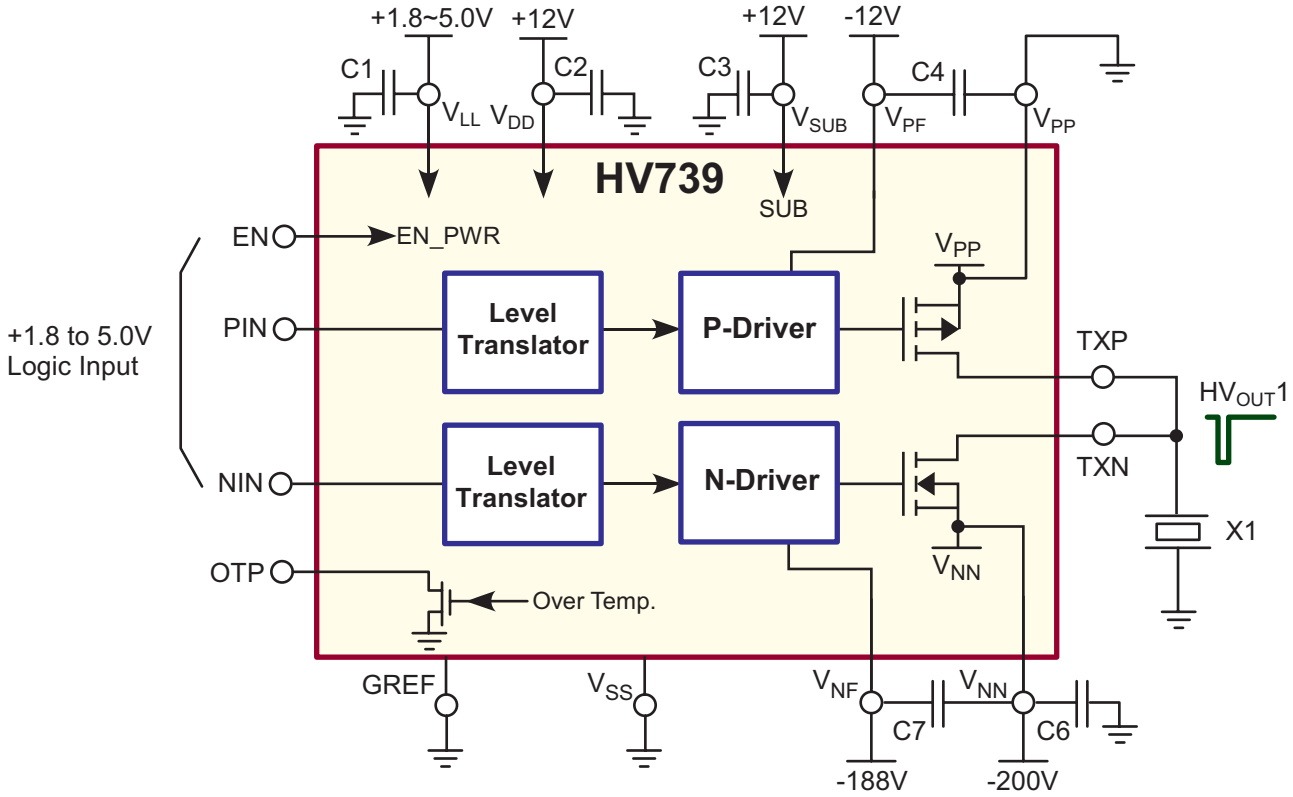
Logic Inputs			Output	
EN	PIN	NIN	TXP	TXN
1	0	0	OFF	OFF
1	1	0	ON	OFF
1	0	1	OFF	ON
1	1	1	ON*	ON*
0	X	X	OFF	OFF

***Note:** Not allowed, may damage IC*

+200V Unipolar Pulser



-200V Unipolar Pulser

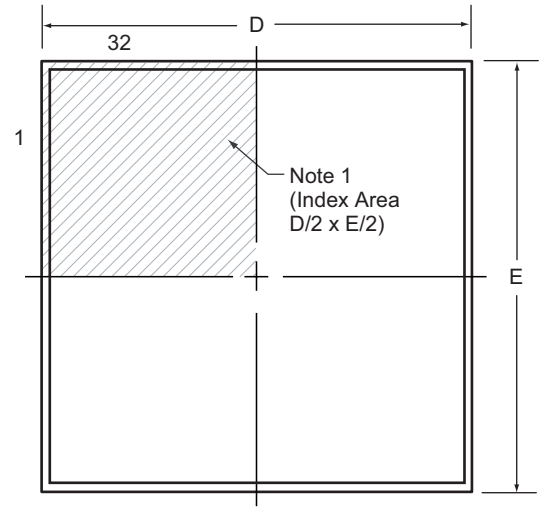


Pin Description

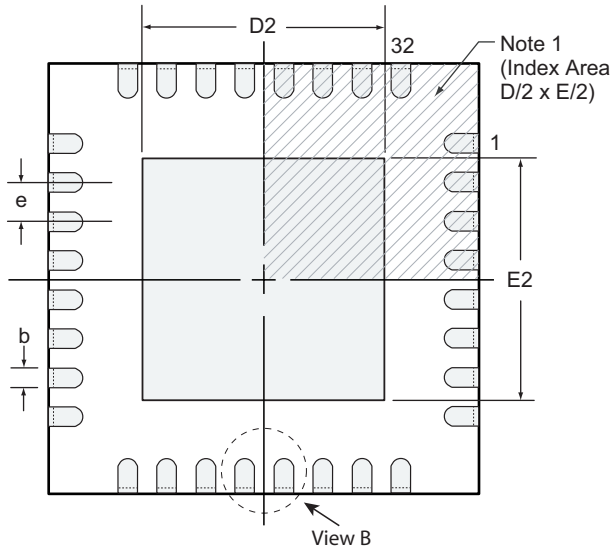
Name	Function
V_{SS}	Power supply return (0V)
V_{DD}	Positive internal voltage supply (+12V).
V_{LL}	Logic voltage high reference input (+3.3V).
GREF	Logic voltage low reference. Logic ground (0V).
V_{PP}	Positive high voltage power supply (+100V).
V_{NN}	Negative high voltage power supply (-100V).
V_{PF}	P-FET gate driver floating power supply, (V_{PP}- V_{PF}) = +12V.
V_{NF}	N-FET gate driver floating power supply, (V_{NF}- V_{NN}) = +12V.
TXP	Output P-FET drain (open drain output).
TXN	Output N-FET drain (open drain output).
PIN	Input logic control of high voltage output P-FET, Hi = on, Low = off.
NIN	Input logic control of high voltage output N-FET, Hi = on, Low = off.
EN	Chip power enable Hi = on, Low=off.
OTP	Open drain output for over temperature protection, Low = over temp.
NC	No connection
V_{SUB} (Pad)	Substrate is internally connected to the central thermal pad on the bottom of package. It must be connected to the most positive potential of the IC externally.

32-Lead QFN Package Outline (K6)

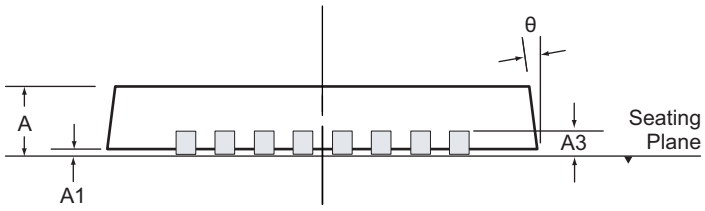
5x5mm body, 1.0mm height (max), 0.50mm pitch



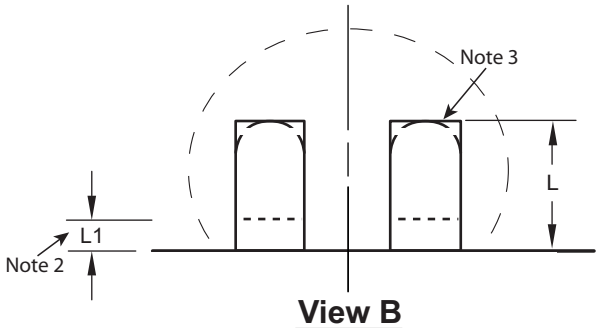
Top View



Bottom View



Side View



View B

Notes:

1. *Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	4.85	3.20	4.85	3.20	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	5.00	-	5.00	-		0.40	-	-
	MAX	1.00	0.05		0.30	5.15	3.70	5.15	3.70		0.50	0.15	14°

JEDEC Registration MO-220, Variation VHHD-5, Issue K, June 2006.
Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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