This serial-in, serial-out, 8-bit shift register is composed of eight R-S master-slave flip-flops, input gating, and a clock drive. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

EFUNCTION TABLE

Ing	Inputs ta		Outputs tn+8		
A	В	Qн	Q́я		
Н	Н	Н	L		
L	X	L	Н		
Х	I.	ī.	Н		

Notes) H; high level, L; low level, X; irrelevant

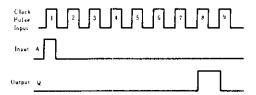
tn; Reference bit time, clock low

tn+8; Bit time after 8 low-to-high clock transitions.

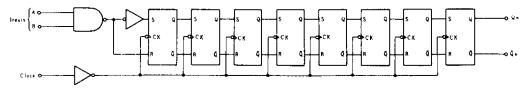
MRECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	max	Unit	
Clock pulse width	t u	25	_	ns	
Setup time	ts u	25	-	ns	
Hold time	Üh	5		ns	

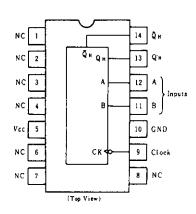
TIMING CHART



BLOCK DIAGRAM



MPIN ARRANGEMENT



ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
	V_{IH}			2.0			ν
Input voltage	V_{IL}				-	0.8	V
	Von	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8$	V, Ion = -400μA	2.7			V
Output voltage	Vot	$V_{CC} = 4.75V$, $V_{IB} = 2V$	IoL = 4mA	-		0.4	v
		$V_{IL}=0.8V$	$I_{OL} = 8 \text{mA}$			0.5	V
Input current	Іін	$V_{CC} = 5.25 \text{V}, V_I = 2.7 \text{V}$				20	μA
	Iιι	$V_{CC} = 5.25 \text{V}, V_I = 0.4 \text{V}$				··· 0 . 4	m A
	It	$V_{CC} = 5.25 \text{V}, V_I = 7 \text{V}$			-	0.1	mA
Short circuit output current	Ios	$V_{CC} = 5.25V$		- 20		- 100	m A
Supply current	Icc**	$V_{CC} = 5.25 \text{V}$			12	20	mА
Input clamp voltage	VIK	$V_{CC} = 4.75 \text{V}, I_{IN} = 18 \text{m}$	A	_		-1.5	V

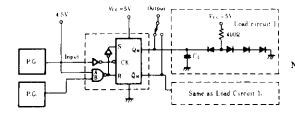
^{*} V_{CC} =5V, Ta=25°C

ESWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Maximum clock frequency	fmax .	and the state of t	10	18	-	MHz
	TP1.H	$C_L = 15 \text{pF}, R_L = 2 \text{k}\Omega$		24	40	ns
Propagation delay time	trut			27	40	ns

TESTING METHOD

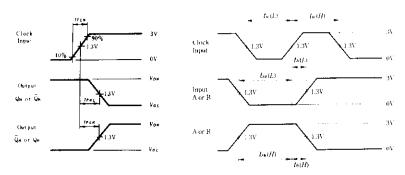
1) Test Circuit



Notes) 1. Input pulse; $t_{TLH} \le 15 \text{ ns}$, $t_{THL} \le 6 \text{ns}$, PRR = 1 MHz, duty cycle=50%

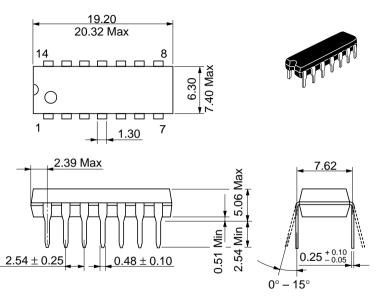
C_L includes probe and jig capacitance.
 All diodes are 1S2074 (1).

Waveform



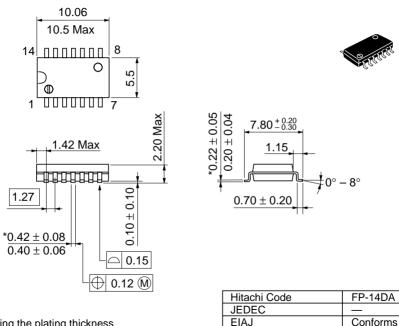
^{**} ICC is measured after the eighth clock pulse with the output open and A and B inputs grounded.

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

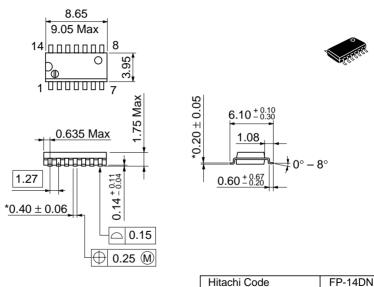


Weight (reference value)

0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



*Pd plating

JEDEC Conforms

EIAJ Conforms

Weight (reference value) 0.13 g

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