



DR8051

8-bit RISC Microcontroller

ver 2.00

OVERVIEW

DR8051 soft core is binary-compatible with the industry standard 8051 8-bit microcontroller and can achieve a performance of up to **55 million instructions** per second in today's integrated circuit technologies. DR8051 has RISC architecture that is 6.7 time faster compare to the original implementation.

KEY FEATURES

- ◆ Software compatible with industry standard 8051
- ◆ RISC architecture
- ◆ 6.7 times faster than the original implementation
- ◆ 4-clk periods multiplication
- ◆ 5-clk periods division
- ◆ Up to 16M bytes of external standard Data Memory
- ◆ Up to 256 bytes of internal dual port Data Memory
- ◆ Up to 64K bytes of Program Memory

- ◆ User programmable RAMWE and RAMRD pulses between 1 to 8 clock periods
- ◆ De-multiplexed Address/Data Bus to allow easy connection to memory
- ◆ Over 16 times data transfer faster than the original implementation
- ◆ Two 16-bit timer/counters
- ◆ Full-duplex serial port
- ◆ Support for External SFRs
- ◆ Fully synthesizable, static synchronous design with no internal tri-states
- ◆ 1 GHz virtual clock frequency compare to the original implementation (over 150 MHz in a typical 0.25u technological process)

SPECIAL FEATURES

- ◆ I2C bus controller
- ◆ Floating-Point arithmetic coprocessor IEEE-754 standard single precision
 - ✓ *FADD, FSUB* - addition, subtraction
 - ✓ *FMUL, FDIV*- multiplication, division
 - ✓ *FSQRT*- square root

- ✓ *FUCOM* - compare
- ✓ *FCHS* - change sign
- ✓ *FABS* - absolute value

- ◆ Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers
 - ✓ *FADD*, *FSUB*- addition, subtraction
 - ✓ *FMUL*, *FDIV*- multiplication, division
 - ✓ *FSQRT*- square root
 - ✓ *FUCOM*- compare
 - ✓ *FCHS* - change sign
 - ✓ *FABS* - absolute value
 - ✓ *FSIN*, *FCOS*- sine, cosine
 - ✓ *FPTAN*, *FPATAN*- tangent, arcs tangent

Up to 104 External Special Function Registers (ESFRs) may be added to the DR8051 design. ESFRs are memory mapped into Direct Memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

✓ **STRETCH MEMORY CYCLE REGISTER:**

Allows applications software to adjust to different external RAM speeds (XRAMWR and XRAMRD pulse between 1 – 8 clock cycles).

✓ **EXTERNAL RAM:**

Allows applications software to access up to 16 MB of external data memory. Extra DPP(*Data Page Pointer*) register is used for segments swapping.

DELIVERABLES

- ◆ VHDL, Verilog source code
- ◆ VITAL simulation model
- ◆ HDL test bench
- ◆ Synthesis scripts
- ◆ Technical documentation
- ◆ Technical support

DESIGN FEATURES

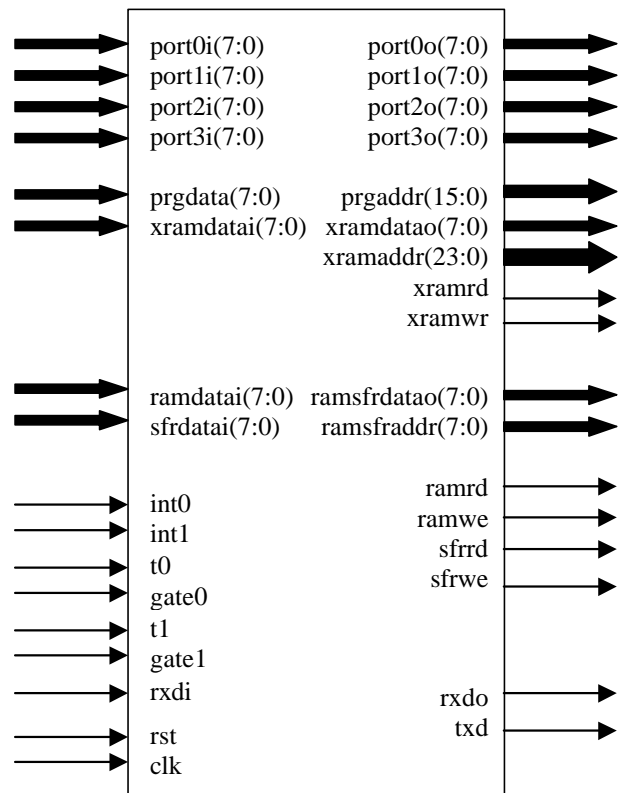
✓ **DATA MEMORY:**

The DR8051 can address Internal Data Memory of up to 256 bytes, and up to 16M bytes of external Data RAM via the function interconnect signals. The Internal Data Memory can be implemented as Single-Port synchronous or asynchronous RAM.

✓ **EXTERNAL SPECIAL FUNCTION REGISTERS:**

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SYMBOL



PINS DESCRIPTION

<http://www.dcd.com.pl>

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
port0i[7:0]	input	Port 0 input
port1i[7:0]	input	Port 1 input
port2i[7:0]	input	Port 2 input
port3i[7:0]	input	Port 3 input
prgdata[7:0]	input	Data bus from program memory
xramdatai[7:0]	input	Data bus from ext. data memory
ramdati[7:0]	input	Data bus from int. data memory
sfrdatai[7:0]	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
t0	input	Timer 0 input
t1	input	Timer 1 input
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
rxdi	input	Serial receiver input
port0o[7:0]	output	Port 0 output
port1o[7:0]	output	Port 1 output
port2o[7:0]	output	Port 2 output
port3o[7:0]	output	Port 3 output
prgaddr[15:0]	output	Program memory address bus
xramaddr[23:0]	output	External data memory address bus
xramdatao[7:0]	output	Data bus for external data memory
xramwr	output	External data memory write
xramrd	output	External data memory read
ramsfraddr[7:0]	output	RAM and SFR's address bus
ramsfrdatao[7:0]	output	Data bus for internal data memory
ramwe	output	Internal data memory write enable
ramrd	output	Internal data memory read
sfrwe	output	User SFR's write enable
sfrrd	output	User SFR's read
rxdo	output	Serial receiver output
txd	output	Serial transmitter output

The following table gives a survey about the DR8051 performance in ALTERA® devices after Place & Route (all key features have been included):

a) FLEX™ 10K100E-1

Area - 2049 LC + 1EAB
System clock f_{max} - 58 MHz

b) APEX™ 20K100E-1

Area - 2120 LC
System clock f_{max} - 58 MHz

c) ACEX™ 1K100-1

Area - 2096 LC + 1 EAB
System clock f_{max} - 57 MHz

PERFORMANCE

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MODIFICATIONS

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