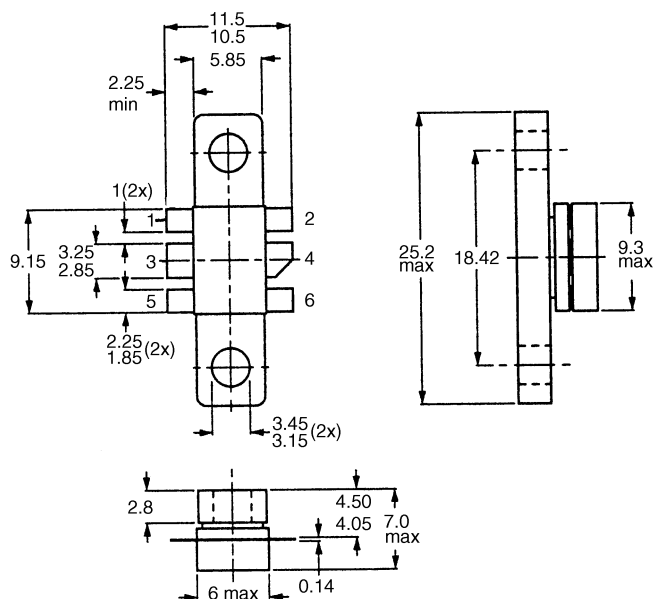


MECHANICAL DATA



**GOLD METALLISED
MULTI-PURPOSE SILICON
DMOS RF FET
15W – 12.5V – 500MHz
SINGLE ENDED**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- VERY LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 11 dB MINIMUM

SOT 171

PIN 1	SOURCE	PIN 2	SOURCE
PIN 3	GATE	PIN 4	DRAIN
PIN 5	SOURCE	PIN 6	SOURCE

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from 1 MHz to 1 GHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	50W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current *	12A
T_{stg}	Storage Temperature	-65 to $150^{\circ}C$
T_j	Maximum Operating Junction Temperature	$200^{\circ}C$

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{DSS} Drain–Source Breakdown Voltage	V _{GS} = 0 I _D = 10mA	40			V
I _{DSS} Zero Gate Voltage Drain Current	V _{DS} = 12.5V V _{GS} = 0			1	mA
I _{GSS} Gate Leakage Current	V _{GS} = 20V V _{DS} = 0			6	μA
V _{GS(th)} Gate Threshold Voltage *	I _D = 10mA V _{DS} = V _{GS}	1		7	V
g _{fs} Forward Transconductance *	V _{DS} = 10V I _D = 0.6A	1.08			S
G _{PS} Common Source Power Gain	P _O = 15W	11			dB
η Drain Efficiency	V _{DS} = 12.5V I _{DQ} = 0.6A	50			%
VSWR Load Mismatch Tolerance	f = 500MHz	20:1			—
C _{iss} Input Capacitance	V _{DS} = 0 V _{GS} = -5V f = 1MHz			72	pF
C _{oss} Output Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			60	pF
C _{rss} Reverse Transfer Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			6	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max.3.5°C / W
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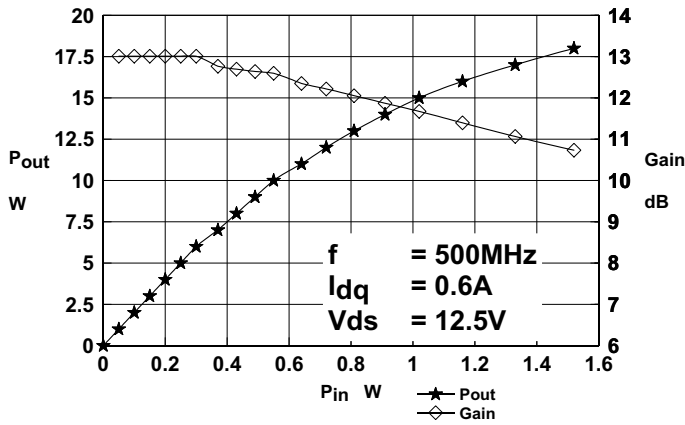


Figure 1
Output power and Gain vs. Input Power

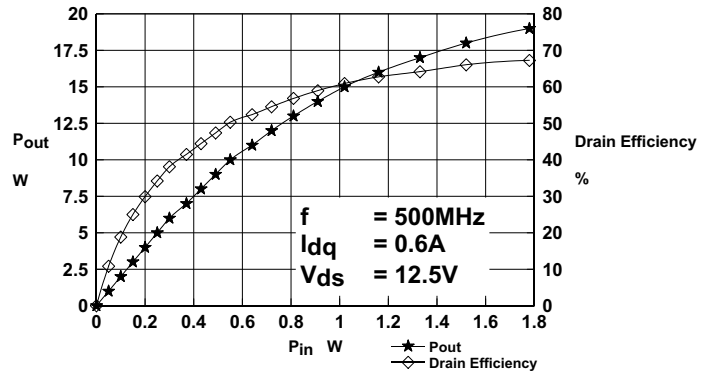


Figure 2
Output power and Efficiency vs. Input Power

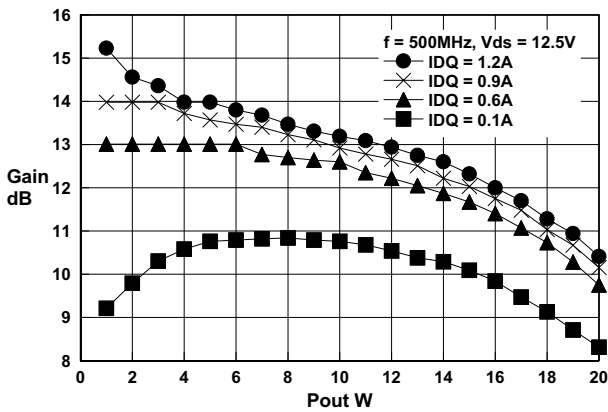


Figure 3
Gain vs. Output Power

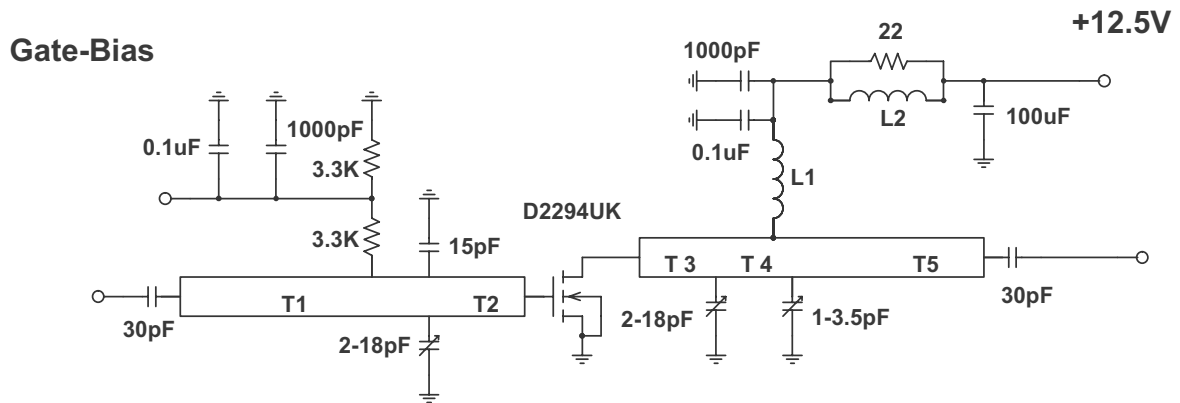
OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	ZL Ω	ZS Ω
500	1.7 + j5.7	3.3+j1.1

Typical S Parameters

! Vds=12.5V, Idq=0.6A
MHZ S MA R 50

Freq MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
70	0.73	-137	14.61	92	0.02	2	0.67	-154
100	0.74	-146	10.8	83	0.02	-3	0.69	-159
150	0.76	-154	6.86	69	0.019	-13	0.73	-163
200	0.78	-159	4.8	60	0.017	-18	0.76	-165
250	0.8	-162	3.6	52	0.015	-22	0.79	-167
300	0.82	-165	3	47	0.014	-22	0.82	-168
350	0.84	-167	2.27	38	0.012	-23	0.84	-171
400	0.86	-169	1.92	34	0.01	-23	0.86	-172
450	0.88	-171	1.52	27	0.008	-20	0.88	-174
500	0.89	-173	1.31	24	0.006	-8	0.89	-175
550	0.9	-174	1.09	19	0.006	7	0.91	-177
600	0.92	-175	0.94	12	0.006	17	0.92	-178
650	0.93	-176	0.74	12	0.006	33	0.93	-180
700	0.94	-178	0.65	7	0.007	39	0.94	179
750	0.94	-180	0.53	8	0.007	49	0.94	178
800	0.95	180	0.43	8	0.008	54	0.95	177
850	0.95	180	0.39	14	0.009	65	0.95	176
900	0.96	178	0.37	15	0.011	69	0.96	175
950	0.95	177	0.35	19	0.013	72	0.95	174
1000	0.95	177	0.34	17	0.014	71	0.96	173



500MHz Test Fixture

Substrate 1.6mm FR4
All microstrip lines $W = 2.75\text{mm}$

T1 47mm
T2 9mm
T3 9mm
T4 13mm
T5 32mm

L1 7 turns 24swg enamelled copper wire, 2mm i.d.
L2 1.5 turns 24swg enamelled copper wire on ferrite core