CS61310

# T1 Line Interface Unit

## Features

- Provides T1 line interface
- No crystal needed for jitter attenuation
- Greater than 14 dB of transmit return loss
- Meets AT&T 62411 jitter tolerance and attenuation requirements
- Meets ANSI T1.231B requirements for LOS and AIS
- AWG for user programmable pulse shapes
- TX driver high impedance / low power control
- Generation and detection of loop up / loop down signaling
- Selectable unipolar or bipolar I/O
- Compliant with:
  - — American National Standards (ANSI): T1.102, T1.105, T1.403, T1.408, and T1.231
  - — FCC Rules and Regulations: Part 68 and Part 15
  - — AT&T Publication 62411
  - — TR-NET-00499

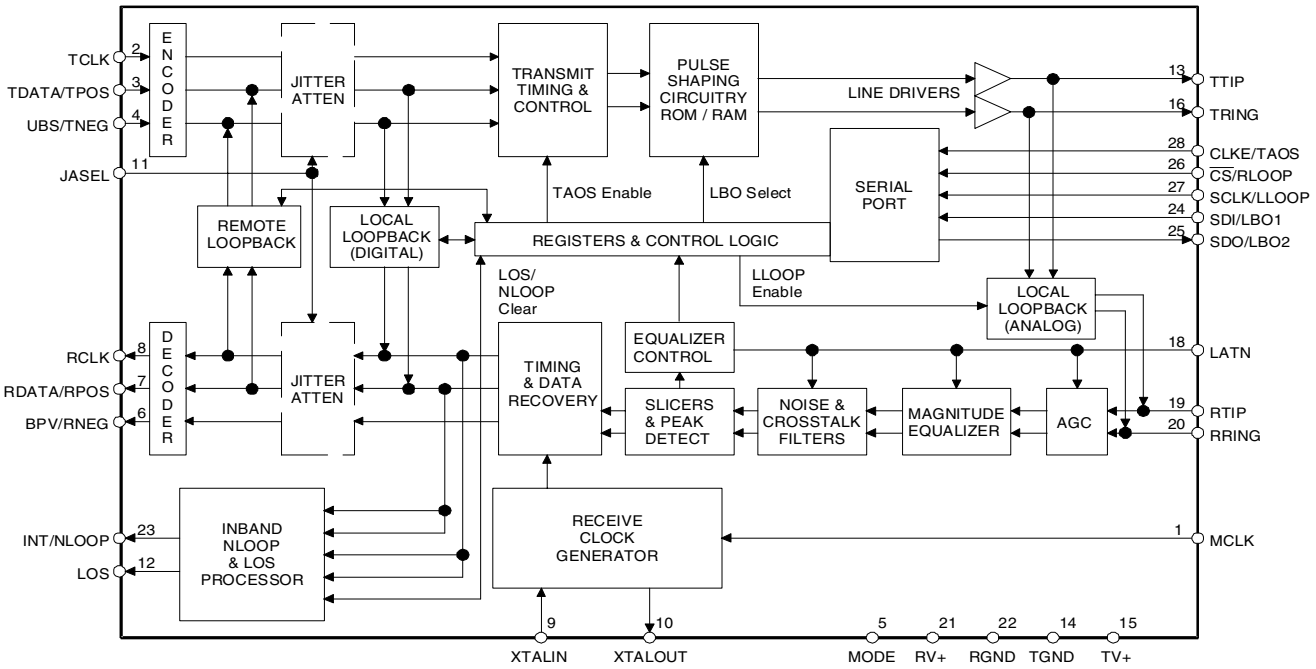
## Description

The CS61310 is a T1 primary rate line interface unit. It combines the complete analog transmit-and-receive circuitry for a single, full-duplex interface at T1 rates. The device is pin- and function-compatible with the Level One LXT310.

Enhanced functionality is available through an extended register set, allowing custom pulse shape generation as well as generation and detection of loop up and loop down codes. The CS61310 features crystal-less jitter attenuation.

**ORDERING INFORMATION**

CS61310-IL 28-pin PLCC




*Final Product Information*

This document contains advanced information for a new product.
Cirrus Logic reserves the right to modify this product without notice.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# 1. CHARACTERISTICS AND SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| DC Supply (referenced to RGND=TGND=0 V) | RV+<br>TV+ | -<br>- | 6.0<br>(RV+) + 0.3 | V<br>V |
| Input Voltage, Any Pin | $V_{in}$ | RGND-0.3 | (RV+) + 0.3 | V |
| Input Current, Any Pin (Note 1) | $I_{in}$ | -10 | 10 | mA |
| Ambient Operating Temperature | $T_A$ | -40 | 85 | °C |
| Storage Temperature | $T_{stg}$ | -65 | 150 | °C |

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| DC Supply (Note 2) | RV+, TV+ | 4.75 | 5.0 | 5.25 | V |
| Ambient Operating Temperature | $T_A$ | -40 | 25 | 85 | °C |
| Power Consumption (Notes 3, 4, 5) | $P_C$ | - | 390 | 630 | mW |

Notes: 2. TV+ must not exceed RV+ by more than 0.3 V.

3. Power consumption measured while driving line load over operating temperature range. Power consumption includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
4. Typical consumption corresponds to 50% ones density and medium line length at 5.0 V.
5. Maximum consumption corresponds to 100% ones density and maximum line length at 5.25 V.

## DIGITAL CHARACTERISTICS

(TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%; GND = 0 V)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage (Note 6) PINS 1-4, 24-28 | $V_{IH}$ | 2.0 | - | - | V |
| Low-Level Input Voltage (Note 6) PINS 1-4, 24-28 | $V_{IL}$ | - | - | 0.8 | V |
| High-Level Output Voltage $I_{OUT}$ = -40 µA (Notes 6, 7) PINS 6-8, 25 | $V_{OH}$ | 2.4 | - | - | V |
| Low-Level Output Voltage $I_{OUT}$ = 1.6 mA (Notes 6, 7) PINS 6-8, 25 | $V_{OL}$ | - | - | 0.4 | V |
| Input Leakage Current | | - | - | ±10 | µA |

Notes: 6. This specification guarantees TTL compatibility ($V_{OH}$ = 2.4 V @ $I_{OUT}$ = -40 µA).

7. Output drivers are TTL compatible and will drive CMOS logic levels into a CMOS load.

## ANALOG CHARACTERISTICS

(TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%; GND = 0 V)

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Transmitter*** | | | | | |
| AMI Output Pulse Amplitudes | (Note 8) | | | | |
| | T1, (FCC Part 68) (Note 9) | 2.7 | 3.0 | 3.3 | V |
| | T1, DSX-1 (Note 10) | 2.4 | 3.0 | 3.6 | V |
| External Equalizer Pulse Amplitude | | 4.8 | 5.6 | | V |
| Transmitter Output Impedance | (Note 12) | | | | |
| Transformer turns ratio = 1:2 | | | 1.5 | | Ω |
| Transformer turns ratio = 1:1.5 | FCC | | 44 | | Ω |
| | DSX1 | | 44 | | Ω |
| | External Equalizer | | 44 | | Ω |
| Jitter Added by the Transmitter | (Notes 11,12) | | | | |
| | 10 Hz - 8 kHz | - | 0.015 | - | UI |
| | 8 kHz - 40 kHz | - | 0.015 | - | UI |
| | 10 Hz - 40 kHz | - | 0.015 | - | UI |
| | Broad Band | - | 0.020 | - | UI |
| Power in 2 kHz band about 772 kHz | (Notes 8, 12) | 12.6 | 15 | 17.9 | dBm |
| Power in 2 kHz band about 1.544 MHz (referenced to power in 2 kHz band at 772 kHz) | (Notes 8, 12) | -29 | -38 | - | dB |
| Positive to Negative Pulse Imbalance | (Notes 8, 12) | - | 0.2 | 0.5 | dB |
| Transmitter Short Circuit Current | (Notes 8, 13) | - | - | 50 | mA RMS |
| ***Receiver*** | | | | | |
| RTIP/RRING Input Impedance | | - | 20k | - | Ω |
| Sensitivity Below DSX (0 dB = 3.0 V) | | -40 | - | - | dB |
| | | 30 | - | - | mV |
| Loss of Signal Threshold | | - | -42 | - | dB |
| Data Decision Threshold | (Notes 12,14) T1, DSX-1 | | 50 | | % of peak |
| | T1, (FCC Part 68) | | 50 | | % of peak |
| Allowable Consecutive Zeros before LOS | | 160 | 175 | 190 | bits |
| Receiver Input Jitter Tolerance | (Note 16) T1:10 kHz - 100 kHz | 0.4 | - | - | UI |
| | (Note 12) 1 Hz | 138 | - | - | UI |

Notes:
8. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.
9. Pulse amplitude measured at the secondary side of the transformer across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
10. Pulse amplitude measured at the DSX-1 Cross-Connect for all line length settings from LEN2/1/0 = 0/1/1 to LEN2/1/0 = 1/1/1.
11. Assuming that jitter free clock is input to TCLK.
12. Not production tested. Parameters guaranteed by design and characterization.
13. Measured broadband through a 0.5 Ω resistor across the secondary of the transmitter transformer during the transmission of an all ones data pattern.
14. Data decision threshold established after the receiver equalizer filters pulse overshoot and undershoot.
15. Jitter tolerance for 0 dB input signal level. Jitter tolerance increases at lower frequencies. See Figure 7.
16. See Receiver Jitter Tolerance Plot, Figure 7.

## T1 SWITCHING CHARACTERISTICS

(TA = -40°C to 85°C; TV+, RV+ = 5.0 V ±5%;
GND = 0 V; Inputs: Logic 0 = 0 V, Logic 1 = RV+; See Figures 1, 2, & 3)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| TCLK Frequency | | $f_{tclk}$ | - | 1.544 | - | MHz |
| TCLK Duty Cycle | (Note 12) | $t_{pwh2}/t_{pw2}$ | 45 | 50 | 55 | % |
| MCLK Frequency | (Note 17) | $f_{mclk}$ | - | 1.544 | - | MHz |
| RCLK Duty Cycle | (Notes 12, 18) | $t_{pwh1}/t_{pw1}$ | 45 | 50 | 55 | % |
| Rise Time, All Digital Outputs | (Note 19) | $t_r$ | - | - | 85 | ns |
| Fall Time, All Digital Outputs | (Note 19) | $t_f$ | - | - | 85 | ns |
| TPOS/TNEG to TCLK Falling Setup Time | | $t_{su2}$ | 25 | - | - | ns |
| TCLK Falling to TPOS/TNEG Hold Time | | $t_{h2}$ | 25 | - | - | ns |
| RPOS/RNEG Valid Before RCLK Falling | (Note 20) | $t_{su1}$ | 150 | 274 | - | ns |
| RPOS/RNEG Valid Before RCLK Rising | (Note 21) | $t_{su1}$ | 150 | 274 | - | ns |
| RPOS/RNEG Valid After RCLK Falling | (Note 20) | $t_{h1}$ | 150 | 274 | - | ns |
| RPOS/RNEG Valid After RCLK Rising | (Note 21) | $t_{h1}$ | 150 | 274 | - | ns |

Notes: 17. MCLK provided by an external source or TCLK.

18. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator FIFO limits are reached.

19. At max load of 1.6 mA and 50 pF.

20. Host Mode (CLKE = 1).

21. Host Mode (CLKE = 0)

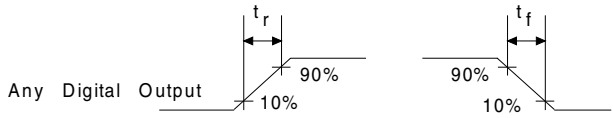



**Figure 1. Signal Rise and Fall Characteristics**

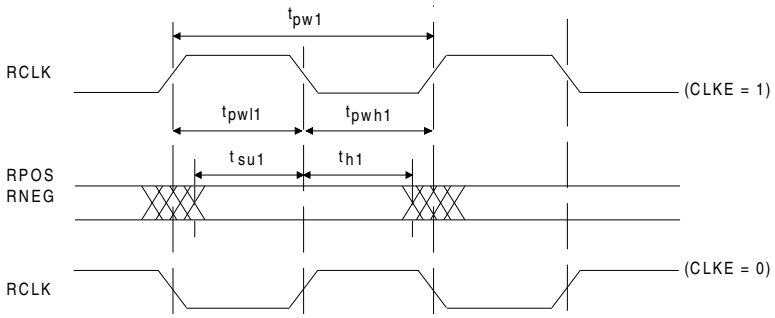



**Figure 2. Recovered Clock and Data Switching Characteristics**

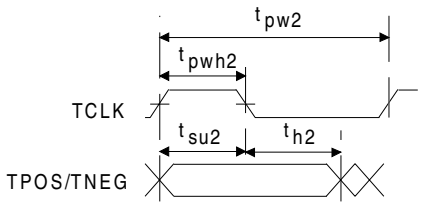



**Figure 3. Transmit Clock and Data Switching Characteristics**

## SERIAL PORT SWITCHING CHARACTERISTICS

(TA = -40° to 85°C; TV+, RV+ = 5V ±5%; Inputs: Logic 0 = 0 V, Logic 1 = RV+)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| SDI to SCLK Setup Time | $t_{dc}$ | 50 | - | - | ns |
| SCLK to SDI Hold Time | $t_{cdh}$ | 50 | - | - | ns |
| SCLK Low Time | $t_{cl}$ | 240 | - | - | ns |
| SCLK High Time | $t_{ch}$ | 240 | - | - | ns |
| SCLK Rise and Fall Time | $t_r$, $t_f$ | - | - | 50 | ns |
| $\overline{CS}$ to SCLK Setup Time | $t_{cc}$ | 50 | - | - | ns |
| SCLK to $\overline{CS}$ Hold Time | $t_{cch}$ | 50 | - | - | ns |
| $\overline{CS}$ Inactive Time | $t_{cwh}$ | 250 | - | - | ns |
| SCLK to SDO Valid (Note 22) | $t_{cdv}$ | - | - | 200 | ns |
| $\overline{CS}$ to SDO High Z | $t_{cdz}$ | - | 100 | - | ns |

Notes: 22. Output load capacitance = 50 pF

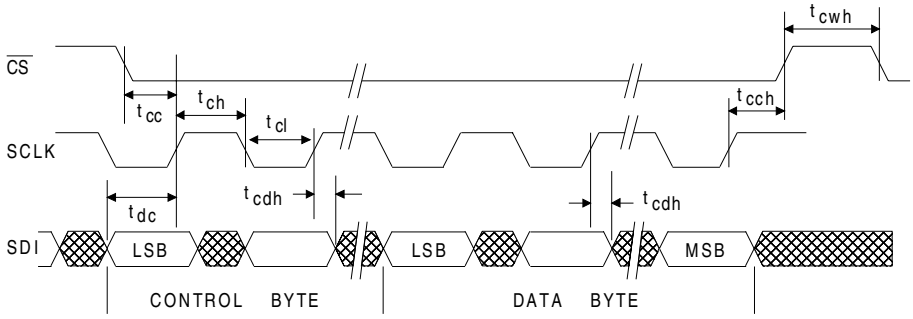



**Figure 4. Serial Port Write Timing Diagram**

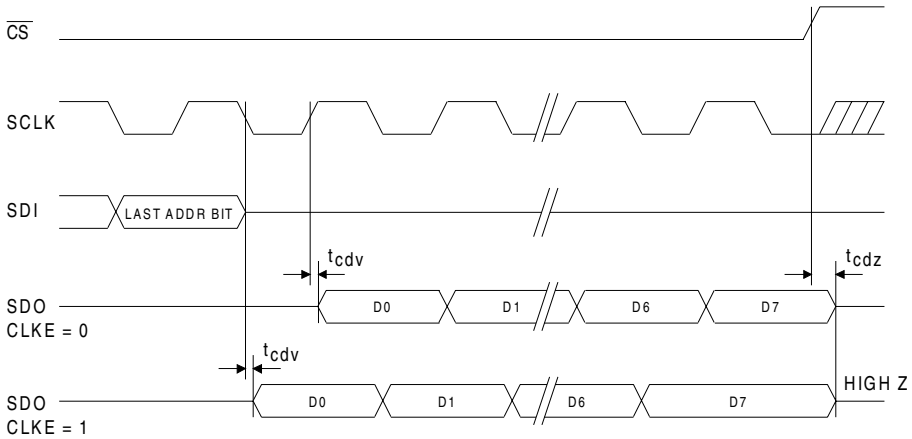



**Figure 5. Serial Port Read Timing Diagram**

## 2. THEORY OF OPERATION

The CS61310 Line Interface Unit is a fully integrated transceiver for T1 long haul applications. The transmitter outputs all pulse shapes for T1 applications.

### 2.1 Interface Modes

The CS61310 can be operated as a stand-alone device with its interface in hardware mode (MODE pin is low), or it can be operated by a microcontroller over a serial interface in host mode (MODE pin is high). Host mode enables the use of additional functionality, as described in the Serial Interface section.

### 2.2 Master Clocks

The CS61310 requires a reference clock for the receiver and the jitter attenuator. A 1.544 MHz external clock can be input to MCLK, or a 4x crystal can be connected to the on-chip oscillator. This frequency reference should be within ±32 ppm of the nominal operating frequency. Jitter and wander on the reference clock will degrade jitter attenuation and receiver jitter tolerance. If MCLK is provided, the crystal oscillator is ignored.

### 2.3 Transmitter

The transmitter accepts digital T1 input data and drives appropriately shaped AMI (Alternate Mark Inversion) pulses onto a transmission line through a transformer. The transmit data (TPOS & TNEG or TDATA) is sampled on the falling edge of the input clock, TCLK.

The pulse shapes comply with FCC Part 68 Option A (0 dB), Option B (-7.5 dB), Option C (-15 dB) or (-22.5 dB) (see Table 1). Pulse shaping and signal level are controlled by LBO1 and LBO2 pins in hardware mode, or the LBO1 and LBO2 bits (CR1.3 and CR1.4) in host mode.

Custom transmit pulse shapes may be implemented by writing pulse shape coefficients to the registers. Custom pulses may be used to correct for pulse shape degradation or distortion caused by improper termination, suboptimal interconnect wiring, or loading from external components such as high voltage protection devices.

For DS-1 applications, the arrangement in Table 1 meets ANSI T1.102 pulse shape requirements. A typical output pulse is shown in Figure 6. These pulse settings can also be used to meet ITU-T pulse shape requirements for 1.544 MHz operation.

| LBO2 | LBO1 | Output Pulse |
|---|---|---|
| 0 | 0 | 0 dB |
| 0 | 1 | -7.5 dB |
| 1 | 0 | -15 dB |
| 1 | 1 | -22.5 dB |

**Table 1. Pulse Shape Selection and Transformer Requirements**

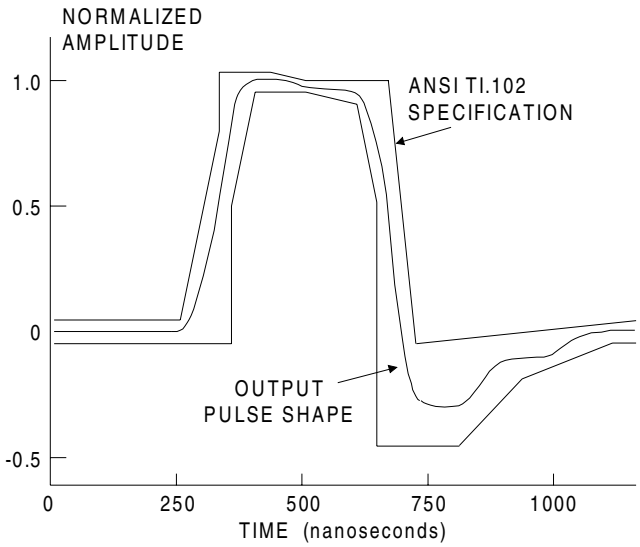



**Figure 6. Typical Pulse Shape for DS-1**

Setting TNEG high for more than 16 TCLK cycles enables the coder mode, changing TPOS to TDATA, RPOS to RDATA, and RNEG to BPV. When configured for coder mode, the MODE pin can be tied to RCLK enabling the B8ZS encoders and decoders.

The CS61310 will detect the absence of TCLK, and will force TTIP and TRING to high impedance

after 175 bit periods, preventing transmission when data input is not present. In host mode, the transmitter can be set to high impedance by setting the TxHIZ bit (CR2.1) to "1."

When any transmit control bit (TAOS, LEN0-2, LBO1-2, or LLOOP) is toggled, the transmitter outputs will require approximately 22 bit periods to stabilize. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

### 2.4 Transmit All Ones Select

The transmitter provides for all ones to be generated at TTIP and TRING. The timing of the bits is controlled by TCLK; if TCLK is absent, then MCLK is used; in the absence of MCLK, the quartz crystal generates the output timing. Transmit all ones is selected in hardware mode by setting the TAOS pin high (CR1.7 = 1 in host mode). When TAOS is active, the TPOS and TNEG (TDATA) inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

### *2.4.1 Receiver*

A noise and cross-talk filter removes signal components that are coupled onto the line from other cables. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publication 43802, Publication 43801, AT&T 62411, and TR-TSY-000170. Jitter tolerance is shown in Figure 7. The RTIP and RRING inputs are biased to an intermediate DC level and treat the input signal differentially.

The receiver extracts data and clock from the input signal. The receiver outputs are the clock and synchronized data. The incoming pulses are amplified, equalized and filtered before being fed to the comparator for peak detection, slicing and data recovery.

### *2.4.2 Clock Recovery*

The clock recovery circuit is a third-order phase-locked loop. The digital PLL in the clock recovery circuit of the CS61310 recovers clock from the edges of the incoming pulses (1's). The clock and data recovery circuit is tolerant of long strings of consecutive zeros, and will successfully receive a 1-in-175, jitter-free input signal.

In the hardware mode, data on RPOS and RNEG (RDATA), is stable and latched on the rising edge of recovered clock, RCLK. In host mode, the CLKE pin determines the clock polarity for which output data is stable and valid (see Table 2). When CLKE is high, RPOS and RNEG (RDATA) are valid on the falling edge of RCLK. When CLKE is low, RPOS and RNEG are valid on the rising edge of RCLK.

| MODE | CLKE | DATA | CLOCK | Clock Edge for Valid Data |
|---|---|---|---|---|
| LOW | Don't Care | RPOS<br>RNEG | RCLK | Rising |
| HIGH | LOW | RPOS<br>RNEG<br>SDO | RCLK<br>RCLK<br>SCLK | Rising<br>Rising<br>Falling |
| HIGH | HIGH | RPOS<br>RNEG<br>SDO | RCLK<br>RCLK<br>SCLK | Falling<br>Falling<br>Rising |

**Table 2. Data Output/Clock Relationship**

Setting TNEG high for more than 16 TCLK cycles enables the coder mode, changing TPOS to TDATA, RPOS to RDATA, and RNEG to BPV. When configured for coder mode, the MODE pin can be tied to RCLK enabling the B8ZS encoders and decoders.

### *2.4.3 Jitter Tolerance*

The receiver jitter tolerance is shown in Figure 7. The CS61310 jitter tolerance exceeds AT&T 62411 for synchronizers.

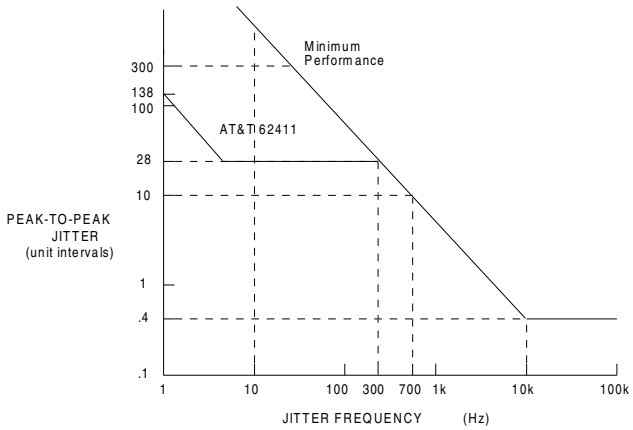



**Figure 7. Minimum Input Jitter Tolerance of Receiver**

### 2.5 Jitter Attenuator

Jitter attenuation can be implemented in either the transmit (JASEL low) or receive (JASEL high) paths, or it can be eliminated from the circuit by setting the XTALIN pin high. The jitter attenuator on the CS61310 does not require a crystal. It is activated when XTALIN is either connected to ground or left open; connecting to ground is the preferred method.

The jitter attenuator corner frequency is set at 4 Hz, with attenuation increasing at a 20 dB per decade rate above 4 Hz. A typical jitter attenuation graph is shown in Figure 8.

### 2.6 Receiver Line Attenuation Indication

The LATN pin outputs a coded signal that represents the signal level at the input of the receiver. As shown in Figure 9, the LATN output is measured against RCLK to provide the signal level in 7.5 dB increments. In host mode, the receive input signal level can be read from the Equalizer Gain register, address 0x12, to greater resolution, dividing the input range into 20 steps of 2 dB increments.

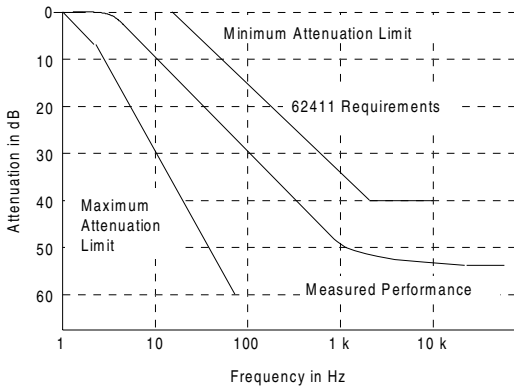



**Figure 8. Typical Jitter Transfer Function**

### 2.7 Receiver Loss of Signal

The receiver will indicate loss of signal by setting the LOS pin high in hardware mode (CR1.0 = 1 in host mode). LOS is active on power up, reset, when receiver gain is maximized, upon receiving 175+/-15 consecutive zeros, or when the received signal power falls below below the signal level, “Loss of Signal Threshold” listed under Analog Specifications. Received zeros are counted based on recovered clock cycles. While in the LOS state, received data on RPOS/RNEG (RDATA in unipolar mode) equals 0 (squelched). The device complies with ANSI T1.231-1993 criteria to exit the LOS condition: 12.5% ones density for 175+/-75 bit periods with no more than 100 consecutive zeros.

While LOS is active, RCLK depends on MCLK and the jitter attenuator. If the jitter attenuator is in the transmit path or not used, RCLK is referenced to MCLK, if provided, or the crystal oscillator otherwise. If the jitter attenuator is in the receive path, the jitter attenuator will hold the average incoming data frequency prior to LOS. The recovered clock remains at a 50% duty cycle. The RPOS (RDATA) and RNEG pins are forced low during LOS.

Timing is recovered by a phase selector which selects one of the phases from the internal synchronization clock (one of three clocks, 120 degrees apart in phase, at 16X of the data rate). Since the selection is made between a limited set of phases, the Digital Timing Recovery process has a small phase error built into the sampling process. By choosing from 48 possible sampling phases, the CS61310 reduces the sampling error to a minimum.

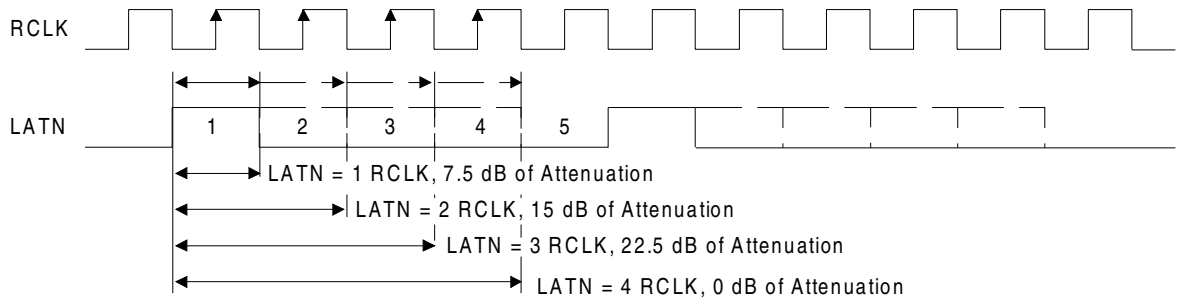



**Figure 9. LATN Pulse Width encoding**

### 2.8 Local Loopback

In hardware mode, local loopback is selected by setting the LLOOP pin high (CR1.6 = 1 in host mode). Selecting local loopback causes clock and data presented on TCLK, TPOS/TNEG (TDATA) to be output at RCLK, RPOS/RNEG (RDATA). Local loopback disconnects the RTIP/RRING inputs from the line. Inputs to the transmitter are still transmitted on TTIP and TRING, unless TAOS has been selected in which case, AMI-encoded continuous ones are transmitted at the TCLK frequency. The receiver RTIP and RRING inputs are ignored when local loopback is in effect.

### 2.9 Remote Loopback

Remote loopback is selected by setting the RLOOP pin high in hardware mode (CR1.5 = 1 in host mode). In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. Selecting remote loopback overrides a TAOS request. The recovered clock is also sent to RCLK, and the recovered data is also sent to RPOS and RNEG in bipolar mode, or RDATA in unipolar mode. Simultaneous selection of local and remote loopback modes will cause a device reset to occur (see Reset).

### 2.10 Network Loopback

Network Loopback (automatic remote loopback) can be commanded from the network when the Network Loopback detect function is enabled. In Host Mode, Network Loopback (NLOOP) detection is enabled by writing ones to TAOS, LLOOP, and RLOOP, then clearing these three bits on a successive write cycle. In hardware mode, Network Loopback can be enabled by tying RLOOP to RCLK or by setting TAOS, LLOOP, and RLOOP high for at least 200 ns, and then low. Once enabled Network Loopback functionality will remain in effect until RLOOP is activated or the device is reset.

When NLOOP detection is enabled, the receiver monitors the input data stream for the NLOOP data patterns (00001 = enable, 001 = disable). When an NLOOP enable data pattern is repeated for a minimum of five seconds (with less than 10E-3 BER), the device initiates a remote loopback. Once Network Loopback detection is enabled and activated by the NLOOP data pattern, the loopback is identical to Remote Loopback initiated at the device. NLOOP is reset if the disable pattern (001) is received for 5 seconds, or by activation of RLOOP. NLOOP is temporarily suspended by LLOOP, but the NLOOP state is not reset.

### 2.11 Alarm Indication Signal

The receiver sets the register bit, AIS, to “1” when less than 9 zeros are detected out of 8192 bit periods. AIS returns to “0” upon the first read after the AIS condition is removed, determined by 9 or more zeros out of 8192 bit periods.

### 2.12 Serial Interface

In the Host Mode, pins 24 through 28 serve as a microcontroller interface. On-chip registers can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through these registers, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 2. Data transfers are terminated by setting CS high. CS may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output and set SDO to high impedance.

Figure 10 shows the timing relationships for data transfers when CLKE = 0. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle. When CLKE = 0, data bit D7 is held valid until the rising edge of the 17th clock cycle. SDO goes high-impedance after $\overline{CS}$ goes high or at the end of the hold period of data bit D7.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bi-directional I/O port.

An address/command byte, shown in Figure 10, points to addresses 0x10 through 0x15 (address 0x10 shown), and precedes a data byte. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The last bit is ignored. Data to the internal registers is input on the eight clock cycles immediately following the address/command byte.

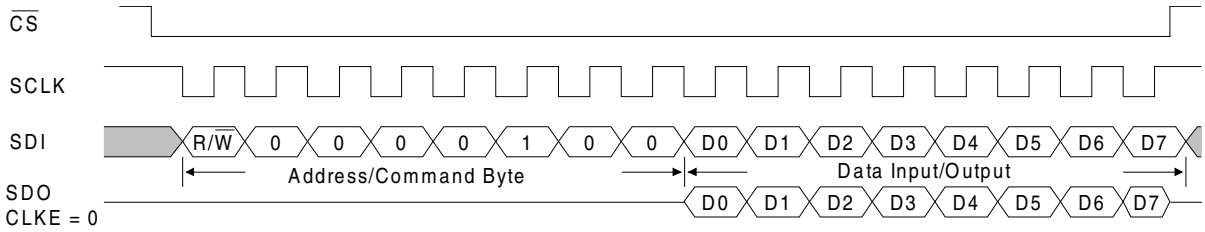



**Figure 10. Input/Output Timing (showing address 0x10)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR |
|---|---|---|---|---|---|---|---|---|---|
| Control Register 1 (CR1) | TAOS | LLOOP | RLOOP | LB02 | LB01 | CODER TAZ | NLOOP | LOS | 0x10 R/W |
| Control Register 2 (CR2) | AIS | RAMPLSE | RSVD set to "0" | LOOPDN | LOOPUP | RPWDN | TxHIZ | RSVD set to "0" | 0x11 R/W |
| Equalizer Gain (EQGAIN) | X | X | X | EQ4 | EQ3 | EQ2 | EQ1 | EQ0 | 0x12 R |
| RAM Address (RAM) | MSB | - | - | - | - | - | - | LSB | 0x13 R/W |
| Reserved Set to "0" | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x14 |

**Table 3. Register Map**

### 2.13 Control Register 1: Address 0x10

| 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|---|---|---|---|---|---|---|---|
| TAOS | LLOOP | RLOOP | LBO2 | LBO1 | CODER TAZ | NLOOP | LOS |

TAOS — Transmit All Ones Select
When TAOS = 1, all ones are transmitted at the TCLK frequency

LLOOP — Local Loopback
When LLOOP = 1, data input at TPOS, TNEG (TDATA) is internally looped back and output on RPOS, RNEG (RDATA). TCLK is routed to RCLK, through the jitter attenuator, if activated.

RLOOP — Remote Loopback
When RLOOP = 1, clock and data recovered by the receiver are sent back through the transmit path and retransmitted. The clock and data are routed through the jitter attenuator, if activated.

LBO2, 1 — Line BuildOut

| LBO2 | LBO1 | Attenuation |
|---|---|---|
| 0 | 0 | 0 dB |
| 0 | 1 | -7.5 dB |
| 1 | 0 | -15 dB |
| 1 | 1 | -22.5 dB |

CODER — Zero Substitution (valid only when TNEG (UBS) is tied high, invoking coder mode).

(TAZ) — Setting CODER to “1” enables B8ZS encoding and decoding.
When not in coder mode (TPOS/TNEG are data inputs) setting TAZ to “1” causes all zeros to be transmitted.

NLOOP — Network Loopback
NLOOP = 1 when a network loopback code has been detected on the received signal.
An interrupt will occur when NLOOP changes state unless a “1” is written to NLOOP disabling the interrupt.

LOS — Loss Of Signal
LOS = 1 when the loss of signal criteria have been met (175 zeros).
LOS = 0 when a valid signal is being received.
An interrupt will occur when LOS changes state unless a “1” is written to LOS disabling the interrupt.

### 2.14 Control Register 2: Address 0x11

| 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|---|---|---|---|---|---|---|---|
| AIS | RAMPLSE | RSVD set to “0” | LOOPDN | LOOPUP | RPWDN | TxHIZ | RSVD set to “0” |

AIS — Alarm Indication Signal.
AIS = 1 when an all ones pattern is present at the receiver. This bit is reset to “0” by the first read occurring after the AIS condition has cleared.
An interrupt will occur when AIS is present unless a “1” is written to AIS disabling the interrupt.

RAMPLSE — When RAMPLSE = 1, output pulse shapes are determined by the codes in the internal, programmable, transmit RAM.

LOOPDN — Loop Down
Setting LOOPDN to “1” causes the data pattern 001... to be repetitively transmitted.

LOOPUP — Loop Up
Setting LOOPUP to "1" causes the data pattern 00001... to be repetitively transmitted.

RPWDN — Receiver Power Down
When RPWDN = 1, the receiver circuitry is powered down, but the transmitter is still active.

TxHIZ — Transmitter High Impedance
When TxHIZ = 1 the transmitter goes to a low-power, high-impedance state

RSVD — Reserved. Set to 0 for proper operation.

### *2.15 Equalizer Gain (EQGAIN): Address 0x12*

| 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|---|---|---|---|---|---|---|---|
| X | X | X | EQ4 | EQ3 | EQ2 | EQ1 | EQ0 |

EQ[4:0] — The receive equalizer gain settings are broken down into 20 segments and provided at the five LSBs of this register, EQ4 - EQ0. 00001 corresponds to -2 dB, 10100 corresponds to -40 dB. The three MSBs are don't cares.

### *2.16 RAM Address (RAM): Address 0x13*

| 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|---|---|---|---|---|---|---|---|
| RAM.7 | RAM.6 | RAM.5 | RAM.4 | RAM.3 | RAM.2 | RAM.1 | RAM.0 |

RAM[7:0] — The RAM address pointer for the arbitrary waveform memory;
a special write procedure must be followed to write the waveform RAM.

### 2.17 Interrupts

An interrupt will occur ($\overline{\text{INT}}$ pulls low) in response to a change in the LOS, AIS or NLOOP bits. The interrupt is cleared when the host processor writes a "1" to the respective bit in the control register.

Writing a "1" to LOS or NLOOP over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).

2) Output data bits 5, 6 and 7 will be reset as appropriate.

3) Interrupts for the corresponding LOS and NLOOP will be prevented from occurring.

Writing a "0" to either LOS or NLOOP enables the corresponding interrupt for LOS and NLOOP. Reading the registers returns their current status or setting. Register 16 outputs the status NLOOP and LOS and has bits 5, 6, and 7 encoded as shown in Table 4.

Writing the arbitrary waveform RAM requires a deviation from normal serial port access. Register 19 is the RAM address register for the arbitrary waveform. Two consecutive address bytes are written; first the Address/Command Byte is written to address 0x13, followed by the address in RAM to be written. This dual address is then followed by the data byte for the waveform amplitude. There are 42 RAM byte locations (numbered h00 to h29).

| Bits | | | Status |
|---|---|---|---|
| 7 | 6 | 5 | |
| 0 | 0 | 0 | Reset has occurred, or no program input |
| 0 | 0 | 1 | RLOOP active |
| 0 | 1 | 0 | LLOOP active |
| 0 | 1 | 1 | LOS has changed state since last Clear LOS occurred |
| 1 | 0 | 0 | TAOS active |
| 1 | 0 | 1 | NLOOP has changed state since last Clear NLOOP occurred |
| 1 | 1 | 0 | TAOS and LLOOP active |
| 1 | 1 | 1 | LOS and NLOOP have both changed state since last Clear NLOOP and Clear LOS |

**Table 4. Register 16 Decoding**

### 2.18 Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately 3 Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the transmit and receive sections commences. Because power up conditions can vary considerably, it is recommended that the device be reset after the power supply has stabilized to ensure a known initial operational condition.

The internal frequency generators can be calibrated only if a reference clock is present. The reference clock for the transmitter is provided by TCLK. The reference for the receiver is either the crystal oscillator or MCLK. If both the oscillator and MCLK are active, MCLK will be used as the reference source. The initial calibration should take less than 20 ms after pulses are input to the receiver.

In operation, the device is continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface when in operation. However, a reset function is available which will reinitiate calibration and clear all registers and clear the Network Loopback function.

In Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. The reset will set all registers to “0” and initiate a calibration.

In Hardware Mode, the CS61310 is reset by simultaneously setting RLOOP and LLOOP high for at least 200 ns. Hardware reset will clear Network Loopback functionality

### 2.19 Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should decoupled to their respective grounds.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 47µF tantalum and 1.0µF mylar or ceramic capacitor should be connected between TV+ and TGND, and a 0.1µF mylar or ceramic capacitor should be connected between RV+ and RGND. Place capacitors as closely as possible to their respective power supply pins. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

## 3. ARBITRARY WAVEFORM GENERATION

In addition to the predefined pulse shapes, the user can create custom pulse shapes using the host mode. This flexibility allows the board designer to accommodate non-standard cables, EMI filters, protection circuitry, etc.

The arbitrary pulse shape of mark (a transmitted “1”) is specified by describing it's pulse shape across three Unit Intervals (UIs). This allows, for example, the long haul return-to-zero tail to extend into the next UI, or two UIs, as is required for isolated pulses.

Each UI is divided into multiple phases, and the users defines the amplitude of each phase. The waveform of a space (a transmitted “0”) is fixed at zero volts. Examples of the phases are shown in Figure 11. In all cases, to define an arbitrary waveform, the user writes to the Waveform Register either 36, 39 or 42 times (12, 13 or 14 phases per UI for three UIs). The phases are written in the order: UI1/phase1, UI1/phase2, ... , UI1/phase14, UI2/phase1, ... , UI2/phase14, UI3/phase1, ... , UI3/phase14.

For DSX-1 and DS1 applications, the CS61310 divides the 648 ns UI into 13 uniform phases (49.8 ns each), and will ignore the phase amplitude information written for phase 14 of each UI.

When transmitting pulses, the CS61310 will add the amplitude information from the prior two symbols with the amplitude of the first UI of the current symbol before outputting a signal on TTIP/TRING. Therefore, a mark preceded by two spaces will be output exactly as the mark is programmed. However, when one mark is preceded by marks, the first portion of the last mark may be modified. With AMI data, where successive pulses have opposite polarity, the undershoot tail of one pulse will cause the rising edge of the next mark to rise more quickly, as shown in Figure 12.

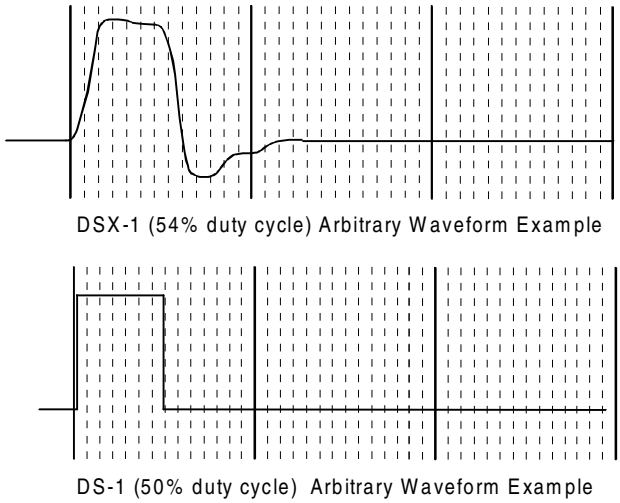



**Figure 11. Phase Definition of Arbitrary Waveforms**

The amplitude of each phase is described by a 7-bit, 2's complement number, where a positive value describes pulse amplitude, and a negative value describes pulse undershoot. The positive full value is hex 3F. The negative full value is hex 40. For T1, the typical output voltage is 38 mV/LSB (peak voltage across the TTIP and TRING outputs).

On the secondary of a 1:2 step-up transformer, the mV/LSB is twice the values stated above. Note that although the full scale digital input is 3F, it is recommended that full scale output voltage on the transformer primary be limited to 2.4 Vpk. At higher output voltages, the driver may not drive the requested output voltage.

The amplitude information for all phases is written via the serial-port to Arbitrary Pulse Shape registers as described in an earlier section. Each phase

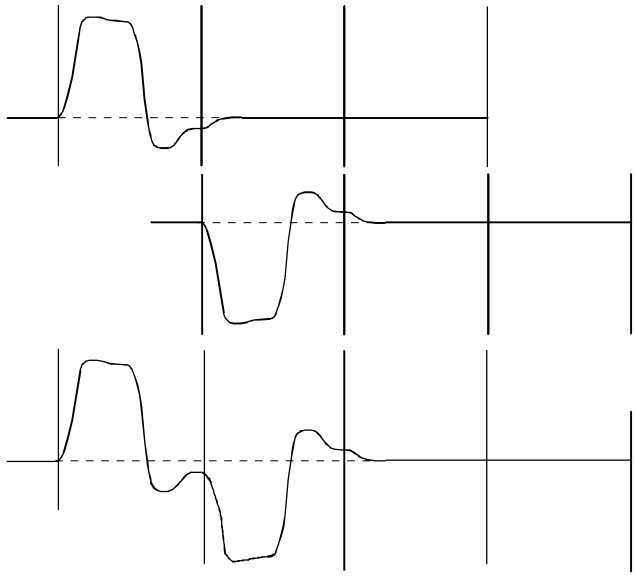


**Figure 12. Example of Summing of Waveforms**

amplitude is written as an eight-bit byte, where the first phase of the symbol is written first.

In serial-port host mode, the amplitude bytes are written LSB first. The contents of the Arbitrary Waveform register can be verified by reading the Waveform Register.

| Diagnostic Mode | Availability (Note 1) H/W | Availability (Note 1) Host | Host Mode (Note 2) Maskable |
|---|---|---|---|
| ***Loopback Modes*** | | | |
| Local Loopback (LLOOP) | Yes | Yes | No |
| Remote Loopback (RLOOP) | Yes | Yes | No |
| In-band Network Loopback (NLOOP) | Yes | Yes | Yes |
| ***Internal Data Pattern Generation and Detection*** | | | |
| Transmit All Ones (TAOS) | Yes | Yes | No |
| In-band Loop-up/down Code Generator | No | Yes | No |
| ***Error Detection*** | | | |
| Bipolar Violation Detection (BPV) | Yes | Yes | No |
| ***Alarm Condition Monitoring*** | | | |
| Receive Loss of Signal Monitoring (LOS) | Yes | Yes | Yes |
| Receive Alarm Indication Signal Monitoring (AIS) | No | Yes | Yes |
| ***Other Diagnostic Reports*** | | | |
| Receive Line Attenuation Indicator (LATN) | Yes | Yes | No |

**Table 5. CS61310 Diagnostic Mode Availability**

Notes: 1. In Hardware Mode the Diagnostic Modes are selected by directly setting the pins on the device; in Host Mode, the appropriate register bits are written for Diagnostic Modes.

2. In Host Mode the interrupts can be masked by writing a “1” to the LOS bit; there is no masking in the Hardware Mode.

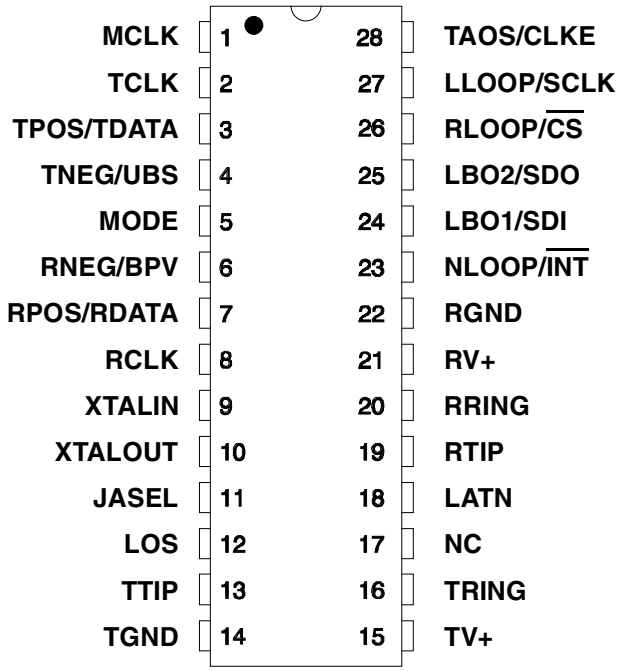
| | |
|---|---|
| Turns ratio | 1:1.5, 1:2 step-up transmit, 1:1 receive |
| Primary inductance | 1.2 mH min at 772 kHz |
| Primary leakage inductance | 0.5 µH max at 772 kHz with secondary shorted |
| Secondary leakage inductance | 0.5 µH max at 772 kHz |
| Interwinding capacitance | 40 pF max, primary to secondary |
| ET-constant | 16 V-µs min |

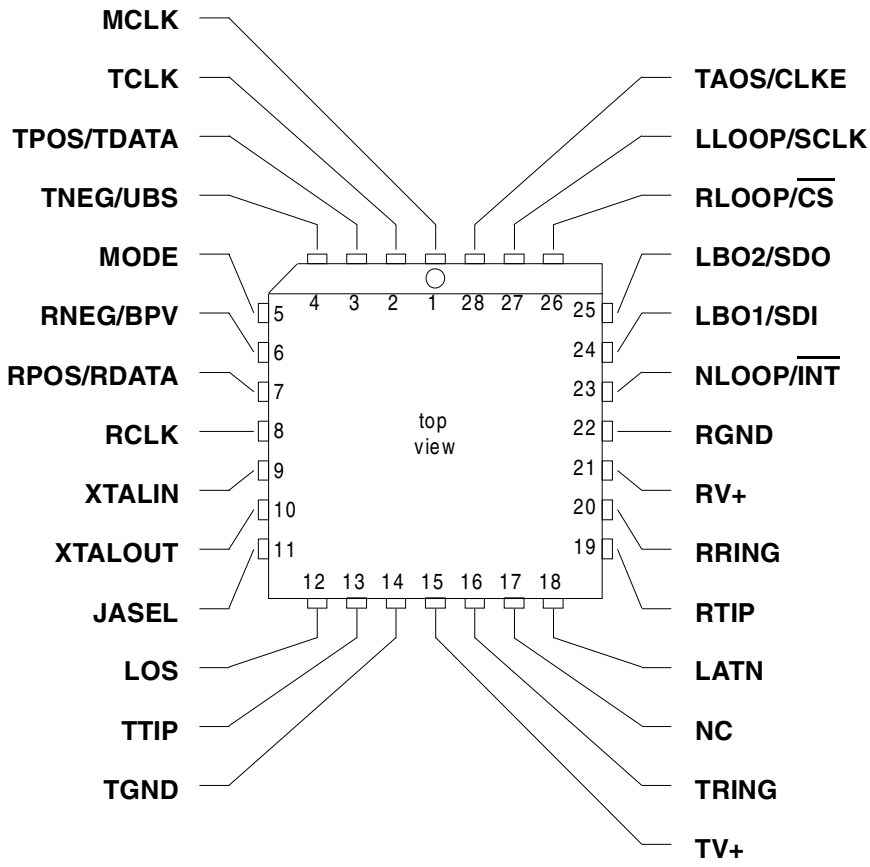
**Table 6. Transformer Specification**

| Turns Ratio(s) | Manufacturer | Part Number | Package Type |
|---|---|---|---|
| 1:1CT | Pulse Engineering | PE-64936 | 1.5 kV, through-hole, single |
| | Valor | PT5008 | |
| | Schott | 67130840 | |
| | Valor | ST5085 | 1.5 kV, surface mount, single |
| | Schott | 31187 | |
| 1:2CT | Pulse Engineering | PE-65351 | 1.5 kV, through-hole, single |
| | Valor | PT5004 | |
| | Schott | 617130850 | |
| | Valor | ST5086 | 1.5 kV, surface mount, single |
| | Schott | 31188 | |
| 1:1.5CT | Pulse Engineering | T-1054 | 1.5 kV, through-hole, single |
| | Schott | 31705 | |
| | Valor | ST5074 | 1.5 kV, surface mount, single |
| | Schott | 31706 | |
| 1:1CT<br>1:2CT | Pulse Engineering | PE-68678 | 1.5 kV, surface mount, dual |
| | Valor | ST5162 | |
| | Pulse Engineering | PE-68877 | 1.5 kV, surface mount, dual extended temp. |
| | Pulse Engineering | T-1068 | 1.5 kV, surface mount, quad port |
| | Valor | ST5173 | |
| | Pulse Engineering | T-1031 | 3 kV, surface mount, dual |
| 1:1CT<br>1:1.5CT | Pulse Engineering | T-1022 | 1.5 kV, surface mount, dual |
| | Valor | ST5221 | |
| | Pulse Engineering | T-1077 | 1.5 kV, surface mount, dual extended temp |
| | Pulse Engineering | T-1081 | 3 kV, surface mount, dual |

**Table 7. Recommended Tranformers for the CS61310**

## 4. PIN DESCRIPTION



*Power Supplies*

### TGND - Ground Transmit Driver, Pin 14.

Power supply ground for the transmit driver; typically 0 Volts.

### TV+ - Power Supply, Transmit Driver, Pin 15.

Power supply for the transmit driver; typically +5 Volts.

### RV+ - Power Supply, Pin 21.

Power supply for all subcircuits except the transmit driver; typically +5 Volts.

### RGND - Ground, Pin 22.

Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

*Oscillator*

### XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz crystal can be connected across these pins. This oscillator provides the reference frequency for the LIU if MCLK is not provided. The load capacitance presented to the crystal by these pins should be approximately 19pF (IC and package, when soldered into a circuit board). The jitter attenuator may be disabled by tying XTALIN to RV+ through a 1kΩ resistor, and floating XTALOUT. When pin 9 has no clock input, a clock must be supplied to the MCLK pin. Alternatively an external 6.176 MHz clock can be driven into XTALIN, and the jitter attenuator circuit will operate.

If MCLK is provided, and XTALIN is tied low or left floating, the jitter attenuator will be enabled.

*Control*

### MCLK - Master Clock Input, Pin 1.

Either MCLK or the crystal oscillator provide the master frequency reference for the CS61310. If both MCLK and the crystal oscillator are present, the oscillator is ignored. MCLK should be 1.544 MHz. If MCLK is not used, it must be grounded.

### MODE - Mode Select Input, Pin 5.

Setting the MODE pin high puts the CS61310 into Host Mode where the device is controlled by a microprocessor, via a serial port. Setting the MODE pin low, configures the part for hardware mode control where various control and status are provided on dedicated pins. The MODE pin is internally pulled down placing the part in Hardware Mode when this pin is left floating. Tying the MODE pin to RCLK places the chip in Hardware Mode and enables the B8ZS encoder/decoder (provided that coder mode has been enabled; see the description for TNEG/UBS pin).

### JASEL - Jitter Attenuator Select, Pin 11.

If the jitter attenuator is enabled (crystal oscillator active, or XTALIN tied low or left floating with MCLK provided), setting JASEL high places the jitter attenuator in the receive path; setting JASEL low places the jitter attenuator in the transmit path.

### NC - No Connect, Pin 17.

The input voltage to this pin does not effect normal operation.

### LBO1, LBO2 - Line Build Out 1 and 2, Pins 24 and 25 (Hardware Mode).

Transmitted line build out pulse shapes are selected by setting LBO1/2: 0/0 = 0 dB, 0/1 = -7.5 dB, 1/0 = -15 dB, and 1/1 = -22.5 dB.

### RLOOP - Remote Loopback Input, Pin 26 (Hardware Mode).

Setting RLOOP to a logic 1 causes the received signal to be passed through the jitter attenuator (if active) and retransmitted onto the line. The internal encoders/decoders will be bypassed in Remote Loopback. Simultaneously setting RLOOP and LLOOP high while TAOS is low resets the CS61310. Simultaneously setting RLOOP, LLOOP and TAOS high enables Network Loopback detection.

### LLOOP - Local Loopback Input, Pin 27(Hardware Mode).

Setting LLOOP to a logic 1 internally routes the transmitter input to the receiver output. If TAOS is low, the signal being output from the transmitter will be internally routed to the receiver inputs allowing nearly the entire chip to be tested. If TAOS and LLOOP are set high at the same time, the local loopback will occur at the jitter attenuator (excluding the transmit and receive circuitry) and the transmitter will transmit all ones. Simultaneously setting RLOOP and LLOOP high while TAOS is low resets the CS61310. Simultaneously setting RLOOP, LLOOP and TAOS high enables Network Loopback detection.

### TAOS - Transmit All Ones Select Input, Pin 28 (Hardware Mode).

Setting TAOS to logic 1 causes continuous ones to be transmitted at the TCLK frequency. When TAOS is high, TPOS and TNEG (TDATA) are not output at the TTIP/TRING pins. TAOS is overridden by Remote Loopback. Setting TAOS, LLOOP, and RLOOP high simultaneously enables Network Loopback detection.

*Status*

### LOS - Loss Of Signal Output, Pin 12.

LOS goes high when 175 consecutive zeros are received. LOS returns low when the ones density reaches 12.5% (based on 175 consecutive bit periods, starting with a one and containing less than 100 consecutive zeros, as prescribed in ANSI T1.231-1993).

### LATN - Line Attenuation Indication Output, Pin 18.

LATN is an encoded output that indicates the receive equalizer gain setting in relation to a five RCLK cycle period. If LATN is high for one RCLK cycle, the equalizer is set for 7.5 dB gain, two cycles = 15 dB gain, three cycles = 22.5 dB gain, four cycles = 0 dB. LATN may be sampled on the rising edge of RCLK.

### NLOOP - Network Loopback Output, Pin 23 (Hardware Mode).

NLOOP goes high when a 00001 pattern is received for five seconds putting the CS61310 into network (remote) loopback. Network loopback is deactivated upon receipt of a 001 pattern for five seconds, or by the selection of RLOOP. Network loopback is temporarily suspended with LLOOP, but the state of the NLOOP pin does not change.

*Serial Control Interface*

### $\overline{\text{INT}}$ - Interrupt Output, Pin 23 (Host Mode).

$\overline{\text{INT}}$ pulls low to flag the host processor when NLOOP, AIS or LOS changes state. $\overline{\text{INT}}$ is an open drain output and should be tied to the supply through a resistor.

### SDI - Serial Data Input, Pin 24 (Host Mode).

Data input to the on-chip register is sampled on the rising edge of SCLK.

### SDO - Serial Data Output, Pin 25 (Host Mode).

Status and control information are output from the on-chip register on SDO. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low, SDO is valid on the falling edge of SCLK. SDO goes to a high-impedance state when the serial port is being written to, or after bit D7 is output or $\overline{CS}$ goes high (whichever occurs first).

### $\overline{CS}$ - Chip Select, Pin 26 (Host Mode).

The serial interface is accessible when $\overline{CS}$ transitions from high to low.

### SCLK - Serial Clock Input, Pin 27 (Host Mode).

SCLK is used to write or read data bits to or from the serial port registers.

### CLKE - Clock Edge Input, Pin 28 (Host Mode).

Setting CLKE to logic 1 causes RPOS and RNEG (RDATA) to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG (RDATA) to be valid on the rising edge of RCLK and SDO to be valid on the falling edge of SCLK.

*Data Input/Output*

### TCLK - Transmit Clock Input, Pin 2.

The 1.544 MHz transmit clock is input on this pin. TPOS and TNEG or TDATA are sampled on the falling edge of TCLK.

### TPOS/TNEG - Transmit Positive Pulse, Transmit Negative Pulse, Pins 3 and 4.

Data input to TPOS and TNEG is sampled on the falling edge of TCLK and transmitted onto the line at TTIP and TRING. An input on TPOS results in transmission of a positive pulse; an input on TNEG results in transmission of a negative pulse. If TNEG, pin 4, is held high for 16 TCLK cycles, the CS61310 reconfigures for unipolar (single pin NRZ) data input at pin 3, TDATA. If TNEG goes low the CS61310 switches back to two-pin bipolar data input format.

### TDATA - Transmit Data, Pin 3.

When pin 4, TNEG/UBS, is held high, pin 3 becomes TDATA, a single-line NRZ (unipolar) data input sampled on the falling edge of TCLK.

### UBS - Unipolar / Bipolar Select, Pin 4.

When UBS is held high for 16 consecutive TCLK cycles (15 consecutive bipolar violations) the CS61310 reconfigures for unipolar (single-line NRZ) data input / output format. Pin 3 becomes TDATA, pin 7 becomes RDATA, and pin 6 becomes BPV.

### NEG/RPOS - Receive Negative Pulse, Receive Positive Pulse, Pins 6 and 7.

Recovered data output on RPOS and RNEG is stable and valid on the rising edge of RCLK in Hardware Mode. In Host Mode, CLKE determines the edge of RCLK on which RPOS and RNEG are valid. A positive pulse on RTIP with respect to RRING generates a logic 1 on RPOS; a positive pulse on RRING with respect to RTIP generates a logic 1 on RNEG.

### BPV - Bipolar Violation, Pin 6.

When pin 4 (TNEG/UBS) is held high, received bipolar violations are flagged by BPV (RNEG) going high along with the offending bit output from RDATA. If the B8ZS encoder/decoder is activated, BPV will not flag bipolar violations resulting from valid zero substitutions.

### RRDATA - Received Data, Pin 7.

Unipolar data (single-line NRZ) data is output on RDATA when pin 4, TNEG/UBS, is held high.

### RCLK - Recovered Clock Output, Pin 8.

RCLK outputs the clock recovered from the input signal at RTIP and RRING. In a Loss of Signal state RCLK is driven either by MCLK or the crystal oscillator, or retains the frequency prior to the LOS state, depending on the clocks provided. While LOS is true, RCLK will be driven either by MCLK or the crystal oscillator. If the jitter attenuator is in the receive path, RCLK will make a smooth transition to the LOS timing. RCLK will remain at its frequency prior to LOS.

### RTIP,RRING - Receive Tip, Receive Ring, Pins 19,20.

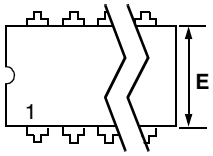
The B8ZS signal received from the line is input via these pins. A 1:1 transformer and appropriate matching resistors are required as shown in the applications section. Data and clock recovered from the signal input on these pins is output via RPOS, RNEG, and RCLK.

### TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13,16

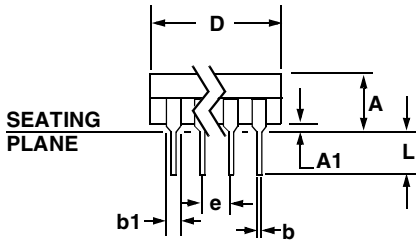
These pins are the output of the differential transmit driver. The transformer and matching resistors can be chosen to give the desired pulse height (see Application Schematics)

## 5. PACKAGE DIMENSIONS

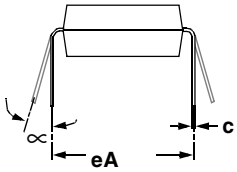
### 28 PIN PLASTIC (PDIP) PACKAGE DRAWING




TOP VIEW




BOTTOM VIEW

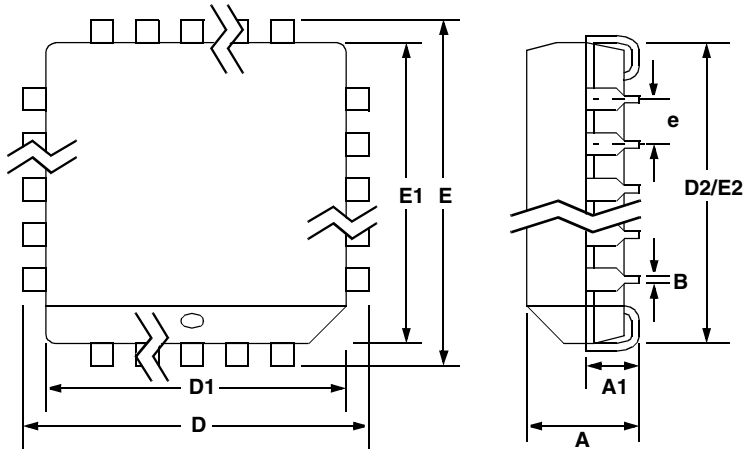



SIDE VIEW

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.155 | 0.200 | 3.94 | 5.08 |
| A1 | 0.020 | 0.040 | 0.51 | 1.02 |
| b | 0.014 | 0.022 | 0.36 | 0.56 |
| b1 | 0.040 | 0.065 | 1.02 | 1.65 |
| c | 0.008 | 0.015 | 0.20 | 0.38 |
| D | 1.435 | 1.465 | 36.45 | 36.83 |
| E | 0.540 | 0.560 | 13.72 | 14.22 |
| e | 0.095 | 0.105 | 2.41 | 2.67 |
| eA | 0.600 | 0.625 | 15.24 | 15.87 |
| L | 0.125 | 0.150 | 3.18 | 3.81 |
| ∝ | 0° | 15° | 0° | 15° |

1. Positional tolerance of leads shall be within 0.25 mm (0.010 in.) at maximum material condition, in relation to seating plane and each other.
2. Dimension eA to center of leads when formed parallel.
3. Dimension E does not include mold flash.

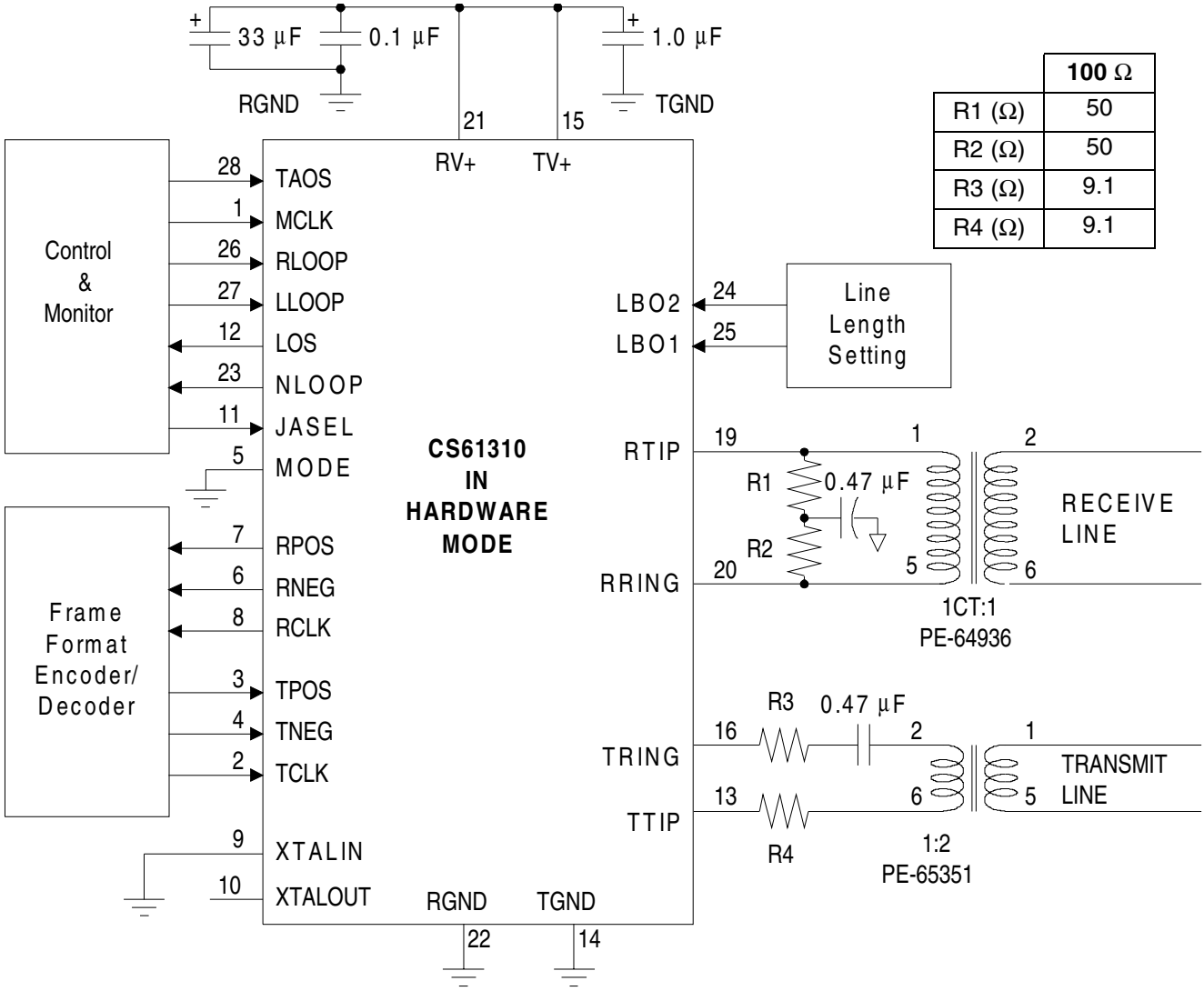
## 28L PLCC PACKAGE DRAWING




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.165 | 0.180 | 4.043 | 4.572 |
| A1 | 0.090 | 0.120 | 2.205 | 3.048 |
| B | 0.013 | 0.021 | 0.319 | 0.533 |
| D | 0.485 | 0.495 | 11.883 | 12.573 |
| D1 | 0.450 | 0.456 | 11.025 | 11.582 |
| D2 | 0.390 | 0.430 | 9.555 | 10.922 |
| E | 0.485 | 0.495 | 11.883 | 12.573 |
| E1 | 0.450 | 0.456 | 11.025 | 11.582 |
| E2 | 0.390 | 0.430 | 9.555 | 10.922 |
| e | 0.040 | 0.060 | 0.980 | 1.524 |

***JEDEC #: MS-018***

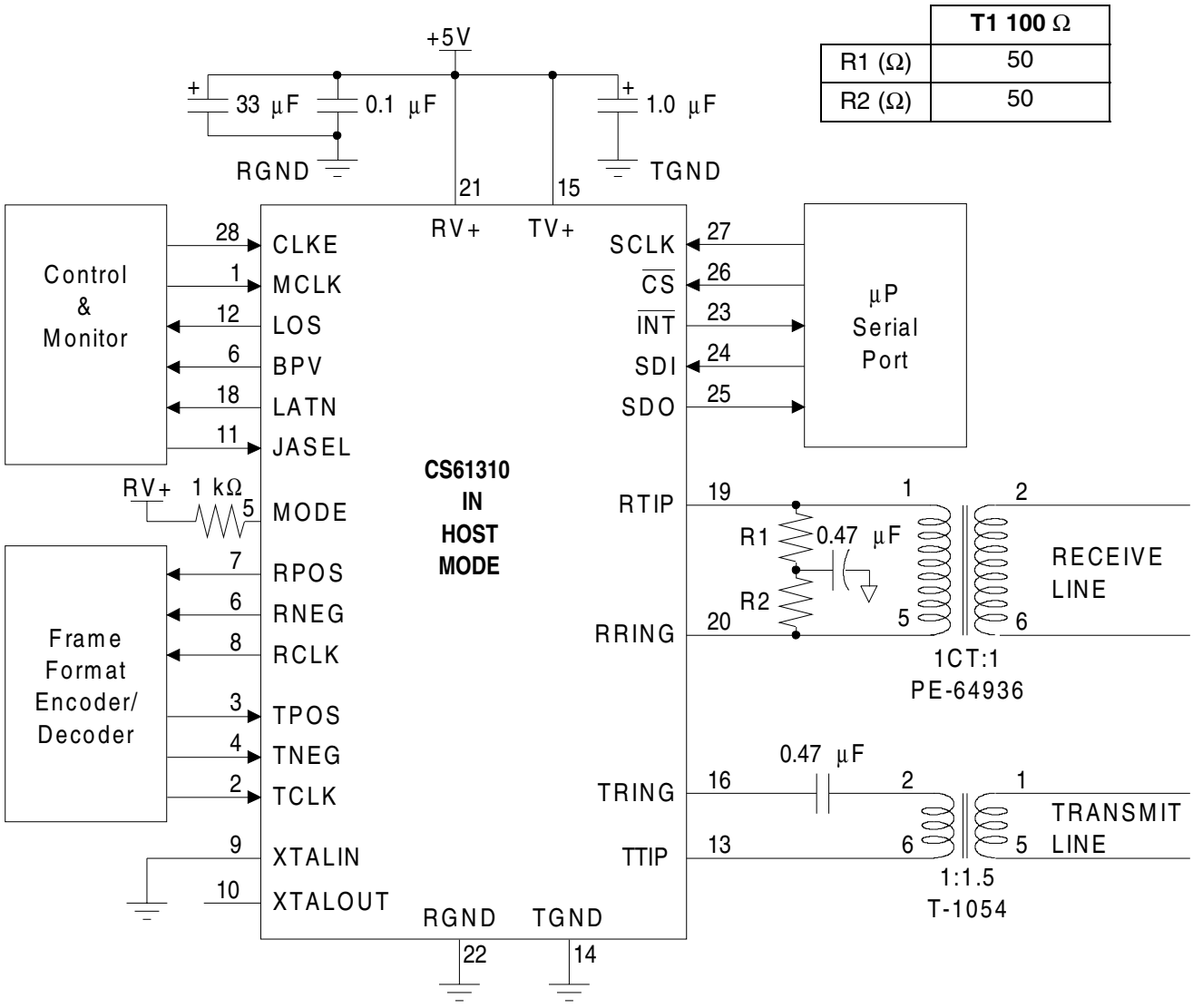
## 6. APPLICATIONS




**NOTE:** The 0.47µF capacitor between R1 & R2 may be omitted if common mode noise is not an issue.

**NOTE:** The optional 0.47µF DC blocking cap eliminates DC saturation current through T2

**Figure 13. Hardware Mode Operation**




| | T1 100 Ω |
|---|---|
| R1 (Ω) | 50 |
| R2 (Ω) | 50 |

**Figure 14. Matched Impedence Output Configuration**

# • Notes •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