BUK9006-55A

TrenchMOS™ logic level FET

Rev. 01 — 1 August 2003 **Preliminary data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor available as a bare die using Philips General Purpose Automotive (GPA) TrenchMOS™ technology.

Product availability:

BUK9006-55A distributed as individual die on reel.

1.2 Features

- 25 A testing of individual die
- Inductive energy testing of individual die
- Life-tested to Q101 at 175 °C
- Automatic visual inspection.

1.3 Applications

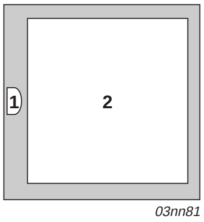
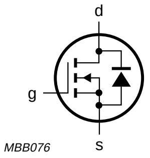
- Automotive systems
- Motors, lamps and solenoids
- 12 V and 24 V loads
- General purpose power switching.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.1$ J
- $V_{(BR)DSS} \leq 55$ V
- Die size = 4.30 × 4.30 mm (typ)
- $R_{DSon(die)} = 5$ mΩ (typ)
- $V_{GS(th)} = 1.5$ V (typ)
- Die thickness = 240 µm (typ).

2. Pinning information

Table 1: Pinning - Bare die simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate		
2	source		
-	drain; connected to underside of die		

3. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			-	55	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	55	V
V_{GS}	gate-source voltage (DC)			-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	[1]	-	125	A
		T_{mb} = 100 °C; V_{GS} = 5 V	[1]	-	88	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	503	A
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[1]	-	125	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	503	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 25 A; $V_{DS} \leq 55$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; starting T_j = 25 °C		-	1.1	J

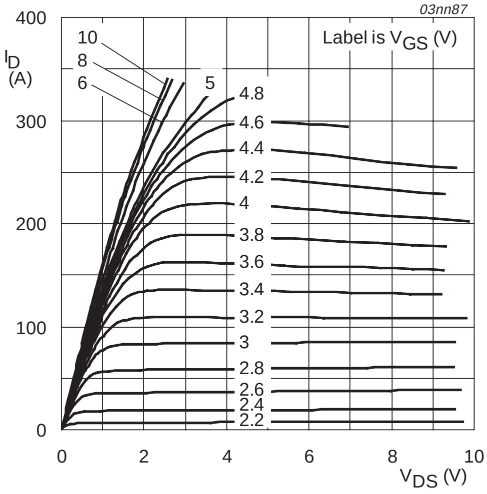
[1] Calculated with $R_{th(j-mb)}$ = 0.59 K/W.

4. Characteristics

Table 3: Characteristics

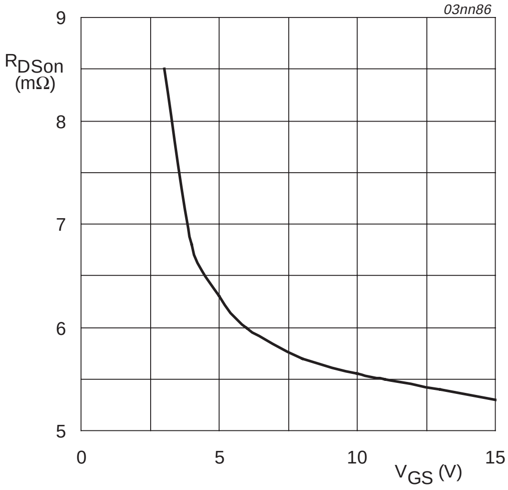
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	55	-	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 5				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	2	100	nA
$R_{DSon(die)}$	die drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 4				
		T_j = 25 °C	-	5	6	mΩ
		T_j = 175 °C	-	-	12	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	V_{GS} = 5 V; V_{DS} = 44 V; I_D = 25 A; Figure 10	-	92	-	nC
Q_{gs}	gate-source charge		-	11	-	nC
Q_{gd}	gate-drain (Miller) charge		-	43	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 8	-	4550	6020	pF
C_{oss}	output capacitance		-	760	900	pF
C_{rss}	reverse transfer capacitance		-	500	690	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	40	-	nS
t_r	rise time		-	175	-	nS
$t_{d(off)}$	turn-off delay time		-	280	-	nS
t_f	fall time		-	167	-	nS
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 11	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs V_{GS} = –10 V; V_{DS} = 30 V	-	70	-	ns
Q_r	recovered charge		-	160	-	nC



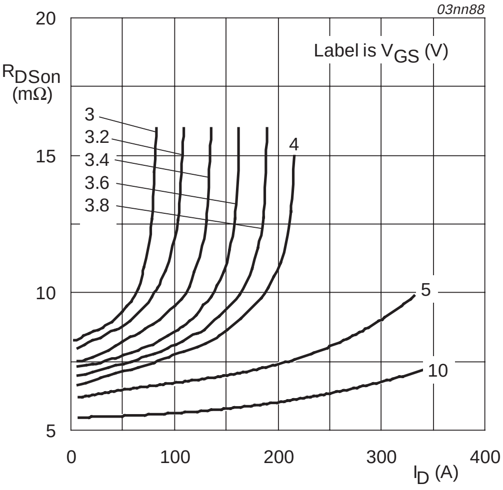
T_j = 25 °C; t_p = 300 µs

Fig 1. Output characteristics: drain current as a function of drain-source voltage; typical values.



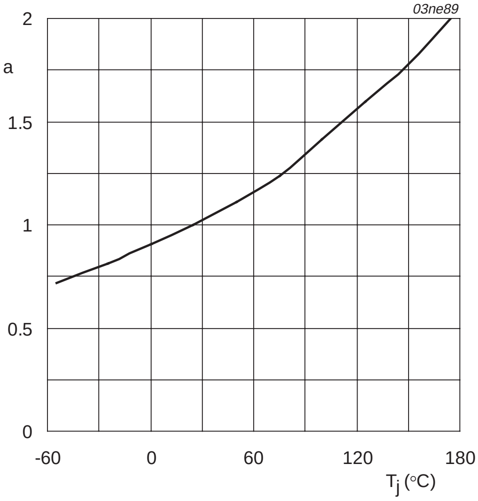
T_j = 25 °C; I_D = 25 A

Fig 2. Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C; t_p = 300 µs

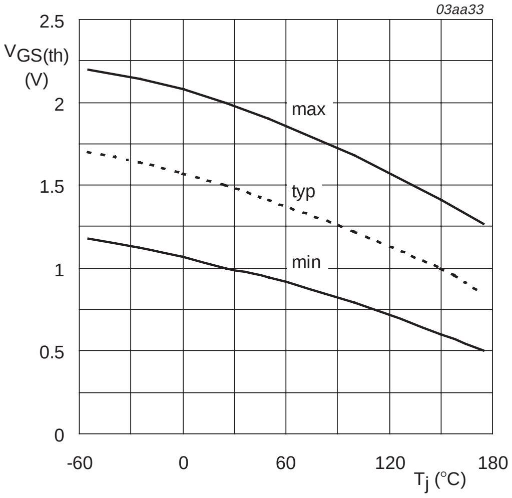
Fig 3. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

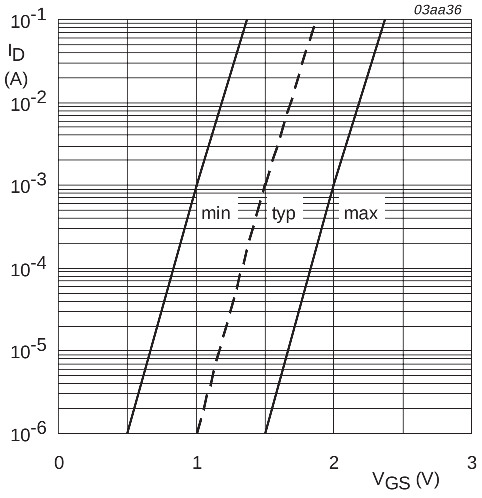
Fig 4. Normalized drain-source on-state resistance factor as a function of junction temperature.

Remark: Figures 1, 2, and 3 measured on die assembled in SOT78 with 3 x 350 µm source bond wires.



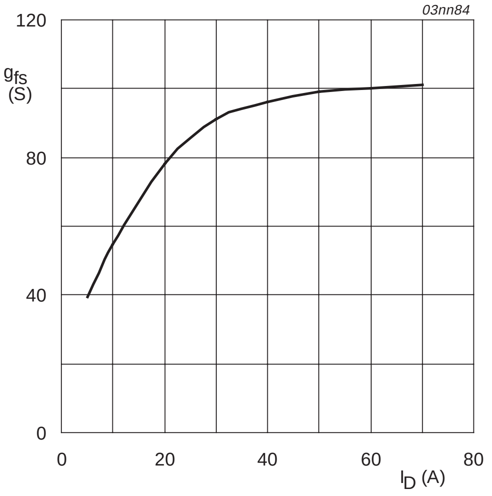
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature.



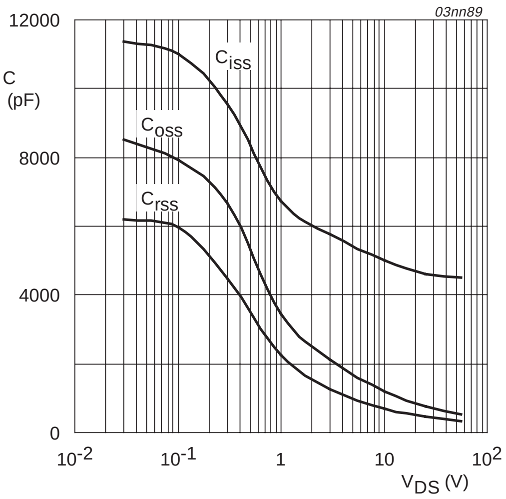
T_j = 25 °C; $V_{DS} = V_{GS}$

Fig 6. Sub-threshold drain current as a function of gate-source voltage.



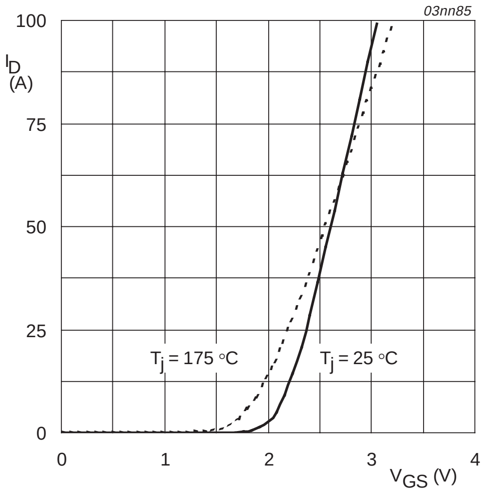
T_j = 25 °C; V_{DS} = 25 V

Fig 7. Forward transconductance as a function of drain current; typical values.



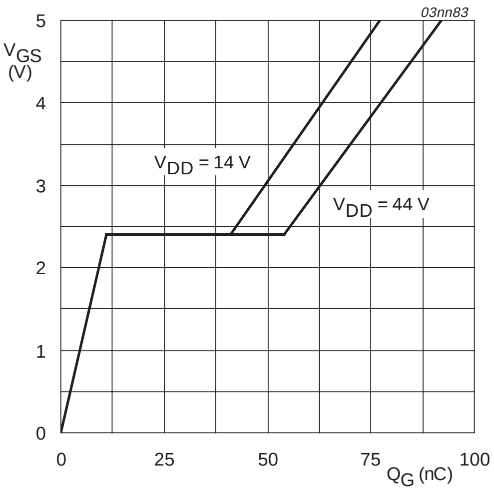
V_{GS} = 0 V; f = 1 MHz

Fig 8. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



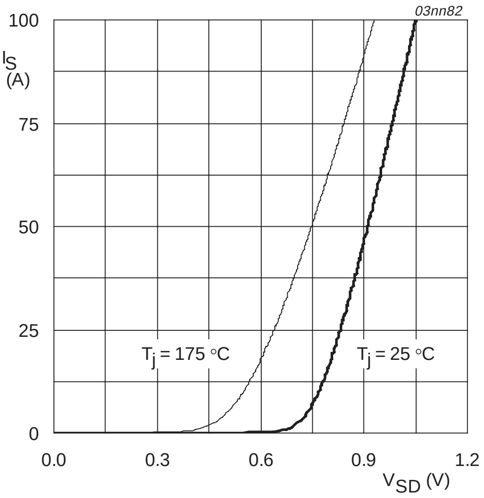
$V_{DS} = 25$ V

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25$ °C; $I_D = 25$ A

Fig 10. Gate-source voltage as a function of gate charge; typical values.

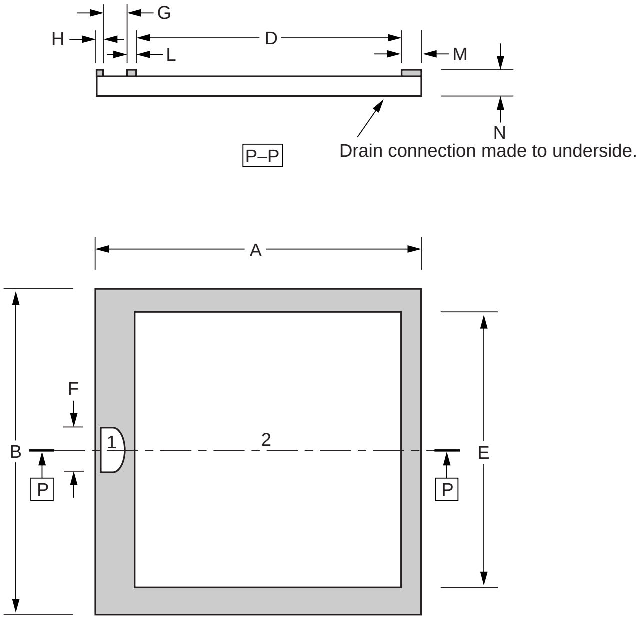


$V_{GS} = 0$ V

Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

Remark: Figures 9, 10, and 11 measured on die assembled in SOT78 with 3 x 350 µm source bond wires.

5. Bare die outline



TYPICAL DIMENSIONS

UNIT	A	B	D	E	F	G	H	L	M	N
mm	4.30	4.30	3.36	3.62	0.54	0.4	0.096	0.175	0.27	0.24 ± 0.025

03nn80

Fig 12. Bare die outline.

Table 4: Bare die information

Parameter	Description
Top-side metallization (gate and source bond pads)	5 µm Al + 1 % Si (sputtered)
Back-side metallization (drain contact)	0.1 µm Ti / 0.3 µm Ni / 0.1 µm Ag (evaporated)
Passivation layer	1 µm Si_3N_4

6. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030801	-	Preliminary data (9397 750 11571)

7. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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