



AOU454

N-Channel Enhancement Mode Field Effect Transistor

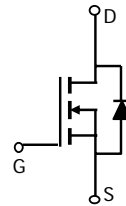
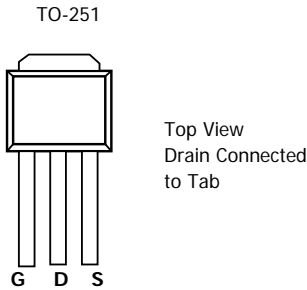


General Description

The AOU454 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. *Standard Product AOU454 is Pb-free (meets ROHS & Sony 259 specifications). AOU454L is a Green Product ordering option. AOU454 and AOU454L are electrically identical.*

Features

- V_{DS} (V) = 40V
- I_D = 12 A (V_{GS} = 10V)
- $R_{DS(ON)}$ < 33 m Ω (V_{GS} = 10V)
- $R_{DS(ON)}$ < 47 m Ω (V_{GS} = 4.5V)



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	30	
Avalanche Current ^C	I_{AR}	12	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	20	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	50	60	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =32V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2.3	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A		25	33	mΩ
		T _J =125°C		39	52	
		V _{GS} =4.5V, I _D =6A		34	47	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =12A		25		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		404		pF
C _{oss}	Output Capacitance			95		pF
C _{rss}	Reverse Transfer Capacitance			37		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.7		Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =12A		9.2		nC
Q _g (4.5V)	Total Gate Charge			4.5		nC
Q _{gs}	Gate Source Charge			1.6		nC
Q _{gd}	Gate Drain Charge			2.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1.7Ω, R _{GEN} =3Ω		3.5		ns
t _r	Turn-On Rise Time			6		ns
t _{D(off)}	Turn-Off DelayTime			13.2		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, dI/dt=100A/μs		22.9		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =12A, dI/dt=100A/μs		18.3		nC

- A: The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.
 - B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
 - C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.
 - D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
 - E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
 - F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.
 - G: The maximum current rating is limited by bond-wires.
- Rev 0 : Aug 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

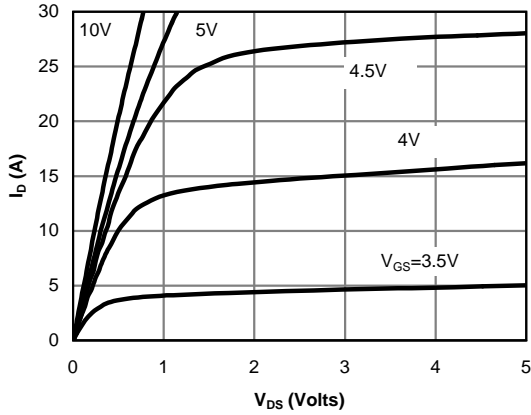


Fig 1: On-Region Characteristics

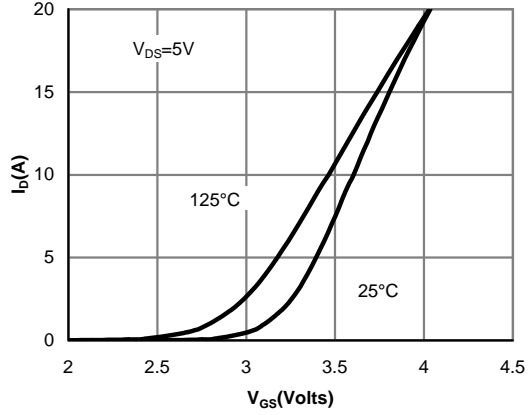


Figure 2: Transfer Characteristics

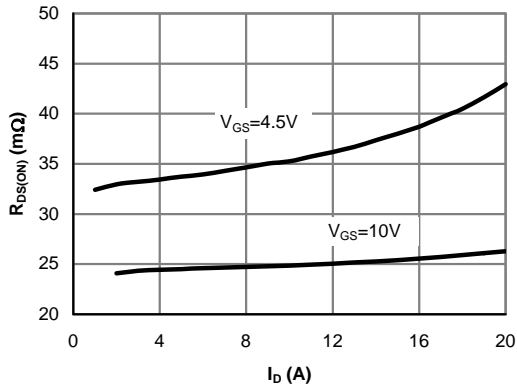


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

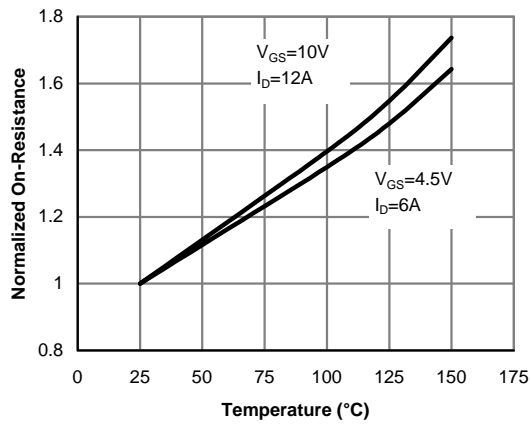


Figure 4: On-Resistance vs. Junction Temperature

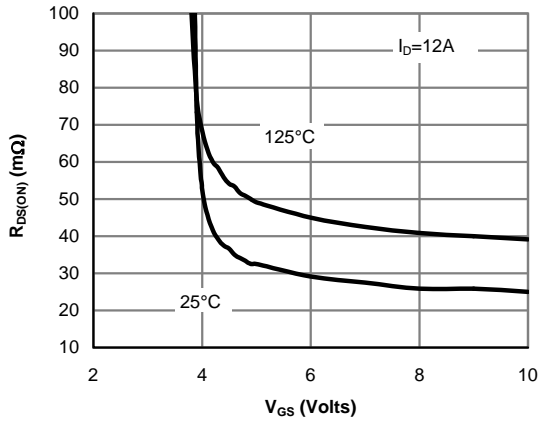


Figure 5: On-Resistance vs. Gate-Source Voltage

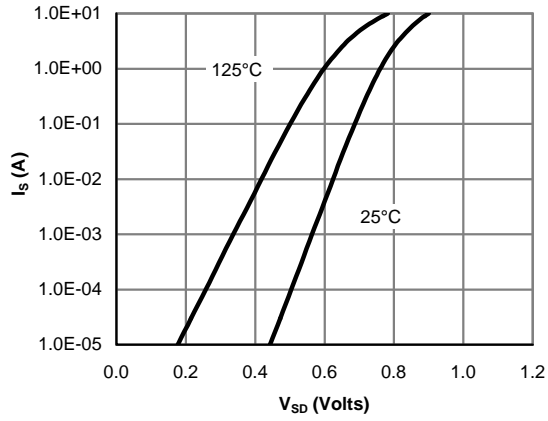


Figure 6: Body-Diode Characteristics

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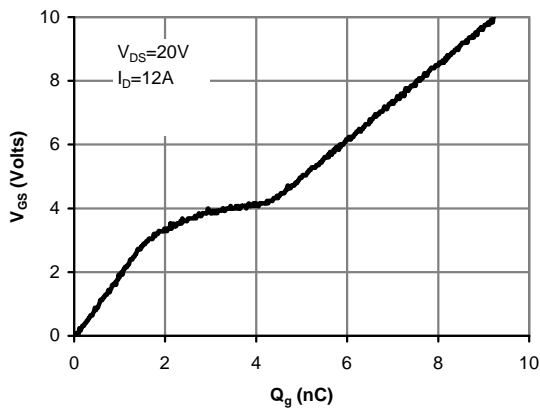


Figure 7: Gate-Charge Characteristics

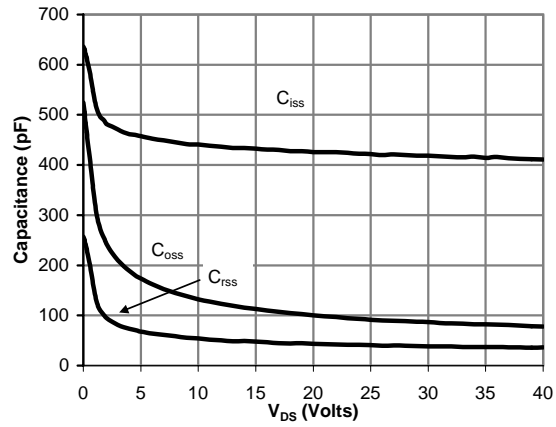


Figure 8: Capacitance Characteristics

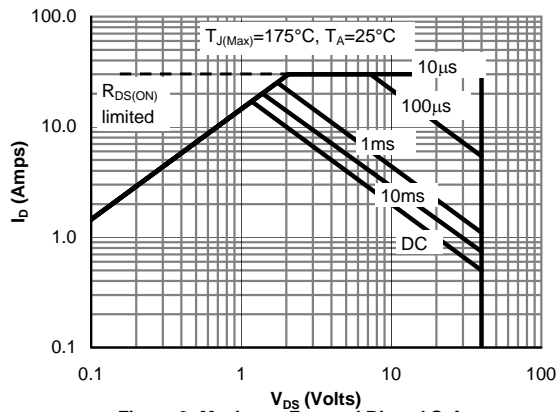


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

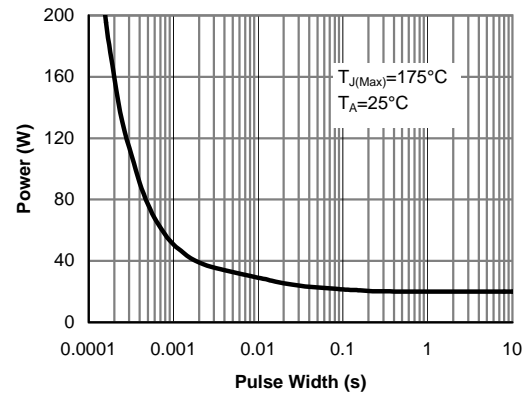


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

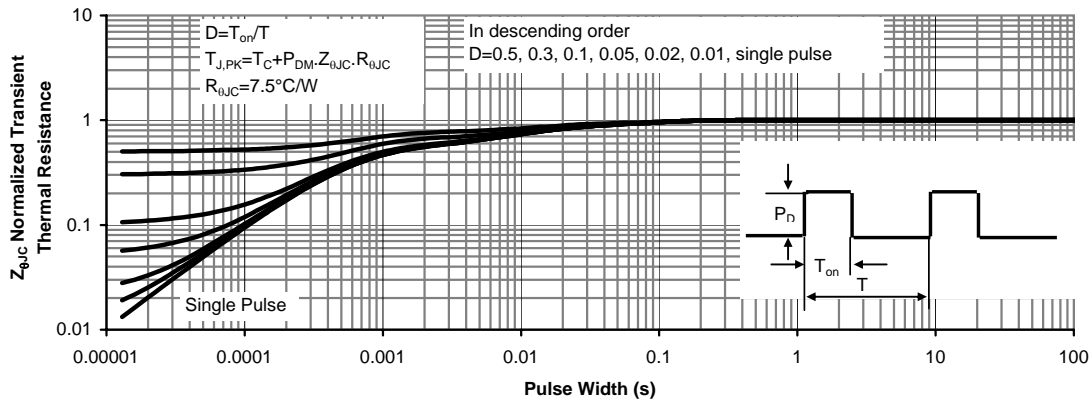


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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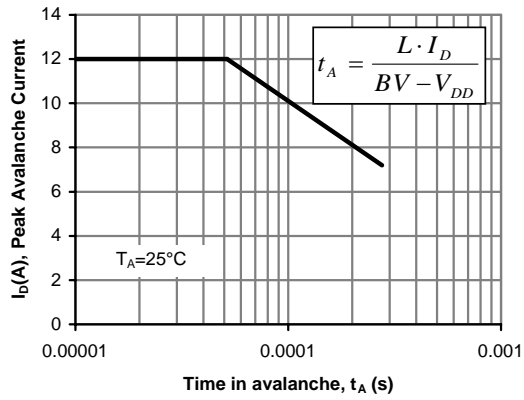


Figure 12: Single Pulse Avalanche capability

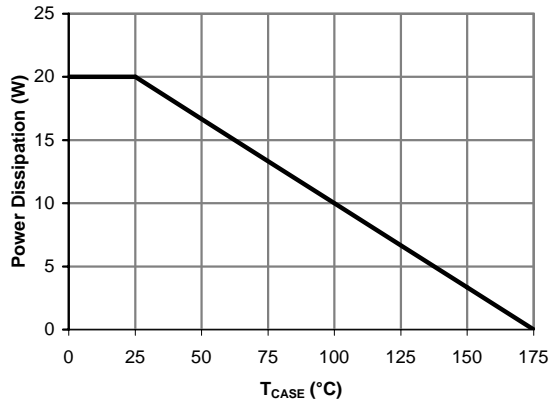


Figure 13: Power De-rating (Note B)

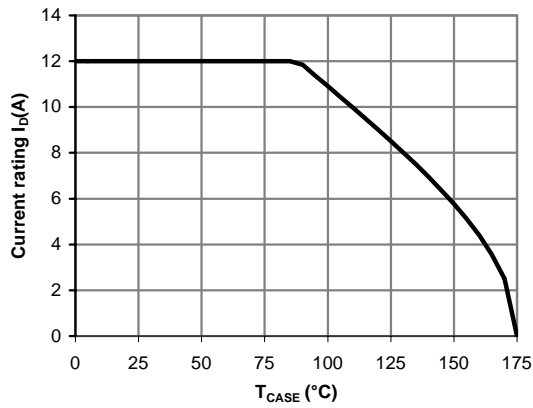


Figure 14: Current De-rating (Note B)