



# Si321X LINEFEED POWER MONITORING AND PROTECTION

## Introduction

The Silicon Laboratories' ProSLIC products are designed to continuously monitor the power dissipated in each of the six external bipolar transistors in the linefeed circuit. These power measurement results are available to the user in software registers and are also used by the ProSLIC to protect linefeed transistors from damage due to overpower conditions. Using proper power threshold and thermal low-pass filter settings, the ProSLIC will either alert the user or automatically transition the open state in the event of an overpower condition.

## Power Threshold

As the dissipated power in linefeed transistors increases, so does the junction temperature of the transistor die. The maximum admissible junction temperature must not be exceeded because this could damage or destroy the transistor die. In the Si321x, the measured power consumed in each of the transistors is compared to the power threshold values in the corresponding indirect registers. If the power in any external transistor exceeds the programmed threshold (after passing through a user-programmable low pass filter which will be explained in the next section), a power alarm is triggered to indicate line fault condition. Unless the auto-open feature is disabled (direct register 67, bit 0), the ProSLIC automatically goes into the open state.

The value of the power threshold is calculated based on the characteristic of the transistors used. Transistor manufacturers provide this information in terms of thermal resistance for each transistor package. The relationship between the maximum junction temperature and the maximum power that can be dissipated by the transistor package is defined in the following equation:

$$T_{JMAX} = T_{AMB} + P_{MAX} \times R_{THJA}$$

where  $T_{JMAX}$  is the maximum junction temperature (usually 150 °C),  $T_{AMB}$  is the ambient temperature (70 °C for commercial rating), and  $P_{MAX}$  is the maximum power allowance on the transistor package.  $R_{THJA}$  is the junction to ambient thermal resistance of the transistor package.

The thermal resistance ( $R_{THJA}$ ) of the transistor is improved when it is mounted on a PCB board. This improvement depends on the PCB size, the material it is made of, and the amount of the copper surface on the PCB board. Figure 1 illustrates how the board material, available board area, and the amount of copper present influence the thermal resistance of the transistors. This chart can be obtained from the transistor manufacturer if not included in the transistor data sheet.

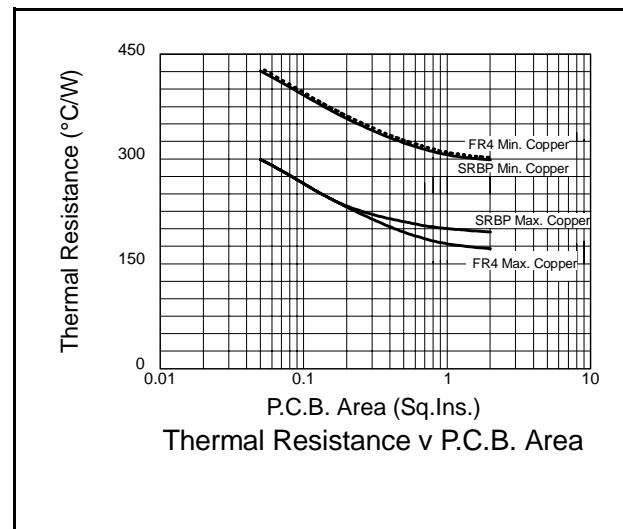


Figure 1. SOT23

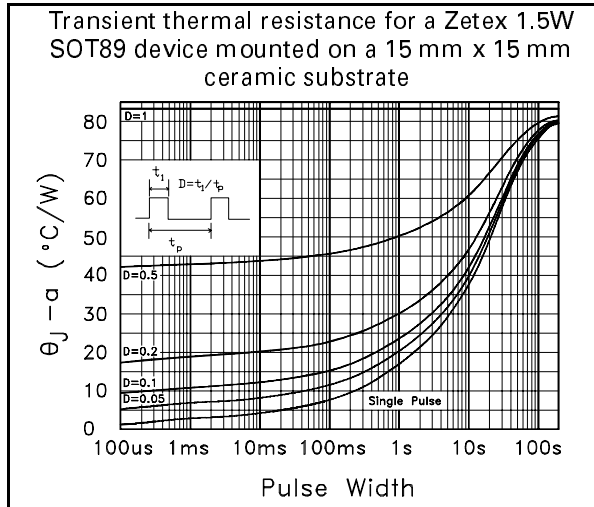
In practice, the transistors are normally mounted on a PCB with several square inches area, but for illustration purposes consider a model in which the transistor package is mounted on 1-inch square of FR4 PCB with 0.25-inch square of copper surface. This 1-inch square PCB model and the thermal resistance vs. PCB area charts provide the practical thermal resistances for the following transistor packages:

SOT23:  $R_{THJA} = 200 \text{ °C/W}$

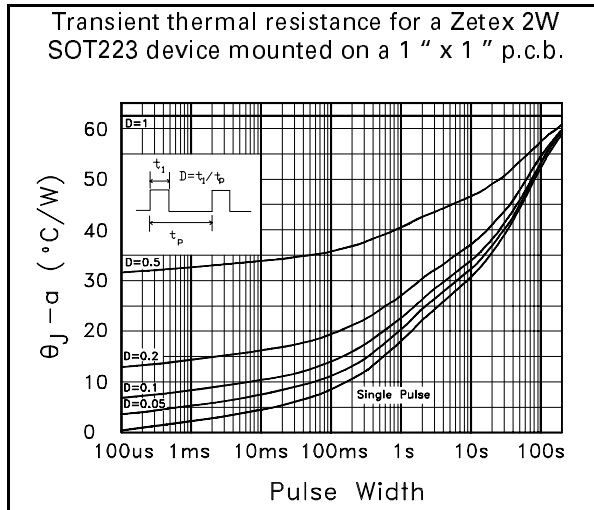
The thermal resistance can also be obtained from the transient thermal resistance curve with  $D = 1$  as shown in Figure 2 and Figure 3.

SOT89:  $R_{THJA} = 82.5 \text{ °C/W}$

SOT223:  $R_{THJA} = 62.5 \text{ °C/W}$



**Figure 2. SOT89**



**Figure 3. SOT223**

The equation to calculate the power threshold value for the transistors pair is as follows:

$$PPT_{xx} = \left( \frac{P_{MAX}}{\text{Resolution}} \right) \times 2^7 (\text{decimal})$$

Where

Resolution = 30.4 mW for Q1, Q2 and Q5, Q6 pairs  
 = 3.62 mW for Q3, Q4 pair

The following calculations are examples of the power threshold coefficient for the SOT223 package:

From equation 1:

$$P_{MAX} = \frac{(T_{JMAX} - T_{AMB})}{R_{THJA}} = \frac{(150^\circ - 70^\circ)}{62.5^\circ\text{C/W}} = 1.28\text{W}$$

From equation 2:

$$PPT_{12 \text{ or } PPT_{56}} = \left( \frac{1.28}{0.0304} \right) \times 2^7 = 5389(d) = 0x150D$$

$$PPT_{34} = \left( \frac{1.28}{0.0362} \right) \times 2^7 = 0xB0CB|_{\text{limited}} = 0x6E7E$$

Because the range of the power threshold is from 0 to 0x7FFF, using 0x6E7E is recommended. While the maximum power threshold for these transistors falls outside the range of Indirect Register 33, 0x6E7E is a conservative estimate of a threshold above the maximum power Q3 and Q4 would be dissipating in a normal application.

### Thermal Low Pass Filter

While the power threshold coefficient sets the absolute maximum dc power that the transistor can handle for an indefinite period of time, it only provides a static maximum dc trip point. In the Si321x circuit application, the transistors are subjected to complex power dissipation, which is comprised of dc biasing current and ac signaling. The ac part of the power dissipation may be limited to short times and with repeated pulse (ringing). A static maximum power threshold setting does not provide an adequate model for real operating conditions. In conjunction with the power threshold setting, the Si321x also provides the thermal low pass filter setting which models the operating condition more accurately.

Calculation of the thermal low pass filter is based on the characteristic of the transistor package. The heating process of the transistor package is an exponential phenomenon which can be described by the following equation:

$$T(t) = T_{DC}(1 - e^{-t/\tau})$$

Where  $T_{DC}$  is the final temperature and,  $\tau$  is the thermal time constant.

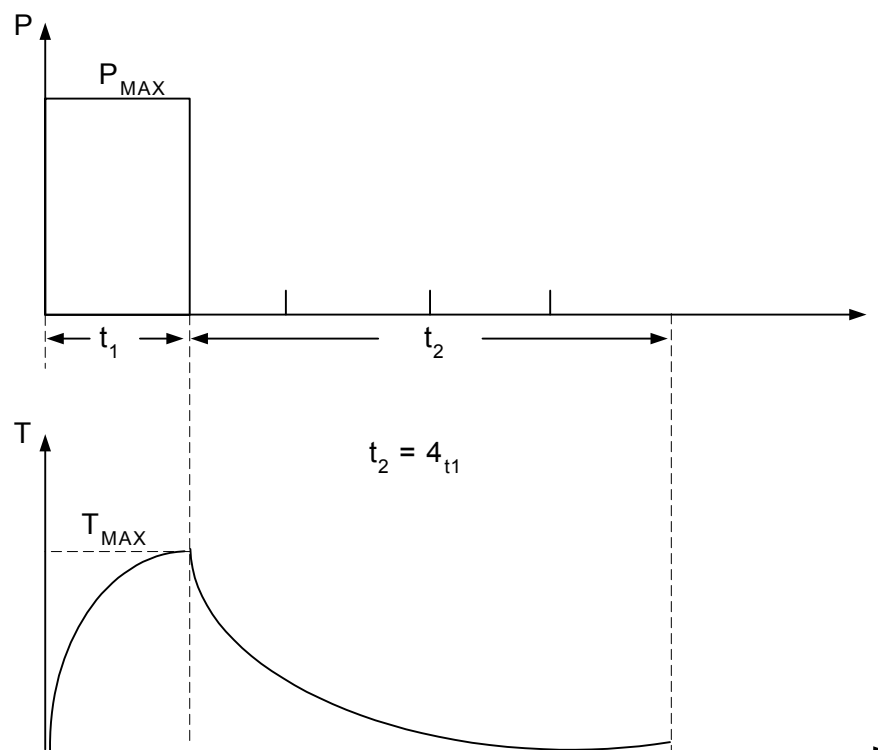
Thermal resistance ( $\theta$ ) may replace the temperature ( $T$ ) in this equation since they both represent the temperature of the transistor package.

$$\theta(t) = \theta_{DC}(1 - e^{-t/\tau})$$

### Equation 1

Where  $\theta_{DC}$  is the dc thermal resistance.

The Si321x implements this transfer function by allowing the setting of the thermal constants ( $\tau$ ) to the registers. Figure 4 shows the heating and cooling of the transistor package. Power is applied to the transistor and heats it up during  $t_1$ . It is allowed to cool during  $t_2$ .



**Figure 4. Transistor Package Heating and Cooling**

The  $\theta_{EFF}$  is defined as the thermal resistance of the transistor package at  $t = \tau$  (one time constant).

$$\theta_{EFF} = \theta(\tau) = \theta_{DC}(1 - e^{-\tau/\tau}) = \theta_{DC}(1 - e^{-1}) = 0.63\theta_{DC}$$

### Equation 2

The cooling process of the transistor is also an exponential process which can be described by the following equation:

$$\theta(t) = \theta_{DC} \times e^{-t/\tau}$$

When  $t = 4\tau$  the  $\theta_{DC}$  (initial condition) is decayed to almost zero.

$$\theta(4\tau) = \theta_{DC} \times e^{-4\tau/\tau} = 0.18\theta_{DC}$$

### Equation 3

The thermal time constant ( $\tau$ ) can be estimated by calculating the  $\theta_{EFF}$  with Equation 2 and the  $\theta_{DC}$  data from the Transient Thermal Resistance curves.

The thermal period ( $t_p$ ) can then be found on the Transient Thermal Resistance graph using the  $\theta_{EFF}$  value and the  $D = .2$  curve. This estimation process is graphically illustrated in Figure 5.

Below is the calculation example of the power threshold coefficient for the SOT223 package.

From Figure 2:

$$\theta_{DC} = 62.5 \text{ (D = 1 line)}$$

From Equation 2:

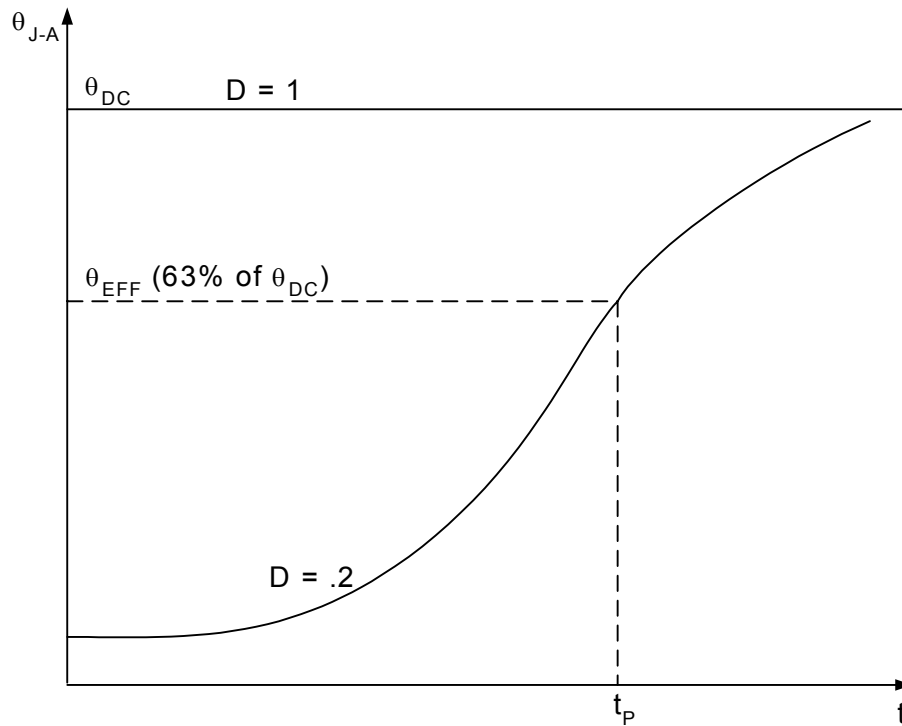
$$\theta_{EFF} = .63\theta_{DC} = 39.4$$

Using  $\theta_{EFF} = 39.4$  to find the thermal period ( $t_p$ ) in Figure 3, using  $D = .2$ , curve:  $t_p = 15 \text{ s}$

$$\tau = 0.2t_p = 3 \text{ s}$$

The equation for calculating the thermal LPF register is given in the Si321x data sheet:

$$\begin{aligned} \text{Thermal LPF register} &= \left(\frac{4096}{800\tau}\right) \times 2^3 \\ &= \left(\frac{4096}{800(3)}\right) \times 2^3 = 13.7 \\ &= 0x0E \text{ (hex)} \end{aligned}$$



**Figure 5. Thermal Time Constant ( $\tau$ ) Estimation**

**Table 1. Power Coefficients for Some Transistor Packages**

Indirect Register	SOT23	SOT89	SOT223
32 (Q1/Q2 Power Threshold)	0x0700	0x0FF4	0x150D
33 (Q3/Q4 Power Threshold)	0x373F	0x6E7E*	0x6E7E*
34 (Q5/Q6 Power Threshold)	—	0x0FF4	0x150D
37 (Q1/Q2 Power LPF)	0x008C	0x0012	0x000E
38 (Q3/Q4 Power LPF)	0x008C	0x0012	0x000E
39 (Q5/Q6 Power LPF)	—	0x0012	0x000E

**\*Note:** While the maximum power threshold for these transistors falls outside the range of Indirect Register 33, 0x6E7E is a conservative estimate of a threshold above the maximum power Q3 and Q4 would be dissipating in a normal application.

## Power Dissipation in the Si3201

The Si3201 is a line-side IC that replaces the discrete transistors in the Si321x schematic. Because the Si3201 circuitry differs from that of the discrete components, it is difficult to compute a maximum power threshold per transistor. Silicon Laboratories recommends SOT89 register settings (as shown in Table 1) when using the Si3201 linefeed IC.

## Document Change List

### Revision 0.1 to Revision 0.2

- Changed power threshold values for SOT89/223 transistors
- Corrected calculations
- Added information for the Si3201



## Contact Information

Silicon Laboratories Inc.  
4635 Boston Lane  
Austin, TX 78735  
Tel: 1+(512) 416-8500  
Fax: 1+(512) 416-9669  
Toll Free: 1+(877) 444-3032  
Email: [productinfo@silabs.com](mailto:productinfo@silabs.com)  
Internet: [www.silabs.com](http://www.silabs.com)

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.