## 1.0 Description

AMI Semiconductor's WSN series is a family of self-scanning photodiode solid-state linear imaging arrays. These photodiode sensors employ AMI Semiconductor's proprietary CMOS image sensing technology to integrate the sensors into a single monolithic chip. These sensors are optimally designed for applications in spectroscopy. Accordingly, these sensors contain a linear array of photodiodes with an optimized geometrical aspect ratio (50µm aperture pitch x 2500µm aperture width) for helping to maintain mechanical stability in spectroscopic instruments and for providing a large light-capturing ability. The family of sensors consists of photodiode arrays of various lengths - 128, 256 and 512 pixels.

The WSN photodiode arrays are mounted in 22-pin ceramic side-brazed dual-in-line packages that fit in standard DIP sockets. A diagram of its pin out configuration is seen in Figure 1.

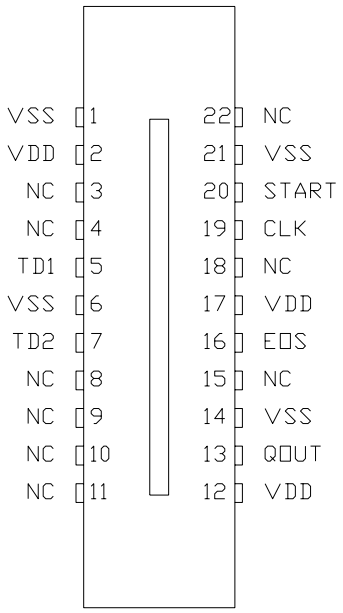



*Figure 1: Pin Out Configuration*

## 2.0 Features

- 65pC saturation capacity for wide dynamic range
- Wide spectral response (180 – 1000nm) for UV and IR response
- NP junction photodiodes with superior resistance to UV damage
- Low dark current
- Integration time up to nine seconds at room temperature
- Integration time extended to hours by cooling
- High linearity
- Low power dissipation (less than 1mW)
- Geometrical structure for enhanced stability and registration
- Standard 22 lead dual-in-line IC package

## 3.0 Sensor Characteristics

AMI Semiconductor's self-scanned WSN photodiodes are spaced on a 50µm pitch. The line density is 20 diodes/mm and accordingly the overall die lengths of the different arrays vary with the number of photodiodes. For example, the 128 pixel array is 6.4mm long, the 256 pixel array is 12.8mm long and the 512 pixel array is 25.6mm long. Each array has four additional dummy photodiodes. On each side, there is one dark (non-imaging) dummy photodiode and one imaging dummy photodiode. The height of the sensors is 2500µm. The tall, narrow apertures make these sensors desirable for use in monochromators and spectrographs.

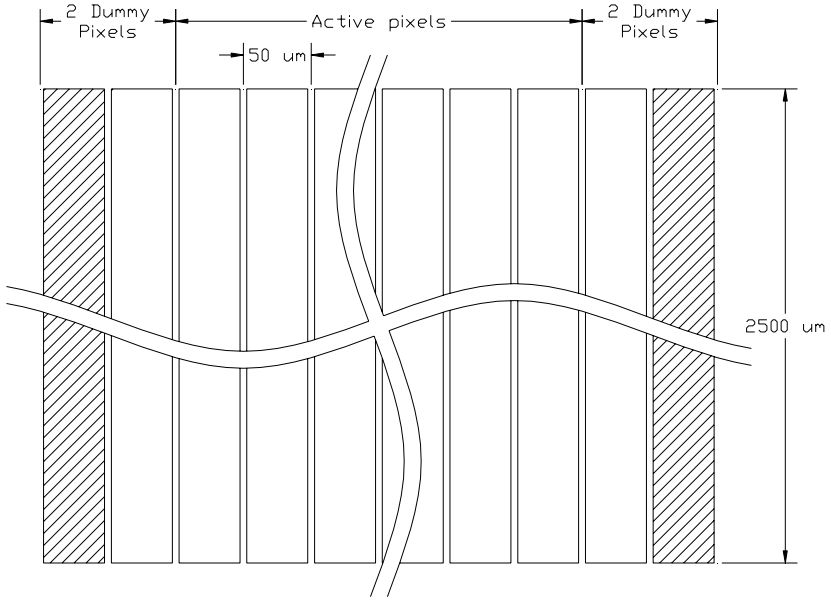



*Figure 2: Geometry and Layout of Photodiode Pixels*

During normal operation, the photons incident in or near the NP photodiode junction generate free charges that are collected and stored on the junction's depletion capacitance. The number of collected charges is proportional to the light exposure. Figure 3 shows the stored signal charge as function of light exposure at a wavelength of 575nm. The exposure is the product of the light intensity in $nW/cm^2$ and integration time in seconds. The charge accumulates linearly until reaching the saturation charge, and the corresponding exposure is the saturation exposure.

The responsivity may be calculated as the saturation charge divided by saturation exposure. The predicted typical responsivity of a photodiode is $3.5 \times 10^{-4}$ $C/J/cm^2$ at 575nm. Figure 4 shows the predicted responsivity of the photodiodes as a function of wavelength.

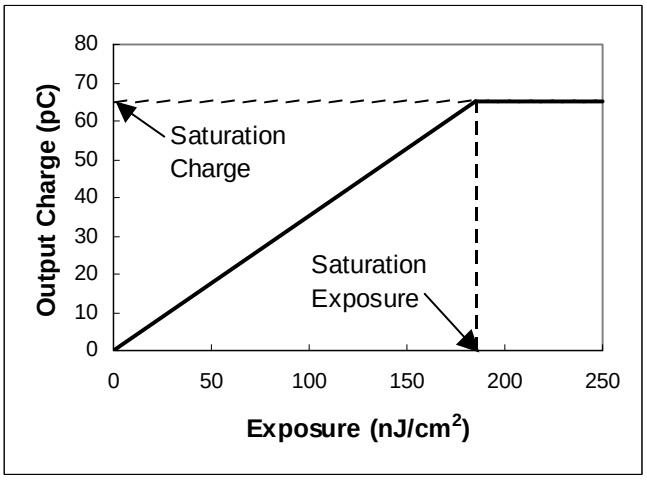



*Figure 3: Stored Signal Charge as a Function of Exposure at a Wavelength of 575nm*

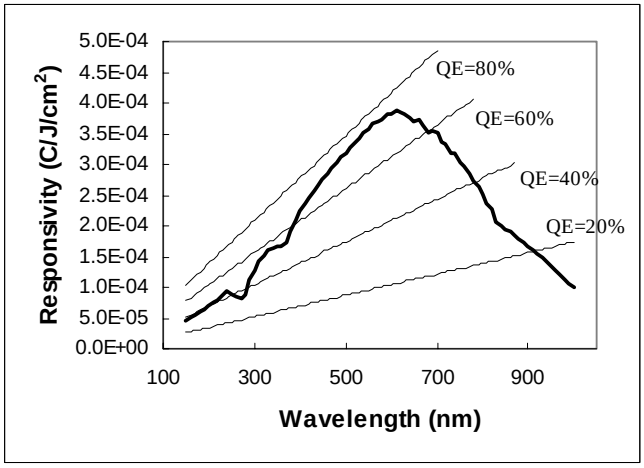



*Figure 4: Predicted Spectral Response*

**Note:** Quantum efficiency (QE) can be calculated by dividing the responsivity by the area of the sensor's element and multiplying the resulting ratio by the energy per photon in electron volts (eV).

The dark current is typically 0.2pA at 25°C and varies as function of temperature. The dark current will contribute dark-signal charges and these charges will increase linearly with integration time. The dark signal and the photo generated signal combined result in the total signal charge.

## 4.0 Self-Scanning Circuit

Figure 5 shows a simplified electrically equivalent circuit diagram of the photodiode array. An MOS read switch connects every photodiode in the array to a common output video line. Incident photons generate electron charge that is collected on each imaging photodiode while the switch is open. The shift register is activated by the start pulse. A pulse propagates through each shift register stage and activates the MOS read switches sequentially. As the shift register sequentially closes each read switch, the negative stored charge, which is proportional in amount to the light exposure, from the corresponding photodiode, is readout onto the video line, QOUT. Typically, an external charge-integrating amplifier senses the negative output charge on the video line from each photodiode pixel. The shift register continues scanning the photodiodes in sequence, until the last shift register stage is reach, at which time the fourth and last dummy pixel is read out and end-of-scan (EOS) output is held high for one clock cycle. The next start pulse can then restart the shift register.

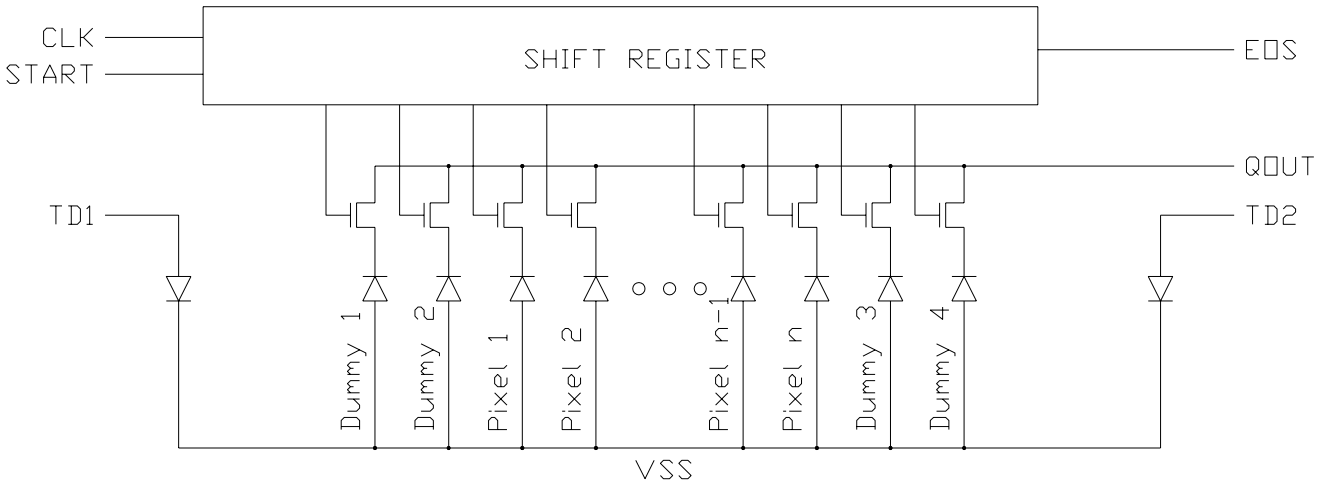



*Figure 5: Simplified Circuit Diagram of a WSN Photodiode Array*

## 5.0 I/O Pins

Although the WSN package has 22 pins, as shown in Figure 1, there are only six functionally active I/O pins in addition to the supply pins, as shown in Figure 5. In essence, only two clocks, CLK and START, are required for controlling the timing of the sensor's video readout. The remaining I/O descriptions are for the video signal output, the end-of-scan signal, the two temperature diodes, and the supply biases. QOUT must be biased externally to Vbias (see Section 7.0 Recommended Operating Conditions). Each temperature diode is operated with a small constant current that forward-biases its PN junction. By measuring the forward-bias voltage, one can track the silicon die temperature. The temperature diodes may be disabled by connecting their anodes to VSS. These I/Os are listed with their acronym designators and functional descriptions in the following Table 1.

Table 1: Symbols and Functions and I/O Pins

| Symbol | Function and Description |
|---|---|
| VSS | Ground |
| VDD | +5.0V |
| START | Start pulse: input to start the line scan |
| CLK | Clock pulse: input to clock the shift register |
| EOS | End of scan: output from the shift register to indicate the completion of one line scan |
| QOUT | Video charge output: output from the photodiodes pixels |
| TD1 | Temperature diode 1: anode of temperature diode 1 |
| TD2 | Temperature diode 2: anode of temperature diode 2 |
| NC | No connection |

## 6.0 Clock and Voltage Requirements

The clocking requirements are relatively simple. As it was indicated in Figure 5 and Table 1, there are only two input signals that require clocked inputs. They are CLK, the clock for the shift register, and START, the shift register start pulse. The timing specifications and the symbol definition for Figure 6 are listed in Table 2. The control clock amplitudes for I/Os are compatible with the 5V CMOS devices.

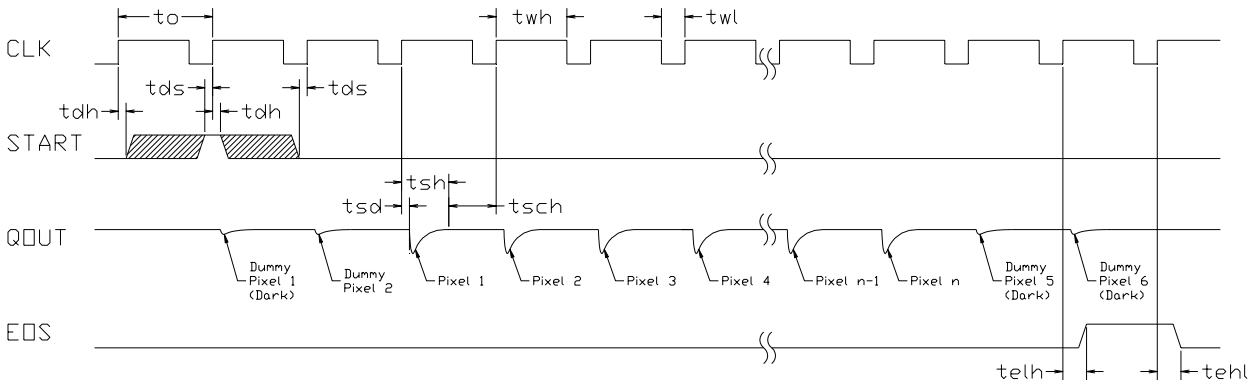



*Figure 6: Timing Diagram*

Table 2: Symbol Definitions and Timing Specifications for Timing Diagram

| Item | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Clock cycle time | to | 666 (AMIS-732128)<br>666 (AMIS-732256)<br>1000 (AMIS-732512) | 10000 | | ns |
| Clock high pulse width | twh | 566 (128WSN)<br>566 (256WSN)<br>900 (512WSN) | | | ns |
| Clock low pulse width | twl | 100 | | | ns |
| Clock duty cycle | | 1 | 50 | 99 | % |
| Data setup time | tds | 100 | | | ns |
| Data hold time | tdh | 100 | | | ns |
| EOS low-to-high delay | telh | | | 400 | ns |
| EOS high-to-low delay | tehl | | | 400 | ns |
| Signal delay time | tsd | 50 | | | ns |
| Signal settling time | tsh | | | 566 (AMIS-732128)<br>566 (AMIS-732256)<br>900 (AMIS-732512) | ns |
| Signal settle to clock edge | tsch | 0 | | | ns |

## 7.0 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 3: Recommended Operating Conditions at 25°C

| Parameters | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Power supply | VDD | 4.5 | 5.0 | 5.5 | V |
| Input clock pulses high level [1] | Vih | VDD – 0.8 | VDD | VDD | V |
| Input clock pulse low level [1] | Vil | 0.0 | 0.0 | 0.8 | V |
| Video charge output external bias | Vbias | VDD – 0.5 | VDD – 0.5 | VDD | V |
| Clock frequency | Fclk | | 0.1 | 1.5 (AMIS-732128)<br>1.5 (AMIS-732256)<br>1.0 (AMIS-732512) | MHz |
| Integration time [2] | Tint | 0.09 (AMIS-732128)<br>0.18 (AMIS-732256)<br>0.52 (AMIS-732512) | | 9000 | ms |

**Notes:**

1. Applies to all control-clock inputs.
2. The Integration time is specified at room temperature such that the maximum dark current charge build up in each pixel is less than 10 percent of the minimum saturation charge. Accordingly, it may be as long as nine seconds at room temperature. Longer integration times may be achieved by cooling the device. An appropriate clock frequency must be chosen so that the shift register completes its operation within the desired integration time.

# 8.0 Electro-Optical Characteristics

The following table lists the electro-optical characteristics.

Table 4: Electro-Optical Characteristics at 25°C

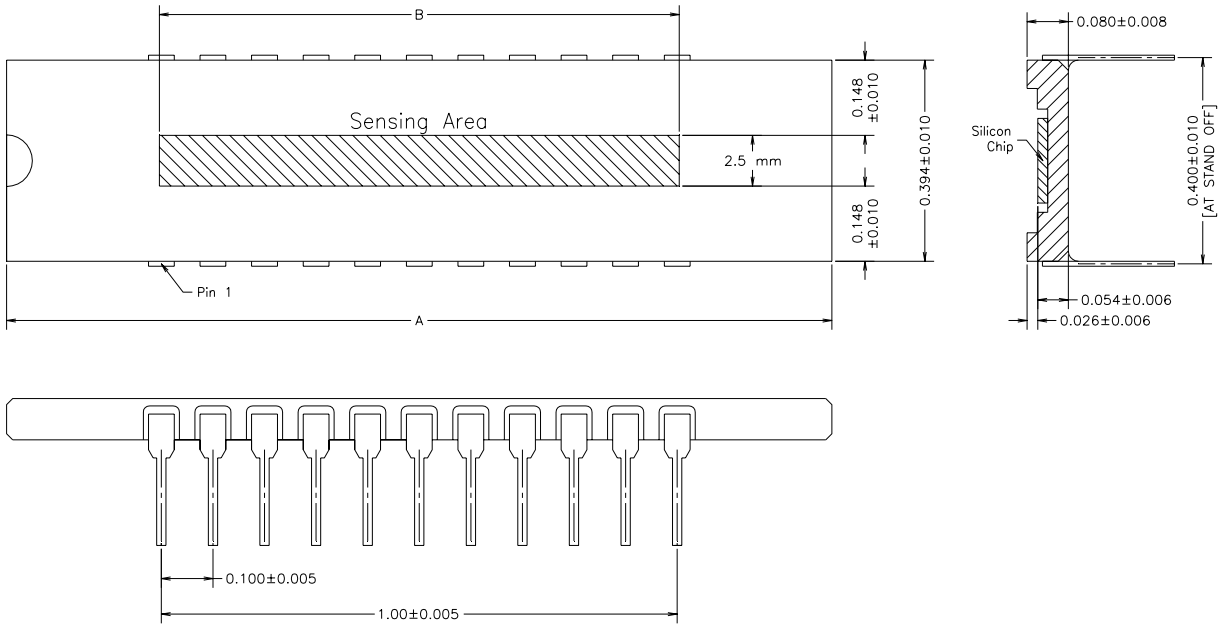
| Parameters | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Center-to-center spacing | | | 50 | | µm |
| Aperture width | | | 2500 | | µm |
| Pixel area | A | | $1.25 \times 10^{-3}$ | | $cm^2$ |
| Fill factor [1] | FF | | 86 | | % |
| Quantum efficiency [1,2] | QE | | 70 | | % |
| Responsivity [1,2] | R | | $3.5 \times 10^{-4}$ | | $C/J/cm^2$ |
| Non-uniformity of response [3] | | | 2 | 5 | +/-% |
| Saturation exposure [2] | Esat | 160 | 185 | | $nJ/cm^2$ |
| Saturation charge [4] | Qsat | 55 | 65 | | pC |
| Average dark current [5] | | | 0.2 | 0.6 | pA |
| Spectral response peak | $\lambda$ | | 600 | | nm |
| Spectral response range [6] | | | 180 – 1000 | | nm |

**Notes:**

1. Fill factor, quantum efficiency and responsivity are related by the equation $R = (q_e \lambda / hc) \cdot QE \cdot FF \cdot A$, where $q_e$ is the charge of an electron and $hc/\lambda$ is the energy of a photon at a given wavelength. Responsivity is therefore given per pixel.
2. At wavelength of 575nm (yellow-green) and with no window.
3. Measured at 50 percent Vsat with an incandescent tungsten lamp filtered with an Schott KG-1 heat-absorbing filter.
4. Saturation charge specified for a video output bias of 4.5V.
5. Max. dark leakage ≤ 1.5 x average dark leakage measured with an integration period of 500ms at 25°C.
6. From 250-1000nm, responsivity ≥ 20 percent of its peak value.

## 9.0 Package Dimensions

The following figure provides the package dimensions.




| Device | A | B |
|---|---|---|
| PI0128WSN | 1.08 ±0.01 | 6.4mm |
| PI0256WSN | 1.08 ±0.01 | 12.8mm |
| PI0512WSN | 1.6 ±0.01 | 25.6mm |

*Figure 7: Package Dimensions*

**Note:** Dimensions are in inches except where millimeters (mm) are indicated.

## 10.0 Company or Product Inquiries

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