79LV0832
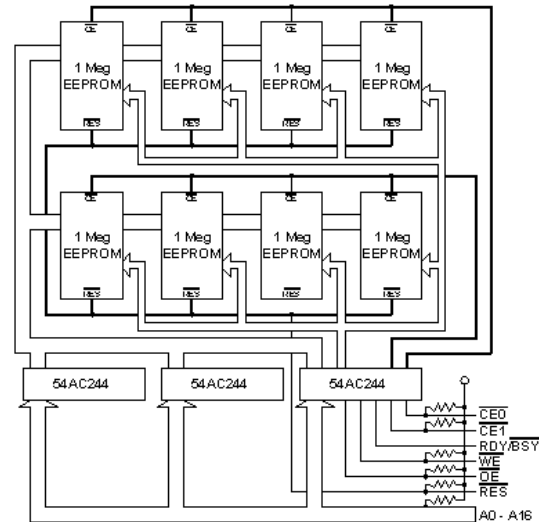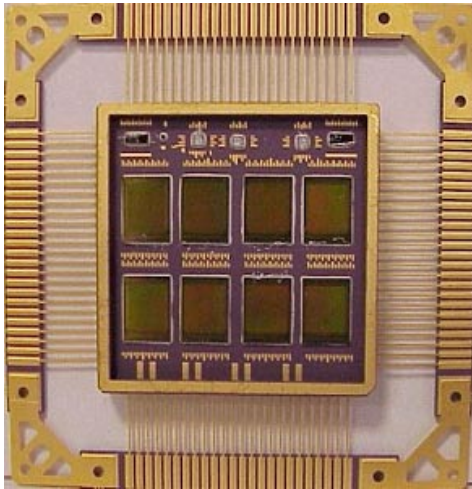## 8 Megabit (256K x 32-Bit)
Low Voltage EEPROM MCM

FEATURES:

- 256k x 32-bit EEPROM MCM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - >100 krad (Si)
  - Dependent upon orbit
- Excellent Single event effects
  - SEL_{TH} > 84.7 MeV/mg/cm^2
  - SEU > 26.6 MeV/mg/cm^2 read mode
  - SEU = 11.4 MeV/mg/cm^2 write mode
- High endurance
  - 10,000 cycles/dword, 10 year data retention
- Page Write Mode: 2 X 128 dword page
- High Speed:
  - 200 and 250 ns maximum access times
- Automatic programming
  - 15 ms automatic Page/dword write

DESCRIPTION:

Maxwell Technologies' 79LV0832 multi-chip module (MCM) memory features a greater than 100 krad (Si) total dose tolerance, dependent upon orbit. Using Maxwell Technologies' patented radiation-hardened RAD-PAK® MCM packaging technology, the 79LV0832 is the first radiation-hardened 8 megabit MCM EEPROM for space application. The 79LV0832 uses eight 1 Megabit high speed CMOS die to yield an 8 megabit product. The 79LV0832 is capable of in-system electrical dword and page programmability. It has a 128 x 32 byte page programming function to make its erase and write operations faster. It also features Data Polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 79LV0832, hardware data protection is provided with the RES pin. Software data protection is implemented using the JEDEC standard algorithm.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK®' provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to MAxwell Technologies self-defined Class K.
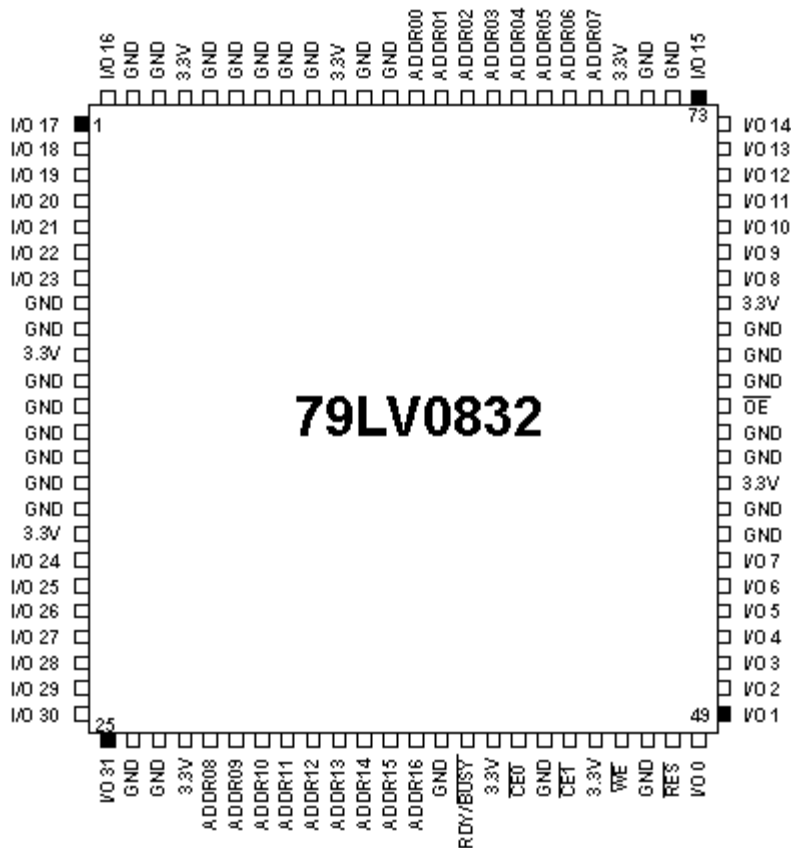
TABLE 1. 79LV0832 PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
84-77, 29-37	ADDR0 to ADDR16	Address Input
48-55, 66-73, 96, 1-7, 18-25	I/O0 to I/O31	Data Input/Output
61	$\overline{OE}$	Output Enable
41, 43	$\overline{CE0\text{-}1}$	Chip Enable 0 through 1
45	$\overline{WE}$	Write Enable
10, 17, 28, 40, 44, 58, 65, 76, 87, 93	3.3V	Power Supply
8, 9, 11-16, 26, 27, 38, 42, 46, 56, 57, 59, 60, 62-64, 74, 75, 85, 86, 88-92, 94, 95	GND	Ground
39	RDY/$\overline{BUSY}$	Ready/Busy
47	$\overline{RES}$	Reset

TABLE 2. 79LV0832 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	-0.6		7.0	V
Input Voltage	V_{IN}	-0.5[1]		7.0	V
Package Weight	RP		45		Grams
	RT		38		
Thermal Impedance (RP and RT Packages; XP TBD)	Φ_{JC}		3		˚C/W
Operating Temperature Range	T_{OPR}	-55		125	˚C
Storage Temperature Range	T_{STG}	-65		150	˚C

1. V_{IN} min = -3.0V for pulse width $\leq$50ns.

TABLE 3. 79LV0832 RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	3.0	3.6	V
Input Voltage	V_{IL}	-0.3[1]	0.8	V
	V_{IH}	2.2	V_{CC} +0.3	V
$\overline{RES\_PIN}$	V_H	V_{CC}-0.5	V_{CC} +1	V
Operating Temperature Range	T_{OPR}	-55	125	˚C

1. V_{IL} min = -1.0V for pulse width $\leq$ 50 ns

TABLE 4. DELTA LIMITS[1]

PARAMETER	VARIATION[2]
I_{CC1A}	+/- 10 %
I_{CC2A}	+/- 10 %
I_{CC2C}	+/- 10 %
I_{LI} - ADDR, CE, OE, WE	+/- 10 %
I_{Lo} - D0 - D31	+/- 10 %

1. Delta limits are calculated from test data taken at preburn-in and post burn-in as defined in MIL-STD-883

2. Specified value in Table 6

TABLE 5. 79LV0832 CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance: V_{IN} = 0V[1]	C_{IN}	--	6	pF
	C_{IN} OE	--	6	
	C_{IN} $\overline{WE}$	--	6	
	C_{IN} $\overline{CE}_{0-1}$	--	6	
	C_{IN} A0-A16	--	6	
	C_{IN} $\overline{RES}$	--	48	
Output Capacitance: V_{OUT} = 0V[1]	C_{Out} RDY/BSY	--	6	pF
	C_{Out} D0-D31	--	12	

1. Guaranteed by design.

TABLE 6. 79LV0832 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Input Leakage Current[1] A0-A16, $\overline{CE}$,$\overline{WE}$, $\overline{OE}$	V_{IN} = V_{CC}	I_{LI}	1, 2, 3	--	4[2]	µA
	V_{IN}=V_{IH}				720[2]	µA
	V_{IN}=0V				720[2]	µA
Input Leakage Current D0-D31	V_{IN}=V_{CC}	I_{LI}	1, 2, 3		4	µA
Output Leakage Current	(V_{CC} = 3.6V, V_{OUT} = 3.6V/0.4V)	I_{LO}	1, 2, 3	--	4	µA
Standby V_{CC} Current[1]	$\overline{CE}$ = ADDR=$\overline{WE}$=$\overline{OE}$ =V_{CC}	I_{CC1A}	1, 2, 3	--	80	µA
	$\overline{CE}$ = ADDR=$\overline{WE}$=$\overline{OE}$ =V_{IH}	I_{CC1B}		--	15	mA
	$\overline{CE}$ = V_{IH}; ADDR=$\overline{WE}$=$\overline{OE}$ =0V	I_{CC1C}		--	15	mA
Operating V_{CC} Current[1,3]	$\overline{OE}$ = 0V; ADDR=$\overline{WE}$=V_{CC} I_{OUT} = 0mA, $\overline{CE}$ Duty = 100%, Cycle = 1 us at V_{CC} = 3.6V	I_{CC2A}	1, 2, 3		24	mA
	$\overline{OE}$ =ADDR=$\overline{WE}$=0V I_{OUT} = 0mA, $\overline{CE}$ Duty = 100%, Cycle = 1 us at V_{CC} = 3.6V	I_{CC2B}	1, 2, 3	--	40	mA
	$\overline{OE}$ = 0V; ADDR=$\overline{WE}$=V_{CC} I_{OUT} = 0mA, $\overline{CE}$ Duty = 100%, Cycle = 200 ns at V_{CC} =3.6V	I_{CC2C}	1, 2, 3		60	mA
	$\overline{OE}$ =ADDR=$\overline{WE}$=0V I_{OUT} = 0mA, $\overline{CE}$ Duty = 100%, Cycle = 200 ns at V_{CC} = 3.6V	I_{CC2D}	1, 2, 3	--	100	mA
Input Voltage $\overline{RES}$_PIN		V_{IL} V_{IH} V_H	1, 2, 3	2.2 V_{CC} -0.5	0.8	V

TABLE 6. 79LV0832 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	TEST CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Output Voltage	Data Lines: V_{CC}Min, I_{OL} = 2.1mA	V_{OL}	1, 2, 3	--	0.4	V
	RDY/BSY_Line: V_{CC} Min, I_{OL} = 12mA	V_{OL}			0.4	V
	Data Lines: V_{CC} Min, I_{OH} = -400µA	V_{OH}		2.4	--	V
	RDY/BSY_Line: V_{CC} Min, I_{OH} = -12mA	V_{OH}		2.4	--	V
	All Outputs: V_{CC}Min, I_{OH}=-100uA			V_{CC}-0.3V		V

1. All Inputs are tied to Vcc with a 5.5KΩ resistor, except for RES which is 30KΩ.

2. For RES I_{LI}=800uA max.

3. Only one $\overline{CE}$ active (low) at a time

TABLE 7. 79LV0832 AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION [1]

(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Address Access Time $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{ACC}	9, 10, 11	 -- --	 200 250	ns
Chip Enable Access Time $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{CE}	9, 10, 11	 -- --	 200 250	ns
Output Enable Access TIme $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{OE}	9, 10, 11	 0 0	 110 120	ns
Output Hold to Address Change $\overline{CE}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{OH}	9, 10, 11	 0 0	 -- --	ns
Output Disable to High-Z [2] $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{DF}	9, 10, 11	 0 0	 50 50	ns
$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{DFR}		 0 0	 300 350	ns
$\overline{RES}$ to Output Delay $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}[3] -200 -250	T_{RR}	9, 10, 11	 0 0	 525 550	ns

1. Test conditions: input pulse levels = 0.4V to 2.2V; input rise and fall times $\leq$ 20 ns; output load = 1 TTL gate + 100 pF (including scope and jig); reference levels for measuring timing = 0.8 V/1.8 V.

2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.

3. Guaranteed by design.

TABLE 8. 79LV0832 AC ELECTRICAL CHARACTERISTICS
PAGE/DWORD ERASE AND PAGE/DWORD WRITE OPERATION
(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN [1]	MAX	UNITS

Address Setup Time
  -200
  -250
	t_{AS}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Chip Enable to Write Setup Time ($\overline{WE}$ controlled)
  -200
  -250
	t_{CS}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Write Pulse Width
$\overline{CE}$ controlled
  -200
  -250
$\overline{WE}$ controlled
  -200
  -250
	
	t_{CW}
	
	t_{WP}
		9, 10, 11	
			
			200
			250
			
			200
			250
				
				--
				--
				
				--
				--
					ns
					
					ns

Address Hold Time
  -200
  -250
	t_{AH}	9, 10, 11	
			200
			250
				
				--
				--
					ns

Data Setup Time
  -200
  -250
	t_{DS}	9, 10, 11	
			150
			200
				
				--
				--
					ns

Data Hold Time
  -200
  -250
	t_{DH}	9, 10, 11	
			10
			10
				
				--
				--
					ns

Chip Enable Hold Time ($\overline{WE}$ controlled)
  -200
  -250
	t_{CH}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Write Enable to Write Setup Time ($\overline{CE}$ controlled)
  -200
  -250
	t_{WS}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Write Enable Hold Time ($\overline{CE}$ controlled)
  -200
  -250
	t_{WH}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Output Enable to Write Setup Time
  -200
  -250
	t_{OES}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Output Enable Hold Time
  -200
  -250
	t_{OEH}	9, 10, 11	
			0
			0
				
				--
				--
					ns

Write Cycle Time [2]
  -200
  -250
	t_{WC}	9, 10, 11	
			--
			--
				
				15
				15
					ms

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TABLE 8. 79LV0832 AC ELECTRICAL CHARACTERISTICS
PAGE/DWORD ERASE AND PAGE/DWORD WRITE OPERATION
(V_{CC} = 3.3V ±10%, T_A = -55 TO +125°C)

PARAMETER	SYMBOL	SUBGROUPS	MIN [1]	MAX	UNITS
Data Latch Time -200 -250	t_{DL}	9, 10, 11	700 750	-- --	ns
Byte Load Window -200 -250	t_{BL}	9, 10, 11	100 200	-- --	µs
Byte Load Cycle -200 -250	t_{BLC}	9, 10, 11	1 1	30 30	µs
Time to Device Busy -200 -250	t_{DB}	9, 10, 11	100 120	-- --	ns
Write Start Time [3] -200 -250	t_{DW}	9, 10, 11	250 250	-- --	ns
$\overline{RES}$ to Write Setup Time[4] -200 -250	t_{RP}	9, 10, 11	100 100	-- --	µs
V_{CC} to $\overline{RES}$ Setup Time[4] -200 -250	t_{RES}	9, 10, 11	1 1	-- --	µs

1. Use this device in a longer cycle than this value.

2. t_{WC} must be longer than this value unless polling techniques or RDY/BUSY are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/BUSY are used.

4. Guaranteed by desgin.

TABLE 9. 79LV0832 MODE SELECTION [1, 2]

PARAMETER	$\overline{CE}$ [3]	$\overline{OE}$	$\overline{WE}$	I/O	$\overline{RES}$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_H	V_{OH}
Standby	V_{IH}	X	X	High-Z	X	V_{OH}
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_H	$V_{OH} \rightarrow V_{OL}$
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	V_{OH}
Write Inhibit	X	X	V_{IH}	--	X	--
	X	V_{IL}	X	--	X	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O7)	V_H	V_{OL}
Program Reset	X	X	X	High-Z	V_{IL}	V_{OH}

1. X = Don't care.
2. Refer to the recommended DC operating conditions.
3. For $\overline{CE}_{0-1}$ only one $\overline{CE}$ can be enabled (Low) at a time.

FIGURE 1. READ TIMING WAVEFORM
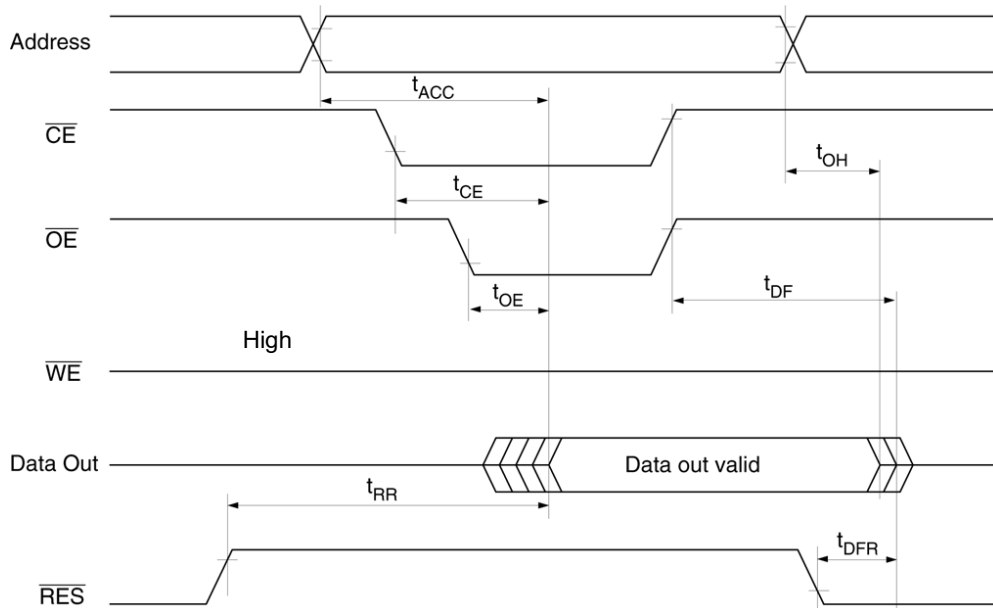
FIGURE 2. DWORD WRITE TIMING WAVEFORM (1) ($\overline{\text{WE}}$ CONTROLLED)
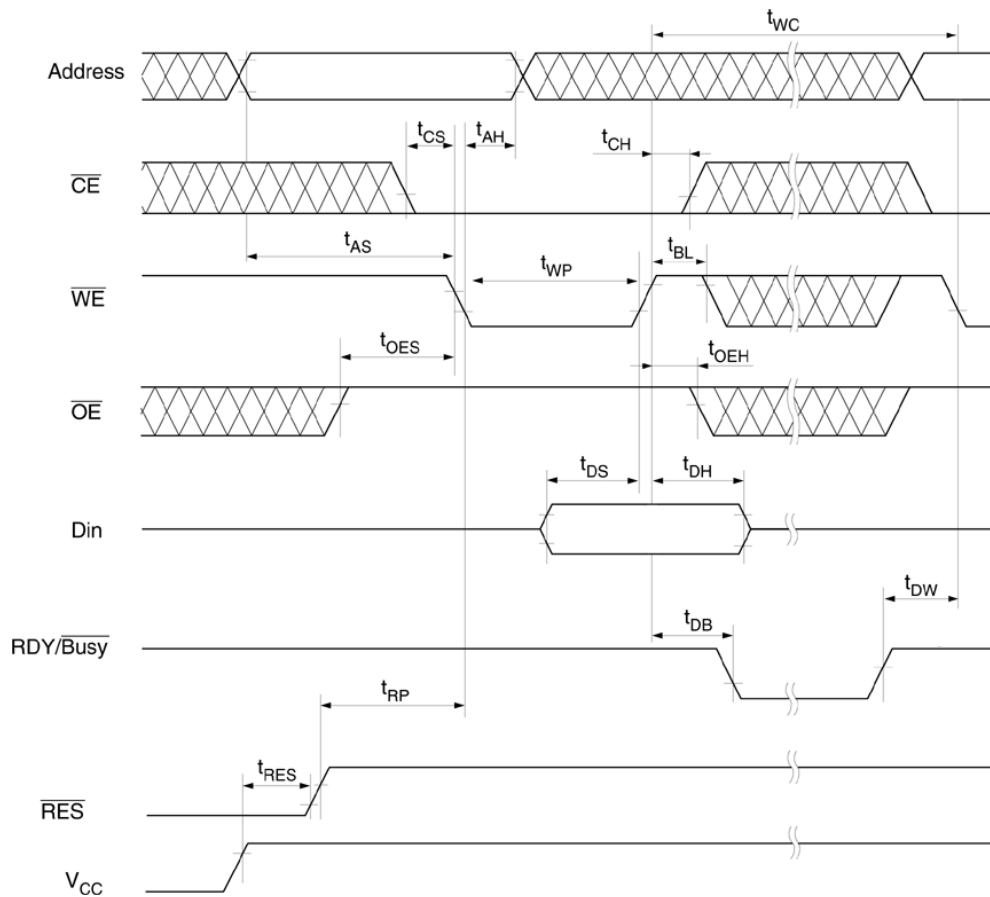
FIGURE 3. DWORD WRITE TIMING WAVEFORM (2) (CE CONTROLLED)
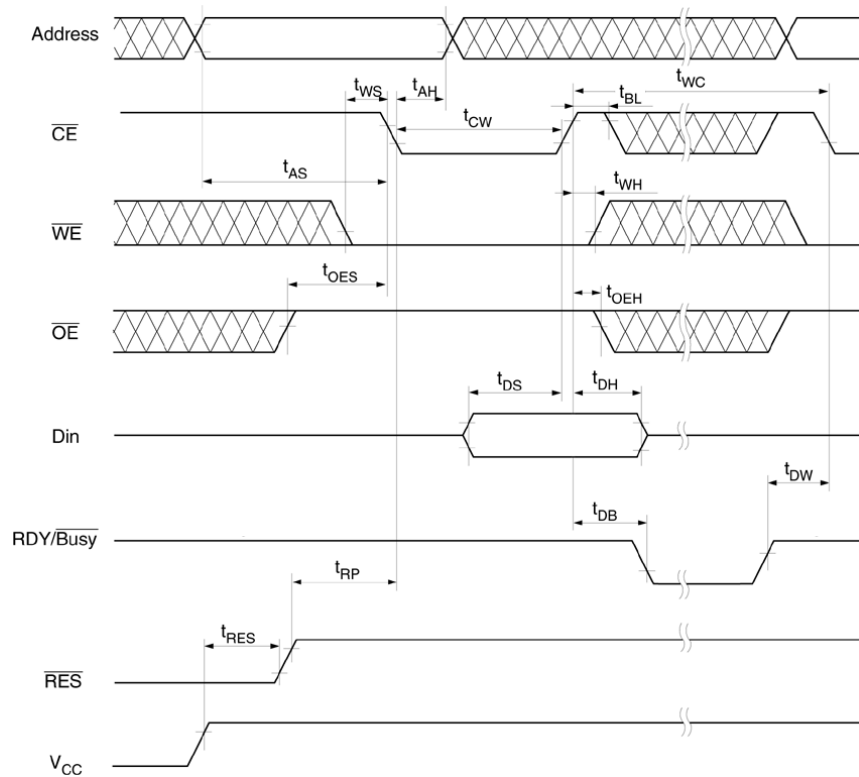
FIGURE 4. PAGE WRITE TIMING WAVEFORM (1) (WE CONTROLLED)

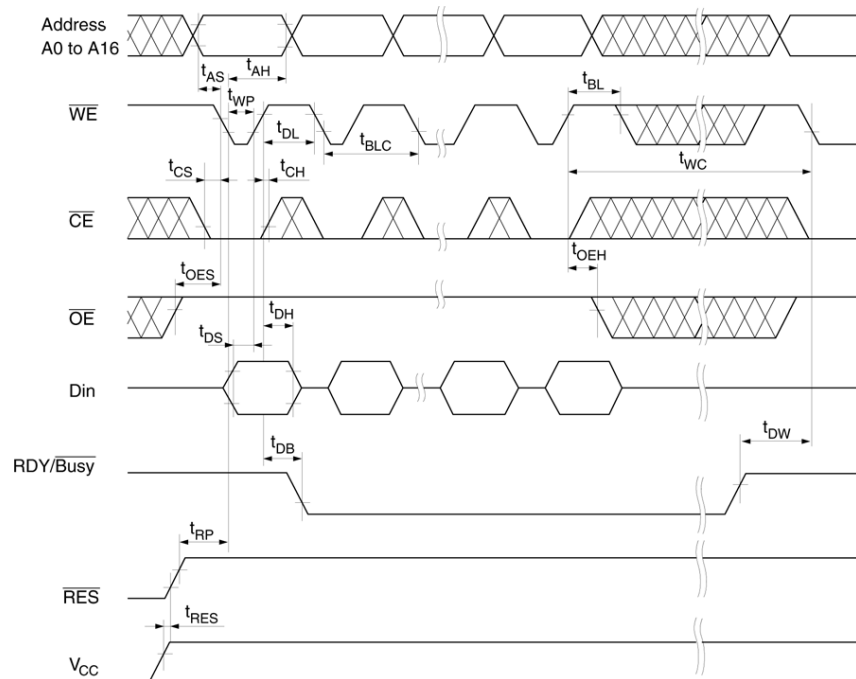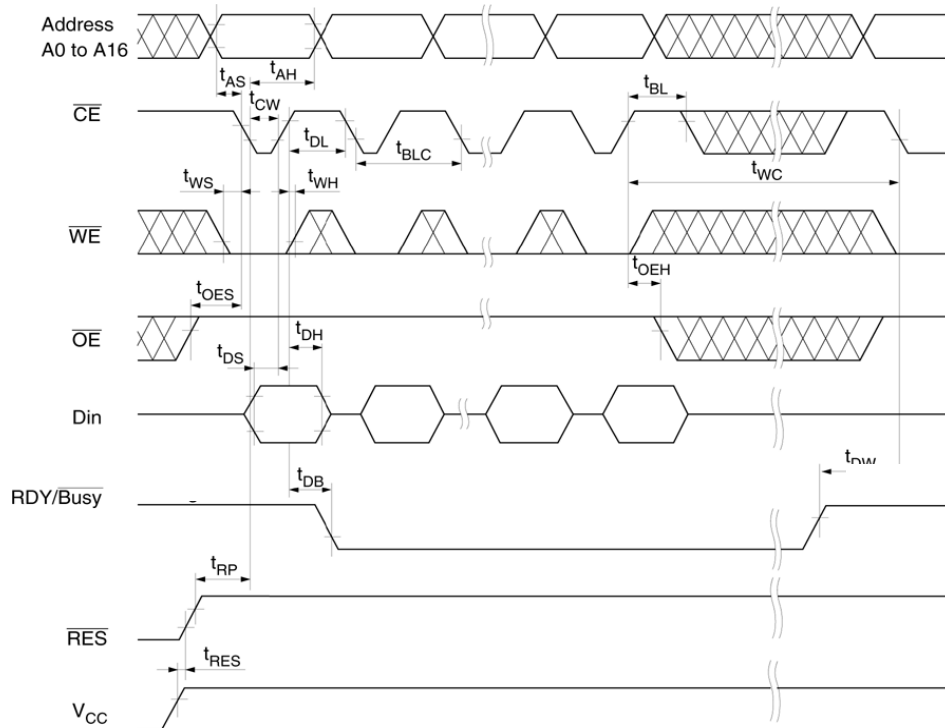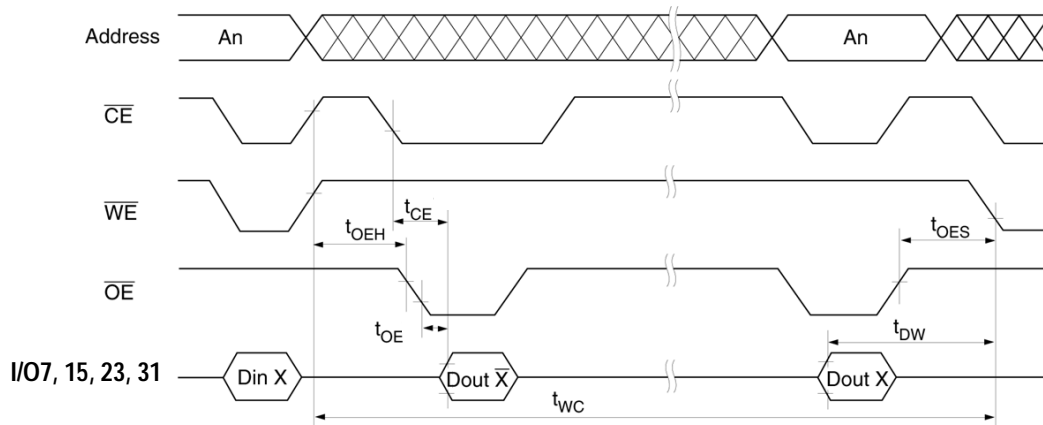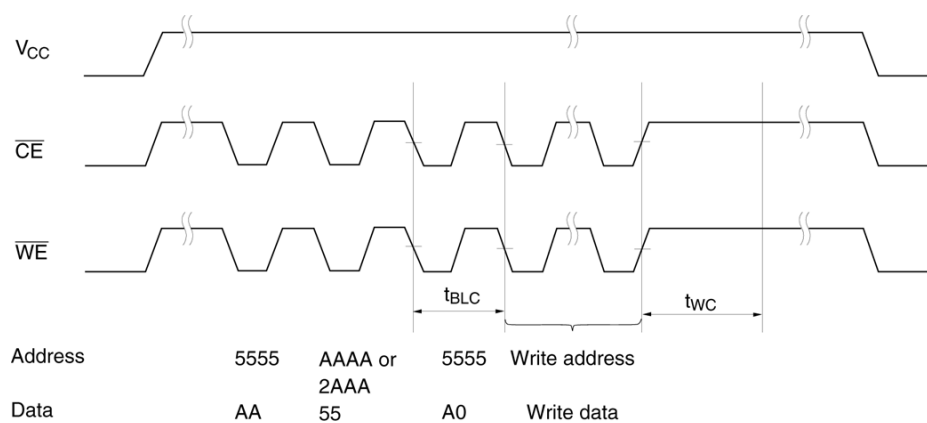FIGURE 5. PAGE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)[1,2]

1) A7-A16 ARE PAGE ADDRESSES AND MUST BE THE SAME WITHIN A PAGE WRITE OPERATION

2) REFER TO TABLE 7 AND 8 FOR TIMING CHARACTERISTICS

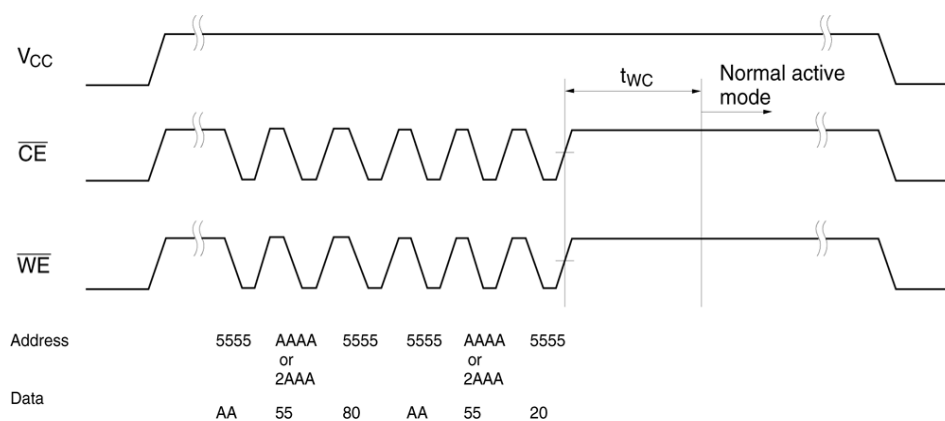FIGURE 6. $\overline{DATA}$ POLLING TIMING WAVEFORM[1]

1) REFER TO TABLE 7 AND 8 FOR TIMING CHARACTORISTICS

FIGURE 7. SOFTWARE DATA PROTECTION TIMING WAVEFORM (1) (IN PROTECTION MODE)[1]

1)REPEAT THE DATA PATTERN IN EACH OF THE FOUR BYTES.

FIGURE 8. SOFTWARE DATA PROTECTION WAVEFORM (2) (IN NON-PROTECTION MODE)[1]

1) REPEAT THE DATA PATTERN IN EACH OF THE FOUR BYTES.

EEPROM APPLICATION NOTES

This application note describes the programming procedures for the EEPROM modules and with details of various techniques to preserve data integrity.

Automatic Page Write

Page-mode write feature allows 1 to 128 dwords of data to be written into the EEPROM in a single write cycle. Loading the first dword of data, the data load window opens 30µs for the second dword. In the same manner each additional dword of data can be loaded within 30µs of the preceding falling edge of either $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ and $\overline{WE}$ are kept

high for 100µs after data input, the EEPROM enters the write mode automatically and the data input is written into the EEPROM.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Data Polling

Data Polling function allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last dword of data to be loaded outputs from I/O 7, 15, 23, 31 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

RDY/$\overline{Busy}$ signal also allows a comparison operation to determine the status of the EEPROM. The RDY/$\overline{Busy}$ signal goes low ($V_{OL)}$ after the first write signal. At the end of the write cycle, the RDY/$\overline{Busy}$ returns to a high state (V_{OH}).

$\overline{RES}$ Signal

When $\overline{RES}$ is LOW (V_L), the EEPROM cannot be read or programmed. The EEPROM data must be protected by keeping $\overline{RES}$ low when V_{CC} is power on and off. $\overline{RES}$ should be high (V_H) during read and programming operations.
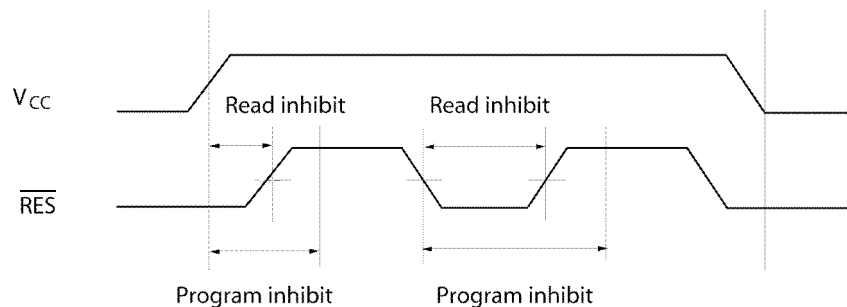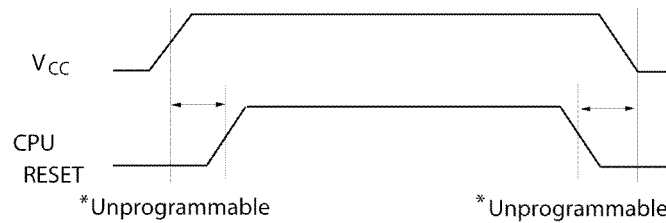

Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

1. Data Protection at V_{CC} on/off

   When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state during V_{CC} on/off by using a CPU reset signal to $\overline{RES}$ pin.

Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

1. Data Protection against Noise of Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.

   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.
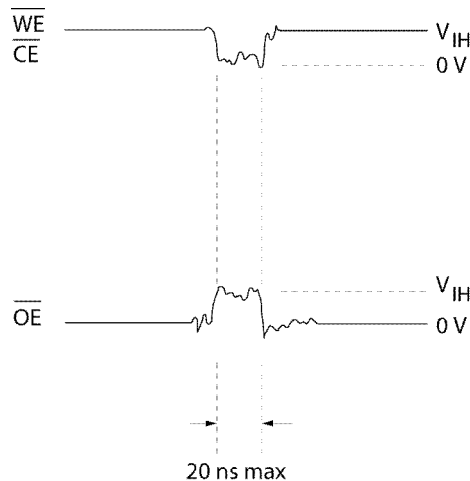
2. $\overline{RES}$ Signal

   $\overline{RES}$ should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when $\overline{RES}$ become low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. RES should be kept high for 10 ms after the last data is input

.
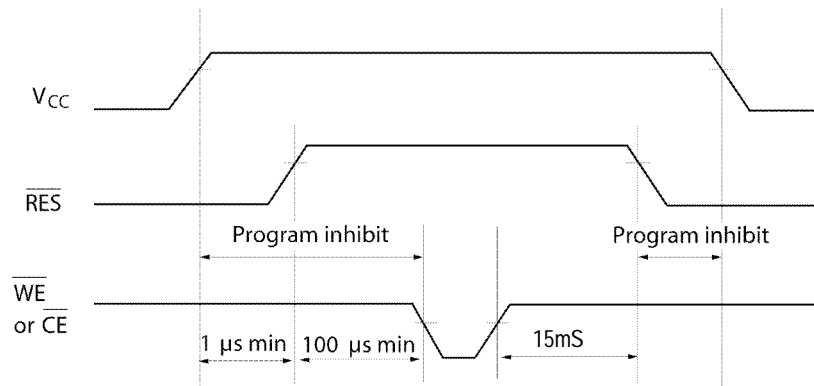
3. Software Data Protection Enable

The 79LV0832 contains a software controlled write protection feature that allows the user to inhibit all write operations to the device. This is useful in protecting the device from unwanted write cycles due to uncontrollable circuit noise or inadvertent writes caused by minor bus contentions. Software data protection is enabled by writing the following data sequence to the EEPROM and allowing the write cycle period (t_{WC}) of 10ms to elapse:

.

Software Data Protection Enable Sequence

Address	Data
5555	AA AA AA AA
AAAA or 2AAA	55 55 55 55
5555	A0 A0 A0 A0

4. Writing to the Memory with Software Data Protection Enabled

To write to the device once Software protection is enabled, the enable sequence must precede the data to be written. This sequence allows the write to occur while at the same time keeping the software protection enabled

Sequence for Writing Data with Software Protection Enabled.

| Address	Data
5555	AA AA AA AA
AAAA or 2AAA	55 55 55 55
5555	A0 A0 A0 A0
Write Address(s)	Normal Data Input

5. Disabling Software Protection

Software data protection mode can be disabled by inputting the following data sequence. Once the software protection sequence has been written, no data can be written to the memory until the write cycle (T_{WC}) has elapsed.

Software Protection Disable Sequence

| Address	Data
5555	AA AA AA AA
AAAA or 2AAA	55 55 55 55
5555	80 80 80 80
5555	AA AA AA AA
AAAA or 2AAA	55 55 55 55
5555	20 20 20 20

Devices are shipped in the "unprotected" state, meaning that the contents of the memory can be changed as required by the user. After the software data protection is enabled, the device enters the Protect Mode where no further write commands have any effect on the memory contents.
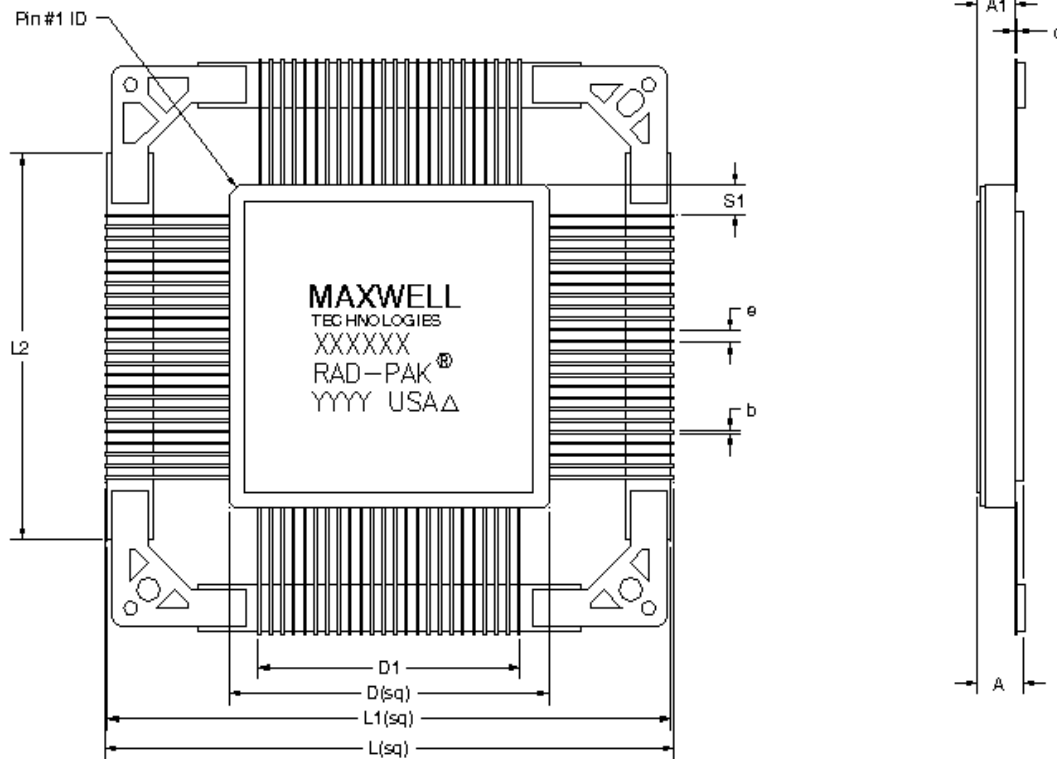
96-PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	.184	.200	.216
b	.010	.012	.013
c	---	.009	.012
D	1.408	1.420	1.432
D1		1.162	
e		.050	
S1		.129	
L	---	2.528	2.543
L1	2.485	2.500	2.505
L2	---	1.700	
A1	.152	.165	.178
N		96	

Note: All dimensions in inches

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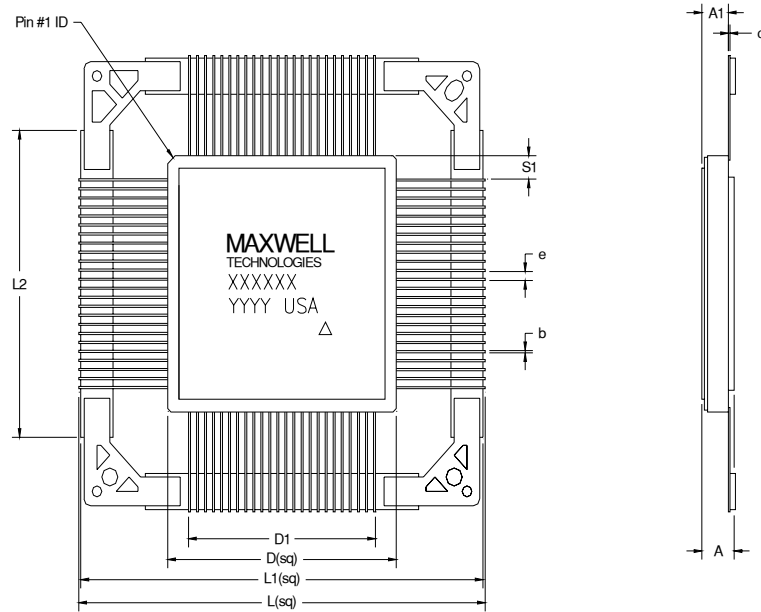
96 PIN RAD-TOLERANT QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	.167	.183	.199
b	.010	.012	.013
c	--	.009	.012
D	1.408	1.420	1.432
D1	1.162		
e	.050		
S1	.129		
L	--	2.528	2.543
L1	2.485	2.500	2.505
L2	--	1.700	--
A1	.152	.165	.178
N	96		

Note: All dimensions in inches
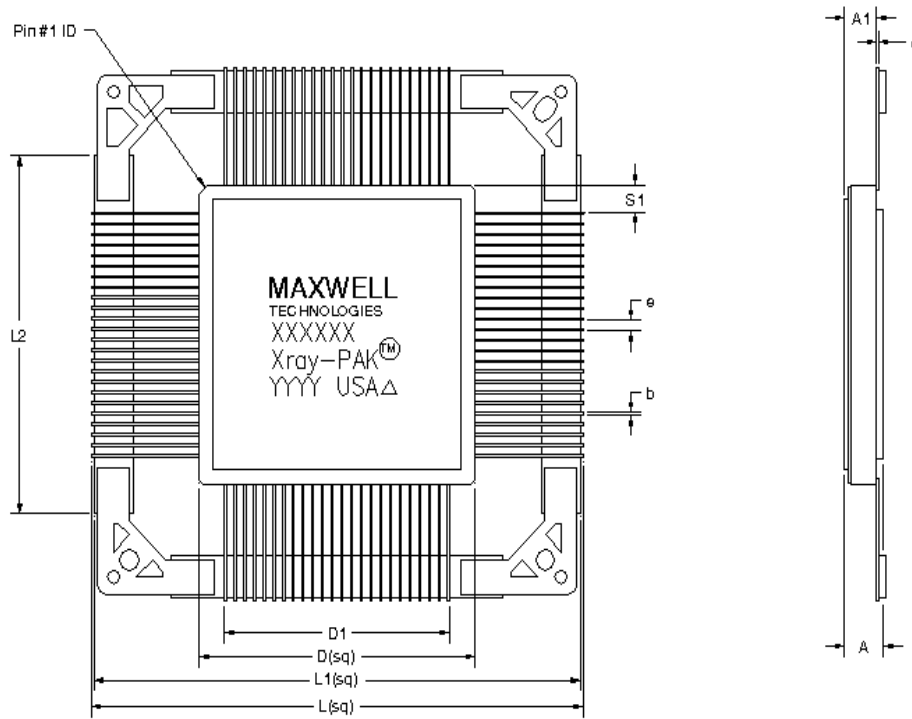
96 PIN XRAY™ QUAD FLAT PACKAGE

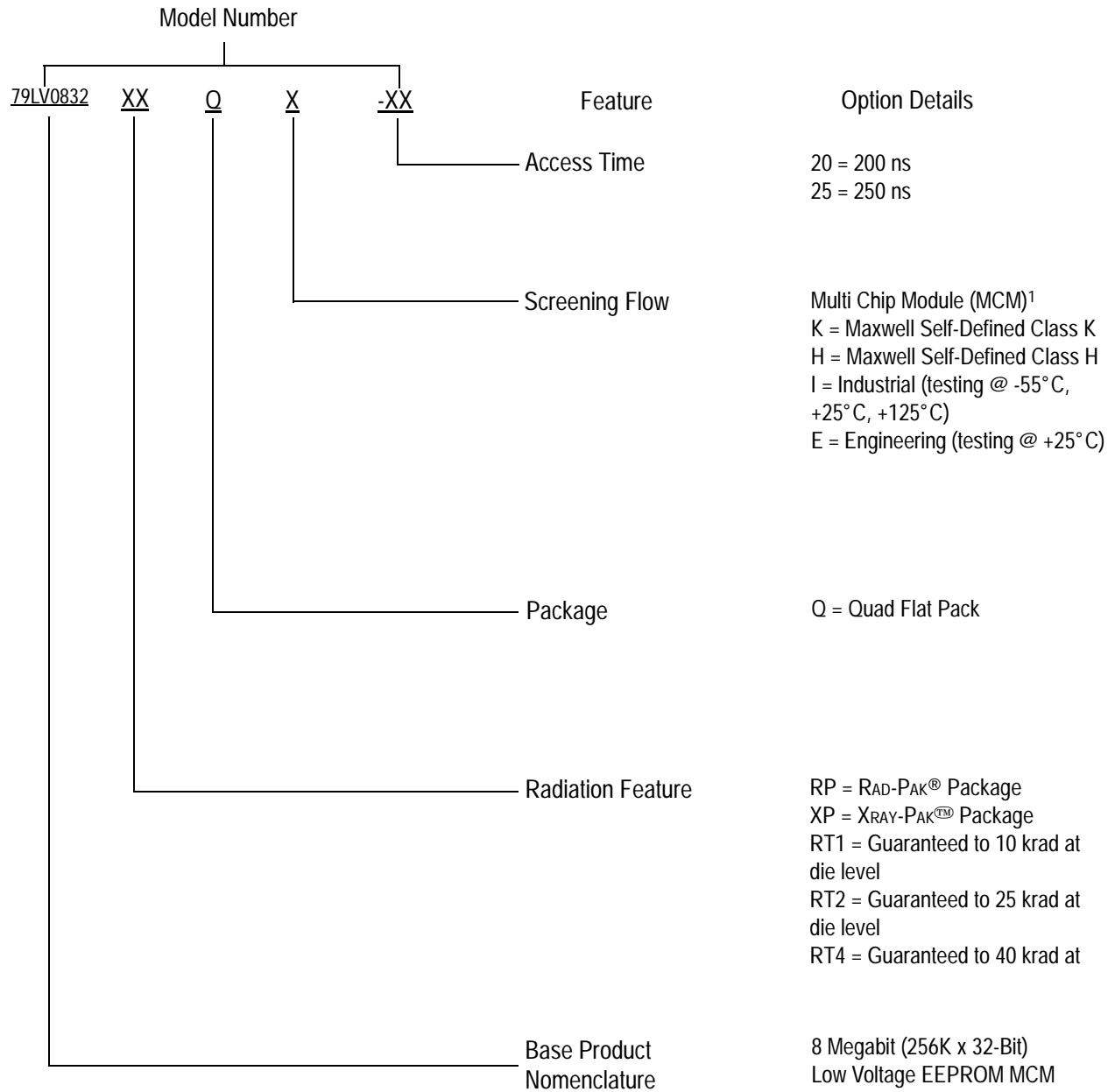| SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	.200	.222	.245
b	.007	.010	.013
c	.009	.009	.012
D	1.690	1.707	1.725
D1	1.150		
e	0.050		
S1	.278		
L	3.000	3.020	3.040
L1	2.985	3.000	3.005
L2	2.090	2.200	2.210
A1	.115	.130	.145
N	96		

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

Product Ordering Options

Model Number

79LV0832   XX   Q   X   -XX   Feature   Option Details

Access Time   20 = 200 ns
                     25 = 250 ns

Screening Flow   Multi Chip Module (MCM)[1]
                        K = Maxwell Self-Defined Class K
                        H = Maxwell Self-Defined Class H
                        I = Industrial (testing @ -55°C, +25°C, +125°C)
                        E = Engineering (testing @ +25°C)

Package   Q = Quad Flat Pack

Radiation Feature   RP = RAD-PAK® Package
                           XP = XRAY-PAK™ Package
                           RT1 = Guaranteed to 10 krad at die level
                           RT2 = Guaranteed to 25 krad at die level
                           RT4 = Guaranteed to 40 krad at

Base Product   8 Megabit (256K x 32-Bit)
Nomenclature   Low Voltage EEPROM MCM

1) Products are manufactured and screened to Maxwell Technologies self-defined Class H and Class K flows.