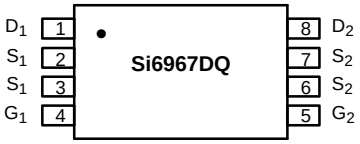
Dual P-Channel 1.8-V (G-S) MOSFET

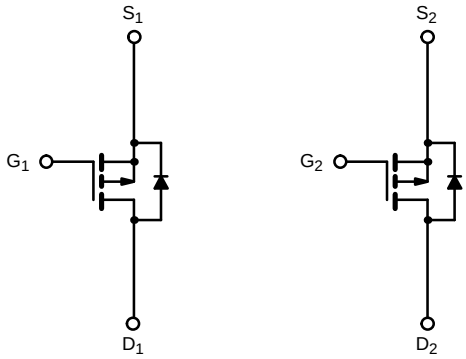
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–8	0.030 @ V_{GS} = –4.5 V	±5.0
	0.045 @ V_{GS} = –2.5 V	±4.0
	0.070 @ V_{GS} = –1.8 V	±3.0

TrenchFET® Power MOSFETs
1.8-V Rated

TSSOP-8



Top View



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–8	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a, b]	T_A = 25°C	I_D	±5.0	A
	T_A = 70°C		±4.0	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a, b]		I_S	–1.25	
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	1.1	W
	T_A = 70°C		0.72	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}		110	°C/W
	Steady State		115		

Notes
a. Surface Mounted on FR4 Board.
b. t ≤ 10 sec.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

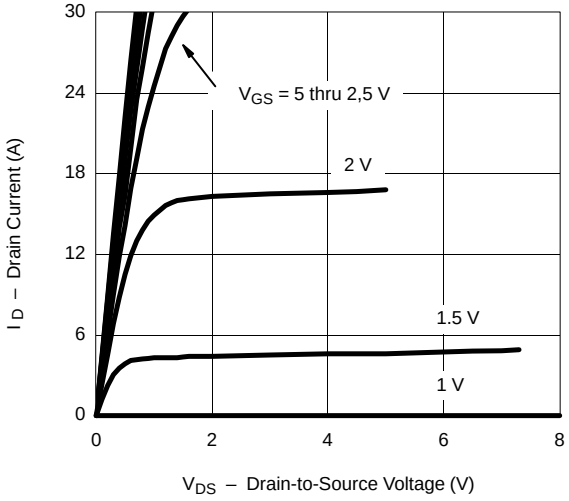
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 µA	–0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –6.4 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –6.4 V, V_{GS} = 0 V, T_J = 70°C			–25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ –8 V, V_{GS} = –4.5 V	–30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –5.0 A		0.024	0.030	Ω
		V_{GS} = –2.5 V, I_D = –4.0 A		0.033	0.045	
		V_{GS} = –1.8 V, I_D = –3.0 A		0.048	0.070	
Forward Transconductance[a]	g_{fs}	V_{DS} = –8 V, I_D = –5.0 A		18		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.25 A, V_{GS} = 0 V		–0.68	–1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –5.0 A		20	40	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			3.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		20	50	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			85	150	
Fall Time	t_f			50	90	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.25 A, di/dt = 100 A/µs		50	100	

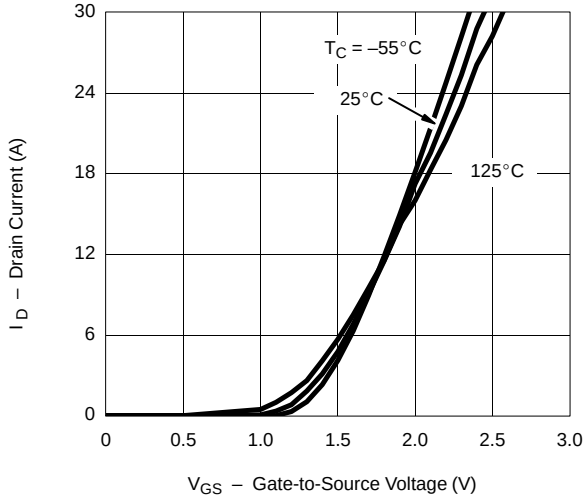
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

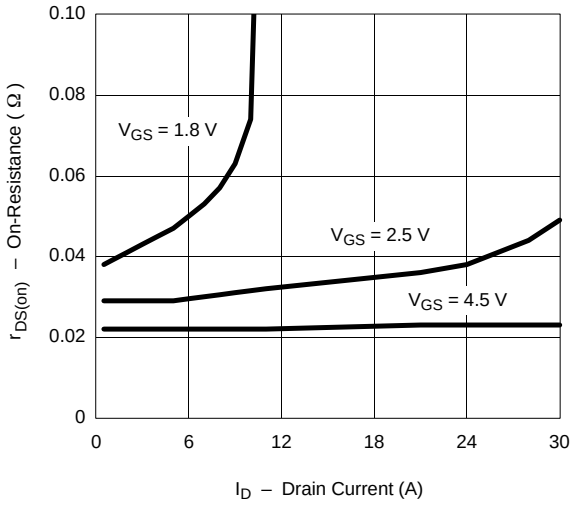
Output Characteristics



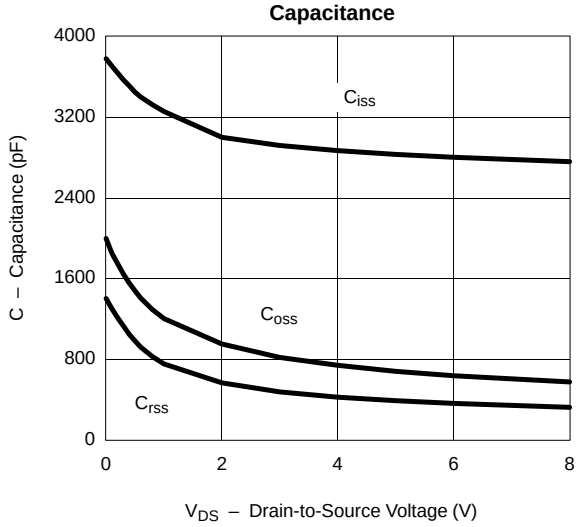
Transfer Characteristics



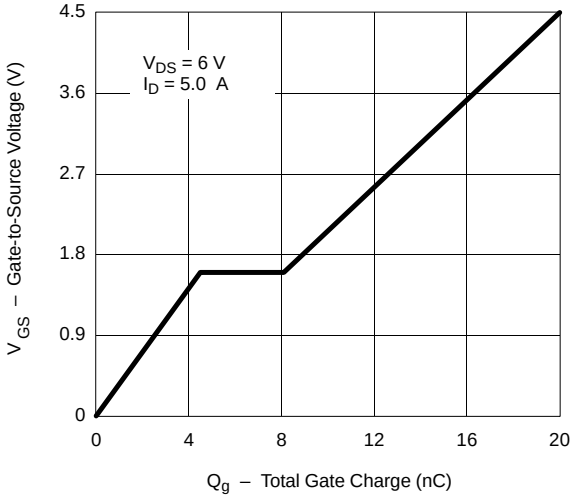
On-Resistance vs. Drain Current



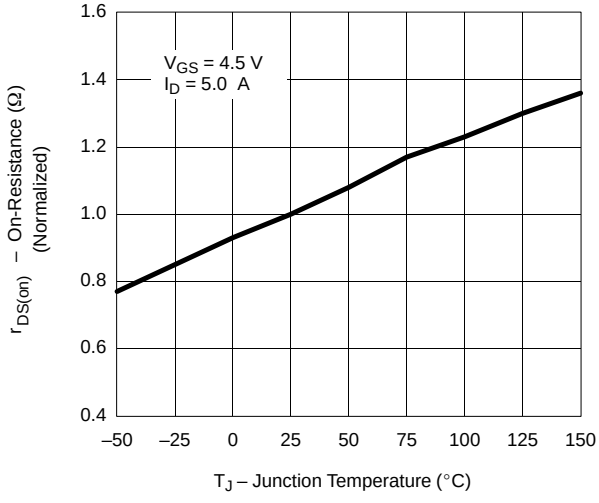
Capacitance



Gate Charge

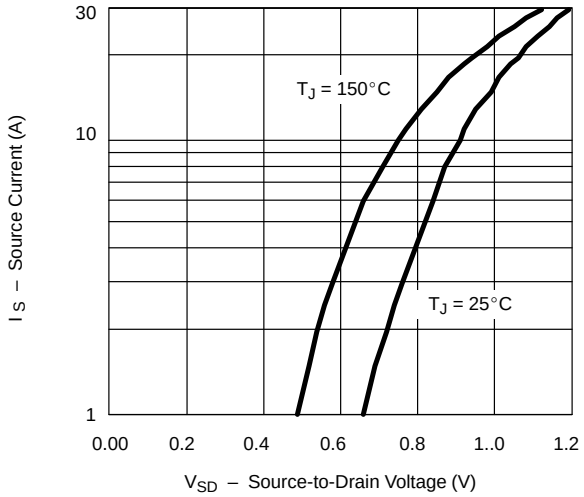


On-Resistance vs. Junction Temperature

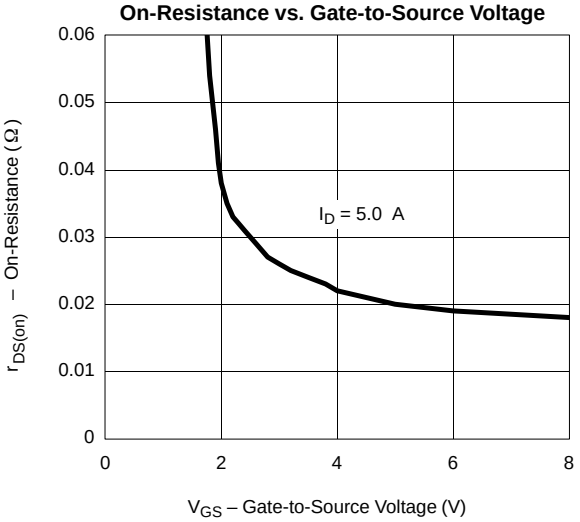


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

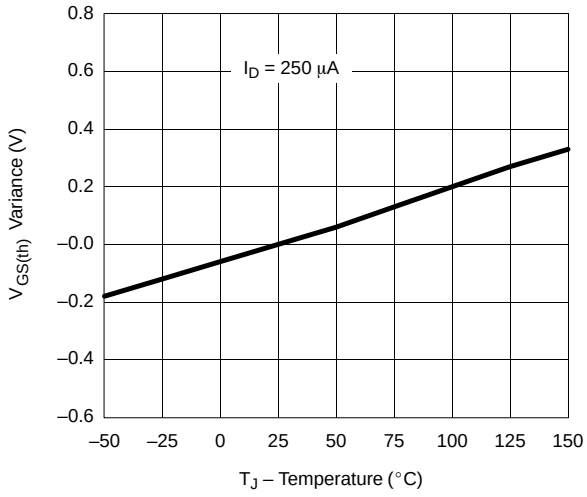
Source-Drain Diode Forward Voltage



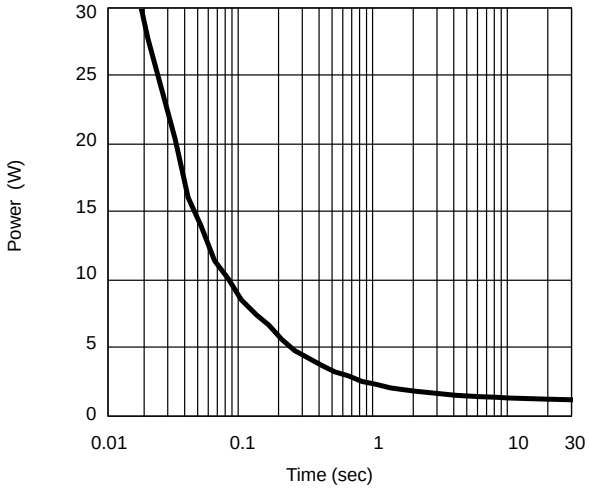
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient