NEC

MOS INTEGRATED CIRCUIT

μPD168002

MONOLITHIC 6-CHANNEL H-BRIDGE DRIVER

DESCRIPTION

The μPD168002 is a monolithic 6-channel H-bridge driver that consists of a CMOS control circuit and a MOS output stage. It can reduce the current consumption and the voltage loss at the output stage compared with conventional driver using bipolar transistors, thanks to employment of a MOS process. The μPD168002 employs P-channel MOS FET in the output stage, and is eliminated the charge pump circuit. Therefore, the circuit current consumption during operation can be significantly reduced.

The package is a 48-pin TQFP that helps reduce the mounting area and height.

The μPD168002 can be used to drive one stepping motor and four DC motors, and is suitable for the motor driver of CD-ROM/CD audios.

FEATURES

- Six H-bridge circuits employing power MOS FET
- Low current consumption due to elimination of charge pump circuit
- Input logic frequency: 100 kHz supported
- 3 V power supply supported for logic

  Minimum operating supply voltage: 2.7 V
- 5 V, 10 V power supply supported for motor

  ch1, ch2, ch5 and ch6: 10 V driving

  ch3 and ch4: 5 V driving
- Undervoltage lockout circuit

  Shuts down the internal circuit at V_{DD} = 1.7 V TYP.
- Overheat protection circuit
- 48-pin TQFP (□7 mm)

ORDERING INFORMATION

Part Number	Package
μPD168002GA-9EU	48-pin plastic TQFP (fine pitch) (7 x 7)

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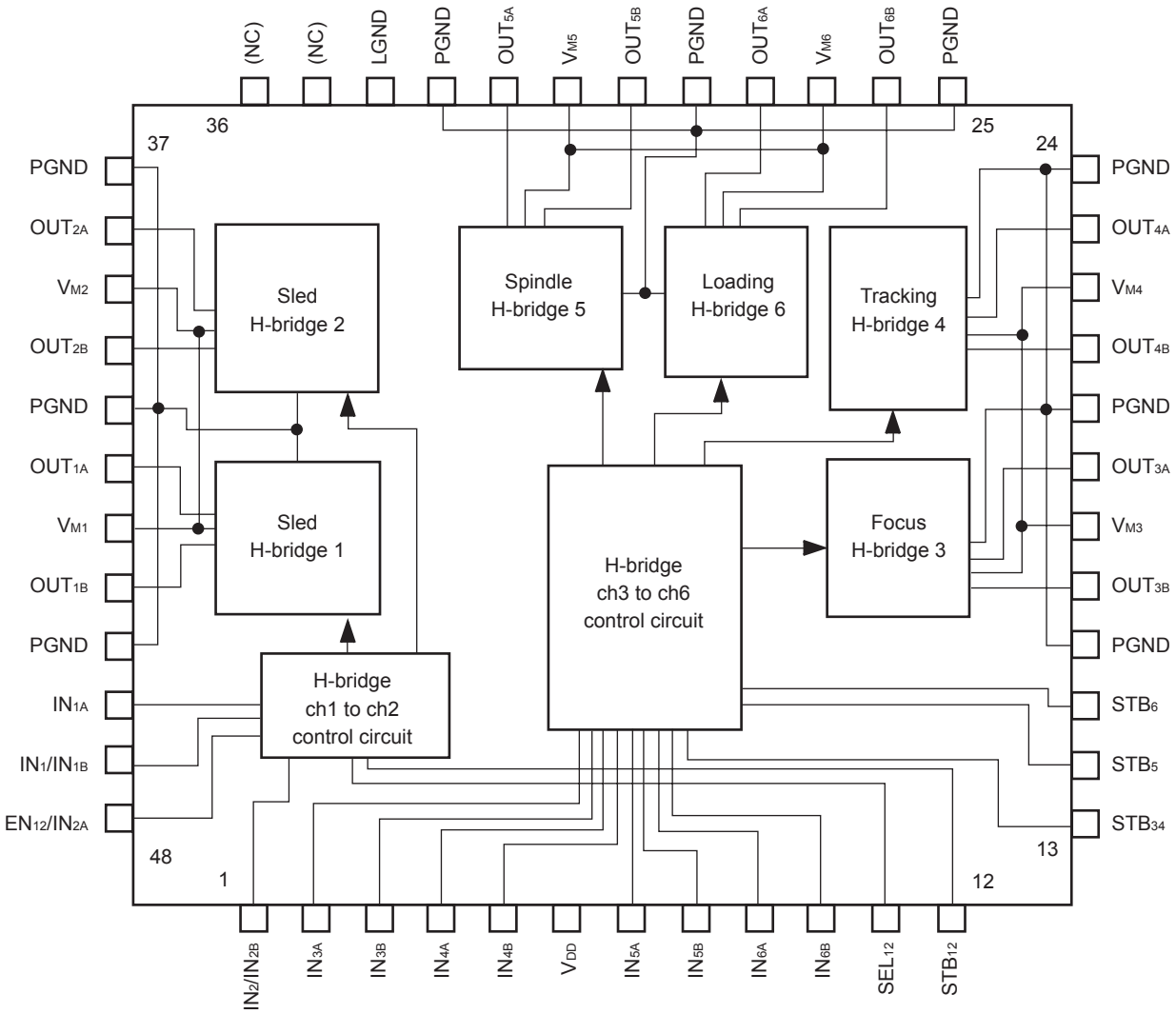
1. BLOCK DIAGRAM



Cautions 1. Be sure to connect all of the pins which have more than one.

2. A pull-down resistor (50 to 200 kΩ) is internally connected to the logic input pins.

Logic input pins: IN_{1A}, IN_1/IN_{1B}, EN_{12}/IN_{2A}, IN_2/IN_{2B}, IN_{3A}, IN_{3B}, IN_{4A}, IN_{4B}, IN_{5A}, IN_{5B}, IN_{6A}, IN_{6B}, SEL_{12}, STB_{12}, STB_{34}, STB_5 and STB_6

3. The power supply pins for motor, V_{M1} and V_{M2}, V_{M3} and V_{M4}, and V_{M5} and V_{M6}, are connected each other inside. These pins must be applied from the same potential.

2. PIN FUNCTIONS

Package: 48-pin plastic TQFP (fine pitch) (7 x 7)

(1/2)

Pin No.	Pin Name	Function
1	IN_2/IN_{2B}	ch2 input pin or ch2 input pin B
2	IN_{3A}	ch3 input pin A
3	IN_{3B}	ch3 input pin B
4	IN_{4A}	ch4 input pin A
5	IN_{4B}	ch4 input pin B
6	V_{DD}	Logic power supply pin
7	IN_{5A}	ch5 input pin A
8	IN_{5B}	ch5 input pin B
9	IN_{6A}	ch6 input pin A
10	IN_{6B}	ch6 input pin B
11	SEL_{12}	ch1 and ch2 input logic selection pin
12	STB_{12}	ch1 and ch2 standby pin
13	STB_{34}	ch3 and ch4 standby pin
14	STB_5	ch5 standby pin
15	STB_6	ch6 standby pin
16	PGND	GND pin
17	OUT_{3B}	ch3 output B
18	V_{M3}	ch3 power supply pin
19	OUT_{3A}	ch3 output A
20	PGND	GND pin
21	OUT_{4B}	ch4 output B
22	V_{M4}	ch4 power supply pin
23	OUT_{4A}	ch4 output A
24	PGND	GND pin
25	PGND	GND pin
26	OUT_{6B}	ch6 output B
27	V_{M6}	ch6 power supply pin
28	OUT_{6A}	ch6 output A
29	PGND	GND pin
30	OUT_{5B}	ch5 output B
31	V_{M5}	ch5 power supply pin
32	OUT_{5A}	ch5 output A
33	PGND	GND pin
34	LGND	GND pin
35	(NC)	Unused

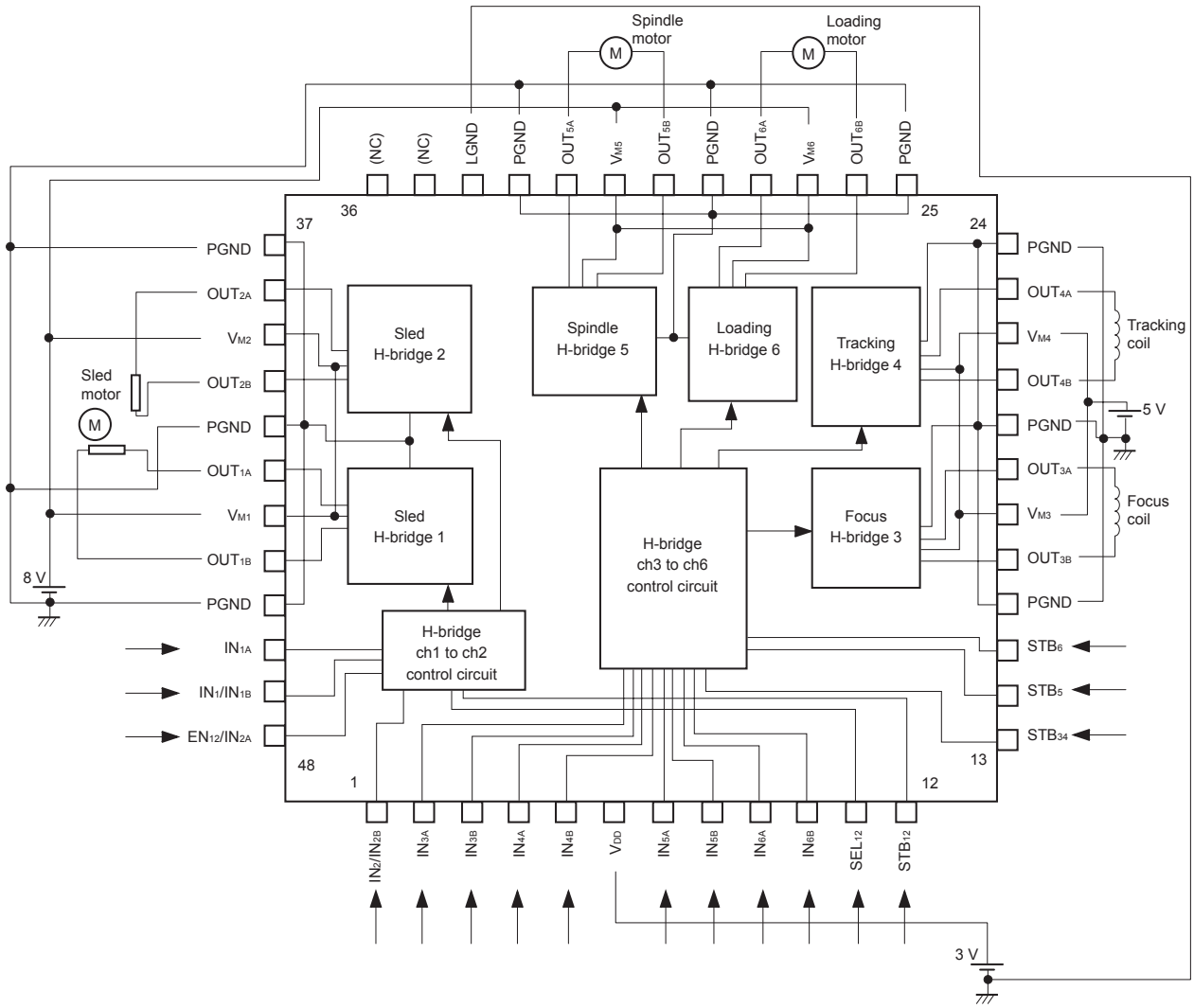
Caution Be sure to connect all of the pins which have more than one.

(2/2)

Pin No.	Pin Name	Function
36	(NC)	Unused
37	PGND	GND pin
38	OUT_{2A}	ch2 output A
39	V_{M2}	ch2 power supply pin
40	OUT_{2B}	ch2 output B
41	PGND	GND pin
42	OUT_{1A}	ch1 output A
43	V_{M1}	ch1 power supply pin
44	OUT_{1B}	ch1 output B
45	PGND	GND pin
46	IN_{1A}	ch1 input pin A
47	IN_1/IN_{1B}	ch1 input pin or ch1 input pin B
48	EN_{12}/IN_{2A}	ch1 and ch2 control pin or ch2 input pin A

Caution Be sure to connect all of the pins which have more than one.

3. STANDARD CONNECTION EXAMPLE



Caution This diagram is the example of connection and is not what was created as a purpose of mass production.

4. FUNCTION OPERATION TABLE

4.1 Relationship between SEL Pin and Input Pins

SEL pin	46-pin	47-pin	48-pin	1-pin
L	Unused	ch1 input pin IN_1	ch1 and ch2 control pin EN_{12}	ch2 input pin IN_2
H	ch1 input pin IN_{1A}	ch1 input pin IN_{1B}	ch2 input pin IN_{2A}	ch2 input pin IN_{2B}

Remark L: Low level, H: High level

4.2 ch1 and ch2 Input/output Truth Table

(1) SEL_{12} = L

Input		Output		Output Status
EN_{12}	IN	OUT_A	OUT_B	
L	x	Z	Z	Stop (output high impedance)
H	L	H	L	Forward revolution ($OUT_A \rightarrow OUT_B$)
H	H	L	H	Reverse revolution ($OUT_B \rightarrow OUT_A$)

Remark x: High level or low level, Z: Output high impedance

(2) SEL_{12} = H

Input		Output		Output Status
IN_A	IN_B	OUT_A	OUT_B	
L	L	L	L	Stop (short brake)
L	H	L	H	Reverse revolution ($OUT_B \rightarrow OUT_A$)
H	L	H	L	Forward revolution ($OUT_A \rightarrow OUT_B$)
H	H	H	H	Stop (short brake)

4.3 ch3 to ch5 Input/output Truth Table

Input		Output		Output Status
IN_A	IN_B	OUT_A	OUT_B	
L	L	L	L	Stop (short brake)
L	H	L	H	Reverse revolution ($OUT_B \rightarrow OUT_A$)
H	L	H	L	Forward revolution ($OUT_A \rightarrow OUT_B$)
(H)	(H)	(H)	(H)	Stop (short brake)

Caution At ch3 to ch5, inputting IN_A = H and IN_B = H prohibits.

4.4 ch6 Input/output Truth Table

Input		Output		Output Status
IN_A	IN_B	OUT_A	OUT_B	
L	L	L	L	Stop (short brake)
L	H	L	H	Reverse revolution ($OUT_B \rightarrow OUT_A$)
H	L	H	L	Forward revolution ($OUT_A \rightarrow OUT_B$)
H	H	H	H	Stop (short brake)

5. STANDBY FUNCTION

The μPD168002 realizes a standby function by combination of an input signal.

The specified output is set to high impedance (Hi-Z) status by setting STB to low level.

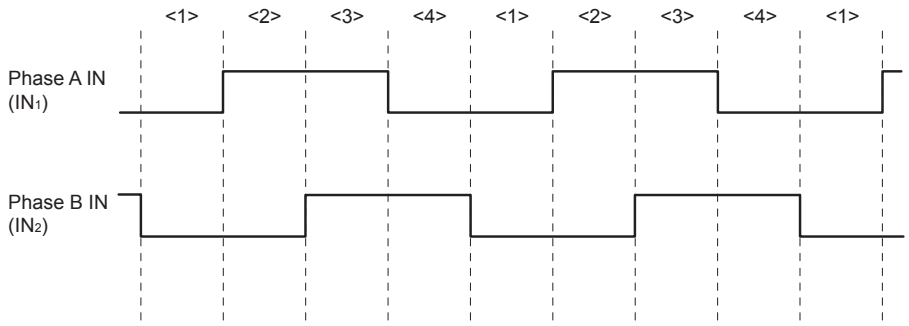
Each pin can be independently controlled, and can be set to standby status of the self current consumption of the IC reduced as much as possible by setting all pins to low level. In the standby status, the overheat protection circuit and the undervoltage lockout circuit do not operate.

Pin	Function	Output Status when Pin = L					
		ch1	ch2	ch3	ch4	ch5	ch6
STB_{12}	Sled block standby	Hi-Z	Hi-Z	ON	ON	ON	ON
STB_{34}	Focus and tracking block standby	ON	ON	Hi-Z	Hi-Z	ON	ON
STB_5	Spindle block standby	ON	ON	ON	ON	Hi-Z	ON
STB_6	Loading block standby	ON	ON	ON	ON	ON	Hi-Z

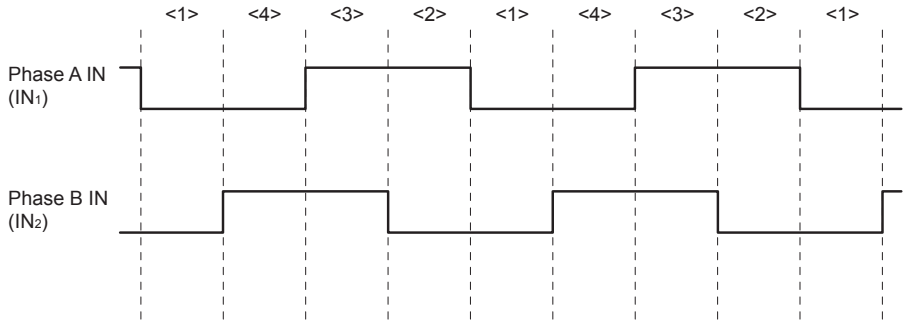
Remark ON: Status which can turn on output, Hi-Z: High impedance

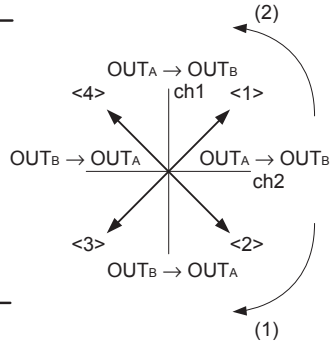
6. OPERATION WAVEFORM EXAMPLES

(1) Example of the clockwise revolution of the right figure when 2-phase diving



(2) Example of the counter-clockwise revolution of the right figure when 2-phase diving





Remark SEL_{12} = L, EN_{12} = H

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

(T_A = 25°C, glass epoxy board of 100 mm x 100 mm x 1 mm with copper foil area of 15%)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Control block	−0.5 to +6.0	V
	V_M	Motor block (ch3 and ch4)	−0.5 to +6.0	V
		Motor block (ch1, ch2, ch5 and ch6)	−0.5 to +12.0	V
Input voltage	V_{IN}		−0.5 to V_{DD} + 0.5	V
Output pin voltage 1	V_{OUT1}	Motor block (ch3 and ch4)	6.2	V
Output pin voltage 2	V_{OUT2}	Motor block (ch1, ch2, ch5 and ch6)	12.2	V
DC output current 1	$I_{D(DC)1}$	DC (ch3 to ch5)	±0.3	A/ch
DC output current 2	$I_{D(DC)2}$	DC (ch1, ch2 and ch6)	±0.15	A/ch
Instantaneous output current 1	$I_{D(pulse)1}$	PW < 10 ms, Duty Cycle ≤ 20% (ch3 to ch5)	±0.6	A/ch
Instantaneous output current 2	$I_{D(pulse)2}$	PW < 10 ms, Duty Cycle ≤ 20% (ch1, ch2 and ch6)	±0.3	A/ch
Power consumption	P_T		1.0	W
Peak junction temperature	$T_{ch(MAX)}$		150	°C
Storage temperature	T_{stg}		−55 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

(T_A = 25°C, glass epoxy board of 100 mm x 100 mm x 1 mm with copper foil area of 15%)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	Control block	2.7		5.5	V
	V_M	Motor block (ch3 and ch4)	2.7		5.5	V
		Motor block (ch1, ch2, ch5 and ch6)	6.0		11.0	V
Input voltage	V_{IN}		0		V_{DD}	V
DC output current 1	$I_{D(DC)1}$	DC (ch3 to ch5)	−0.2		+0.2	A/ch
DC output current 2	$I_{D(DC)2}$	DC (ch1, ch2 and ch6)	−0.1		+0.1	A/ch
Instantaneous output current 1	$I_{D(pulse)1}$	PW < 10 ms, Duty Cycle ≤ 20% (ch3 to ch5)	−0.4		+0.4	A/ch
Instantaneous output current 2	$I_{D(pulse)2}$	PW < 10 ms, Duty Cycle ≤ 20% (ch1, ch2 and ch6)	−0.2		+0.2	A/ch
Logic input frequency	f_{IN}				100	kHz
Operating temperature range	T_A		−40		85	°C

Electrical Characteristics

(Unless otherwise specified, T_A = 25°C, V_{DD} = 3 V, V_M = 5 V (ch3 and ch4), V_M = 8 V (ch1, ch2, ch5 and ch6))

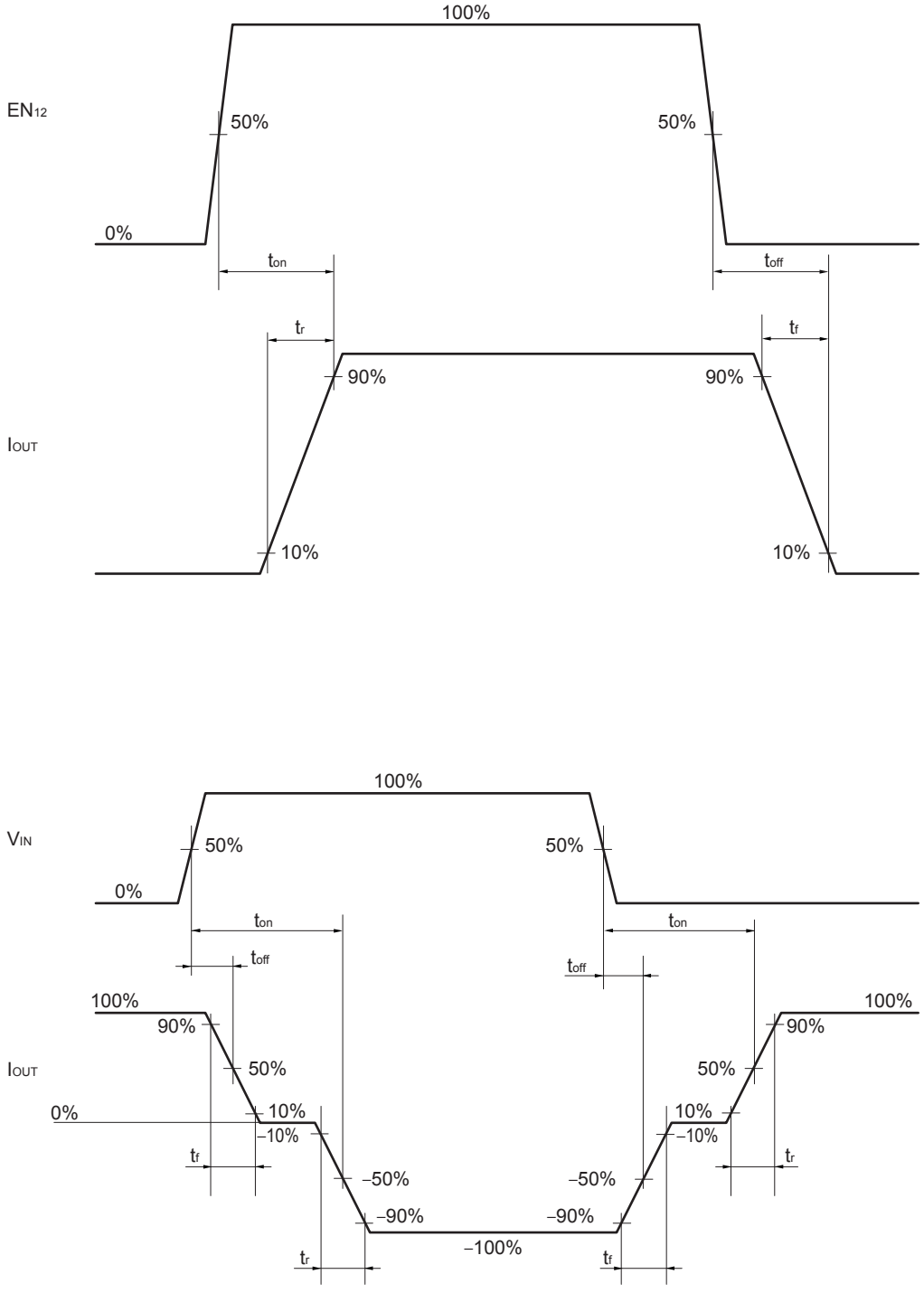
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_{DD} pin current in standby mode	$I_{DD(STB)}$	All control pin: Low level			1.0	μA
V_{DD} pin current in during operation	$I_{DD(ACT)}$				1.0	mA
V_M pin current in during operation	I_M	Output with no load, IN pin, EN pin: Low level			100	μA
High-level input current	I_{IH}	$V_{IN} = V_{DD}$			60	μA
Low-level input current	I_{IL}	V_{IN} = 0 V	−1.0			μA
Input pull-down resistance	R_{IND}		50		200	kΩ
High-level input voltage	V_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7 x V_{DD}			V
Low-level input voltage	V_{IL}	2.7 V ≤ V_{DD} ≤ 5.5 V			0.3 x V_{DD}	V
H-bridge on-state resistance 1 (ch1, ch2 and ch5)	R_{on1}	I_M = 0.1 A (ch1 and ch2), I_M = 0.2 A (ch5), sum of upper and lower stages		2.0	3.0	Ω
H-bridge on-state resistance 2 (ch3 and ch4)	R_{on2}	I_M = 0.2 A, sum of upper and lower stages		1.2	2.0	Ω
H-bridge on-state resistance 3 (ch6)	R_{on3}	I_M = 0.1 A, sum of upper and lower stages		3.5	5.0	Ω
Output leakage current	$I_{M(off)}$	Per V_M pin, All control pin: Low level (V_M = MAX. value in the recommended range)			10	μA
Low-voltage detection voltage	V_{DDS}			1.7	2.5	V
Output turn-on time [Note]	t_{on2}	I_M = 0.1 A (ch1, ch2 and ch6), Refer to **Figure 7–1. H-bridge Switching Waveform (when SEL_{12} = L)** and **Figure 7–2. H-bridge Switching Waveform (when SEL_{12} = H)** .	0.2	0.6	2.0	μs
Output turn-off time [Note]	t_{off2}		0.05	0.3	1.0	μs
Output turn-on time [Note]	t_{on1}	I_M = 0.2 A (ch3 to ch5), Refer to **Figure 7–2. H-bridge Switching Waveform (when SEL_{12} = H) (only when V_{INB} = L)** .	0.05	0.15	1.0	μs
Output turn-off time [Note]	t_{off1}		0.05	0.2	1.0	μs

Note For the turn-on time and the turn-off time, to fix one of two input pins to low level is conditions.

Remark The overheat protection circuit operates under T_{ch} > 150°C. All outputs goes high impedance in the protection status. Note that the overheat protection circuit and the undervoltage lockout circuit do not operate in the standby status.

Switching Characteristics Waveform

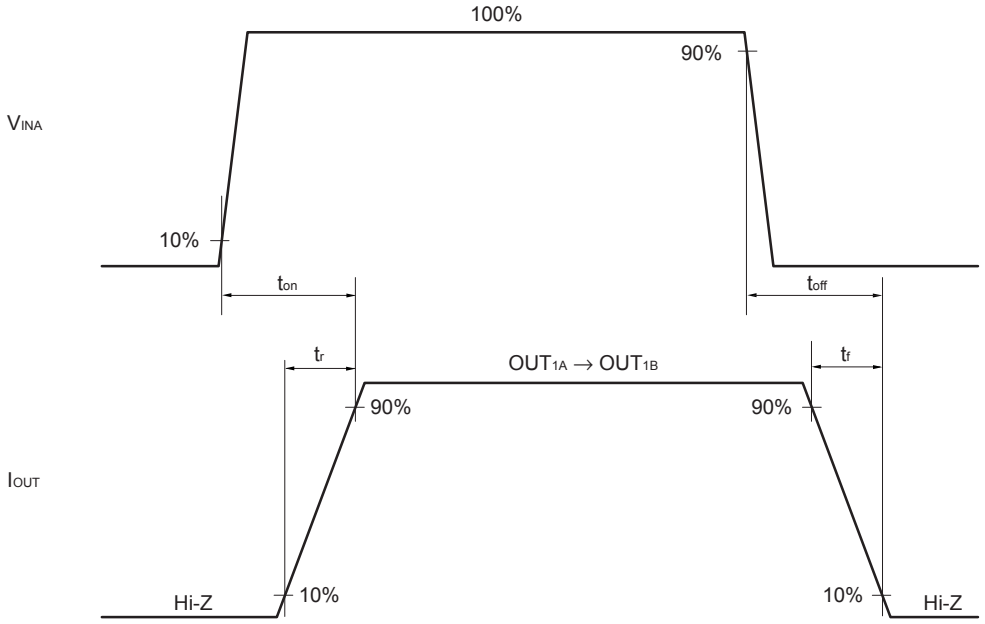
Figure7–1. H-bridge Switching Waveform (when SEL_{12} = L)



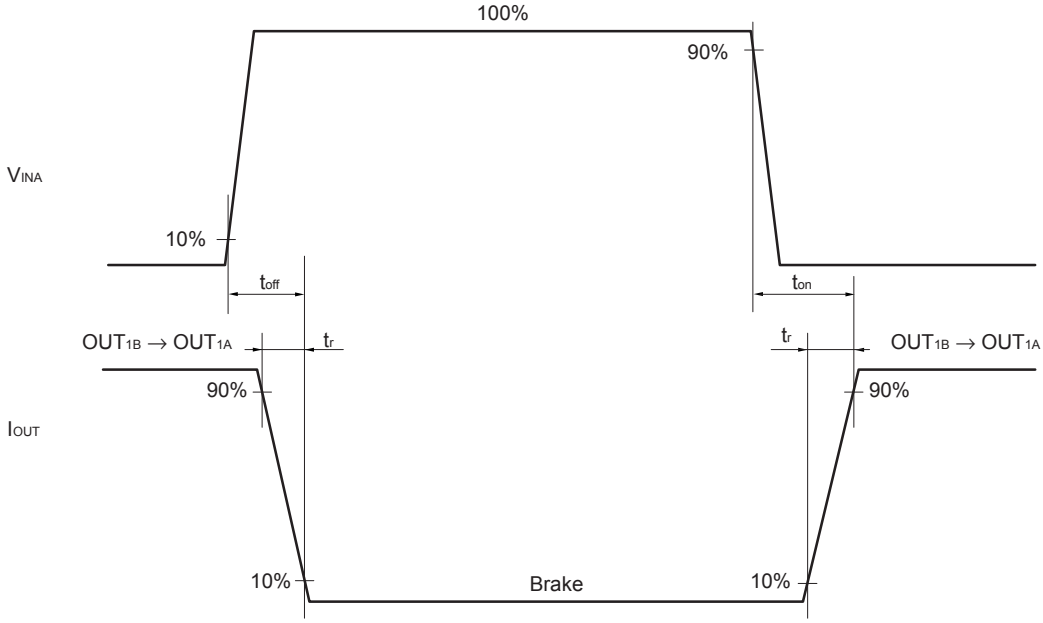
Remark The high impedance period of about 50 ns is prepared for the through-current prevention at the time of mode switching. The t_r (rise time) is designed as 50 ns, and the t_f (fall time) is designed as about 50 ns.

Figure7–2. H-bridge Switching Waveform (when SEL_{12} = H)

When V_{INB} = L



When V_{INB} = H **Note**

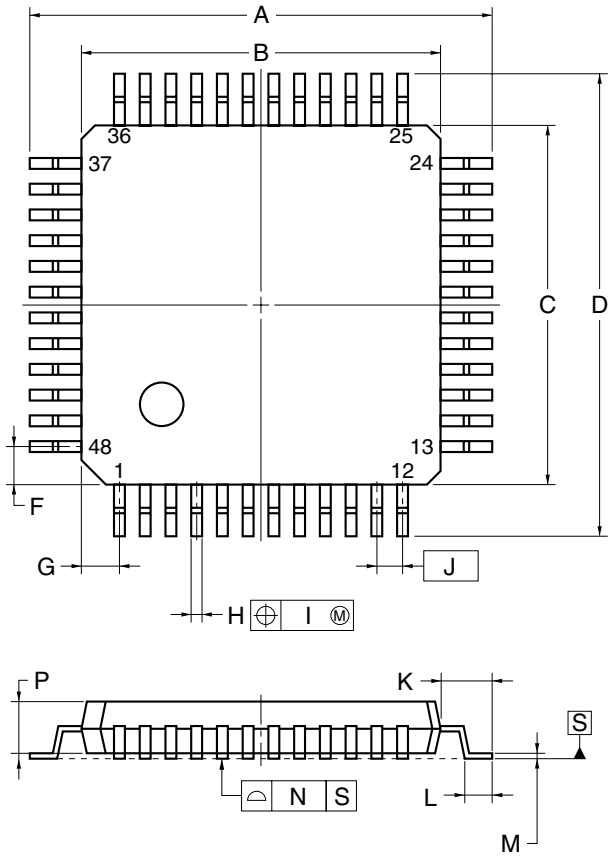


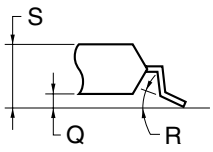
Note The conditions of V_{INB} = H is valid only at ch1, ch2 and ch6. The through current may be flowed, if the switching operation is performed under the conditions of V_{INB} = H at ch3 to ch5.

Remark The high impedance period of about 50 ns is prepared for the through-current prevention at the time of mode switching. The t_r (rise time) is designed as 50 ns, and the t_f (fall time) is designed as about 50 ns.

8. PACKAGE DRAWING

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)





NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.0±0.2
B	7.0±0.2
C	7.0±0.2
D	9.0±0.2
F	0.75
G	0.75
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

S48GA-50-9EU-2

9. RECOMMENDED SOLDERING CONDITIONS

The μPD168002 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPD168002GA-9EU: 48-pin plastic TQFP (fine pitch) (7 x 7)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 60 seconds MAX. (at 210°C or higher) , Count: Three times or less, Exposure limit: None, Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.	IR35-00-3

Caution Do not use different soldering methods together (except for partial heating) .

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades on NEC Semiconductor Devices (C11531E)

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