FAIRCHILD SEMICONDUCTOR®

April 2005

# FDFM2P110
# Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

## Features

- –3.5 A, –20 V $R_{DS(ON)}$ = 140 mΩ @ $V_{GS}$ = –4.5 V
  $R_{DS(ON)}$ = 200 mΩ @ $V_{GS}$ = –2.5 V
- Low Profile – 0.8mm maximum – in the new package MicroFET 3x3 mm

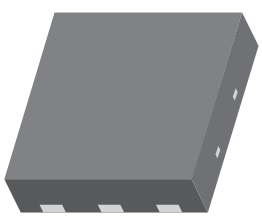
## Applications

- DC-DC Converter

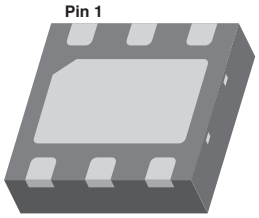
## General Description

FDFM2P110 combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in a MicroFET package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance.



Top

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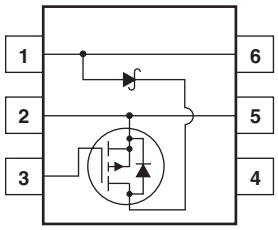



MLP 3x3

## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±12 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | –3.5 | A |
| | – Pulsed | | –10 | |
| $V_{RRM}$ | Schottky Repetitive Peak Reverse Voltage | | 20 | V |
| $I_O$ | Schottky Average Forward Current | (Note 1a) | 2 | A |
| $P_D$ | Power Dissipation (Steady State) | (Note 1a) | 2.4 | W |
| | | (Note 1b) | 1.2 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |
| **Thermal Characteristics** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 60 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 145 | |

## Package Marking and Ordering Information

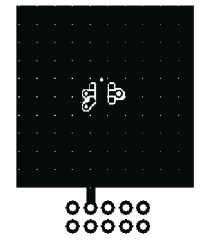
| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| 2P110 | FDFM2P110 | 7" | 12mm | 3000 units |

## Electrical Characteristics $T_A$ = 25°C unless otherwise noted

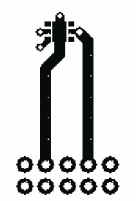
| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 μA | | –20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 μA, Referenced to 25°C | | | –11 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | | | | –1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 V | | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | | –0.6 | –1.0 | –1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 μA, Referenced to 25°C | | | 3 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –4.5 V, $I_D$ = –3.5 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –3.0 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –3.5A, $T_J$ = 125°C | | | 101<br>145<br>136 | 140<br>200<br>202 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –2.5 V, $V_{DS}$ = –5 V | | –10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –3.5 A | | | 6 | | S |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | | 280 | | pF |
| $C_{oss}$ | Output Capacitance | | | | 65 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | | 35 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 0 V, f = 1.0 MHz | | | 7 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –10 V, $I_D$ = –1 A, $V_{GS}$ = –4.5 V, $R_{GEN}$ = 6 Ω | | | 8 | 16 | ns |
| $t_r$ | Turn–On Rise Time | | | | 12 | 22 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | | 11 | 20 | ns |
| $t_f$ | Turn–Off Fall Time | | | | 3.2 | 6.4 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –10 V, $I_D$ = –3.5 A, $V_{GS}$ = –4.5 V | | | 3 | 4 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | | 0.7 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | | 1 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | | –2 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –2 A (Note 2) | | | –0.9 | –1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = –3.5 A, $dI_F/dt$ = 100 A/μs | | | 13 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | | 3 | | nC |
| **Schottky Diode Characteristic** | | | | | | | |
| $V_R$ | Reverse Voltage | $I_R$ = 1 mA | | 20 | | | V |
| $I_R$ | Reverse Leakage | $V_R$ = 5 V | $T_J$ = 25°C | | | 100 | μA |
| | | | $T_J$ = 100°C | | | 10 | mA |
| $V_F$ | Forward Voltage | $I_F$ = 1 A | $T_J$ = 25°C | | 0.32 | 0.39 | V |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 70°C/W when mounted on a 1 $in^2$ pad of 2 oz copper



b) 145°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Characteristics

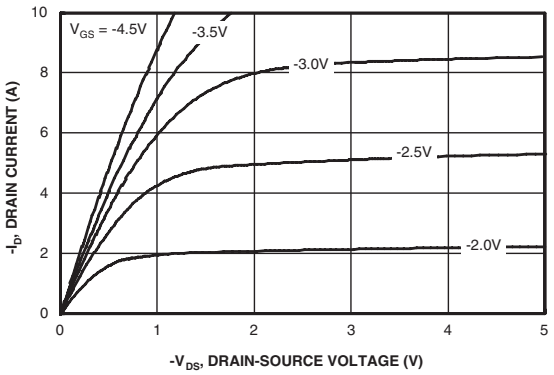



**Figure 1. On-Region Characteristics.**

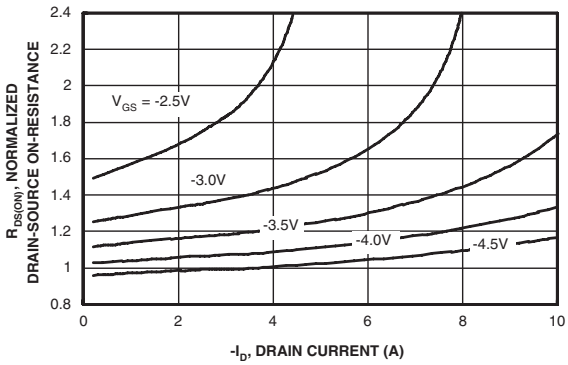



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

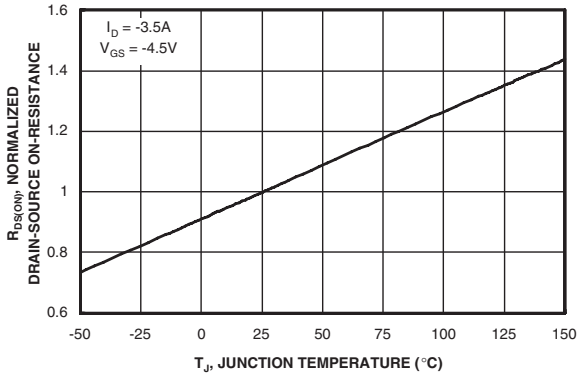



**Figure 3. On-Resistance Variation with Temperature.**

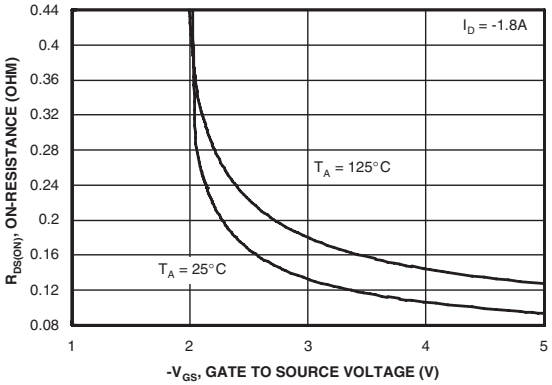



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

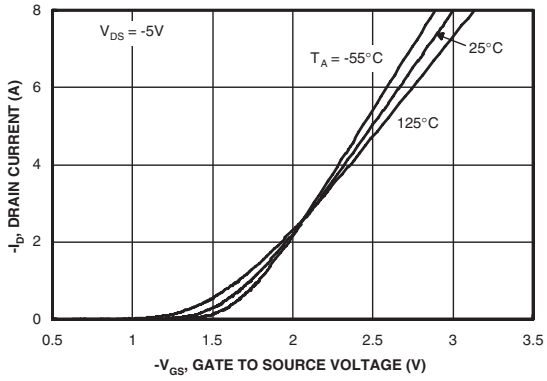



**Figure 5. Transfer Characteristics.**

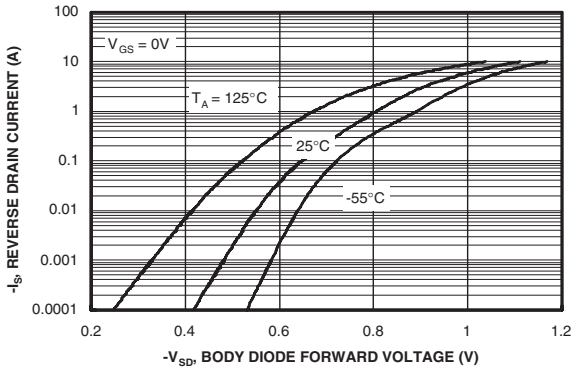



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

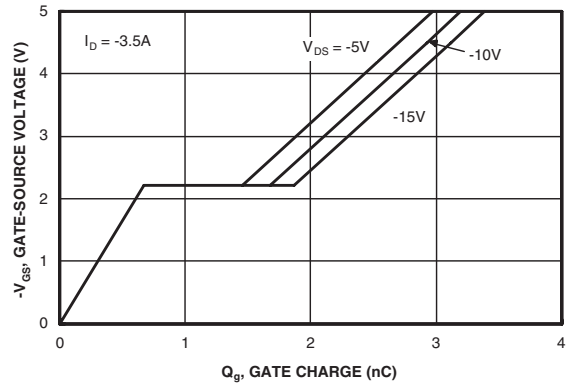



**Figure 7. Gate Charge Characteristics.**

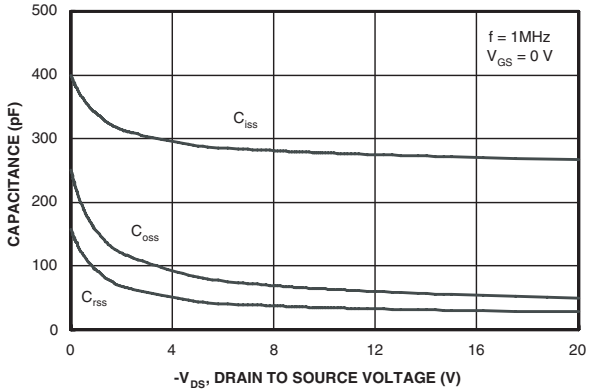



**Figure 8. Capacitance Characteristics.**

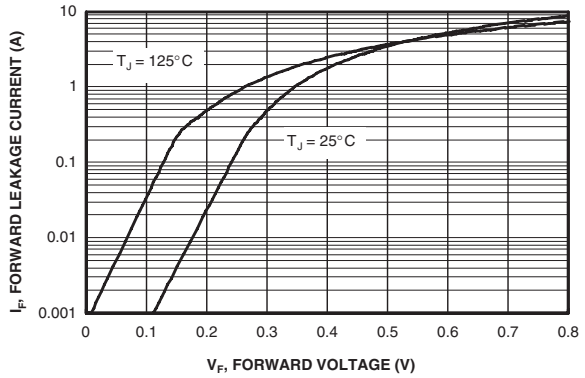



**Figure 9. Schottky Diode Forward Voltage.**

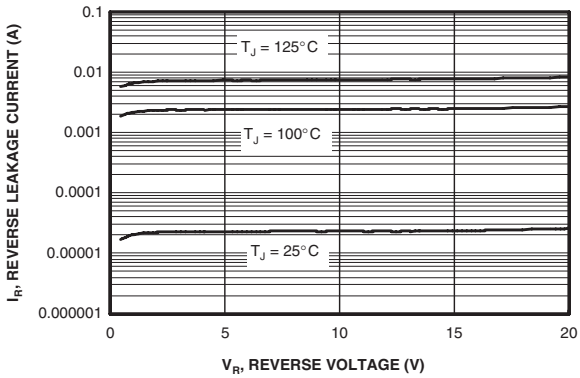



**Figure 10. Schottky Diode Reverse Current.**

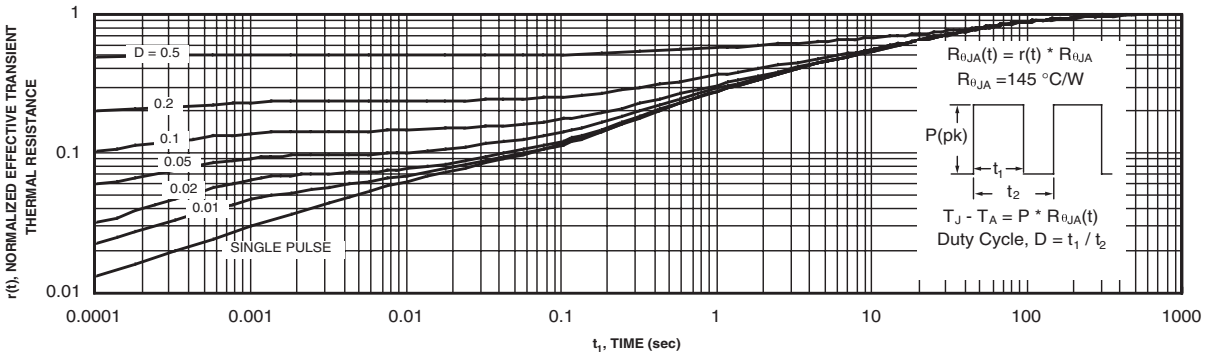
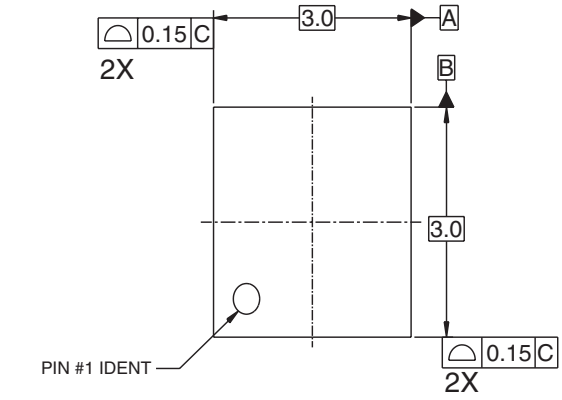


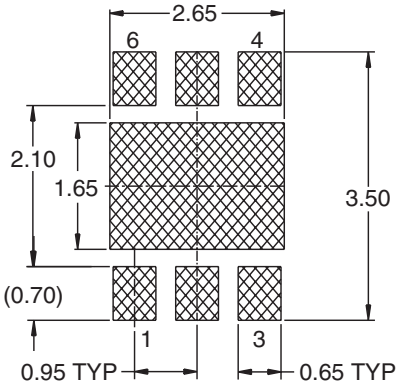

**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1b.**
**Transient thermal response will change depending on the circuit board design.**

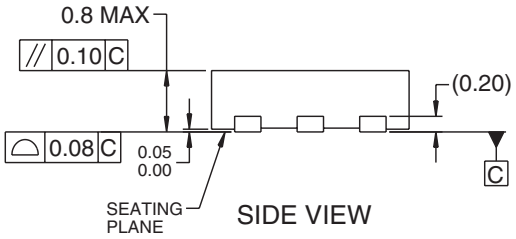
## Package Dimensions



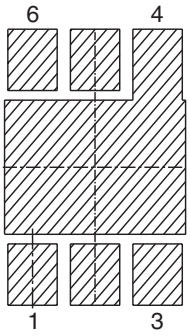

TOP VIEW



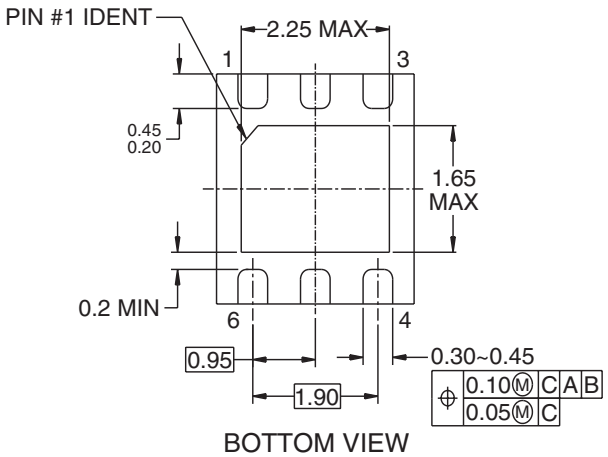

RECOMMENDED LAND PATTERN




SIDE VIEW




RECOMMENDED COPPER TRACE




BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEEA, DATED 11/2001

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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| FACT™ | ImpliedDisconnect™ | OCX™ | RapidConfigure™ | TruTranslation™ |
| FACT Quiet Series™ | | OCXPro™ | RapidConnect™ | UHC™ |
| Across the board. Around the world.™ | | OPTOLOGIC® | µSerDes™ | UltraFET® |
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