



# STL100NH3LL

N-CHANNEL 30V - 0.0032Ω - 25A PowerFLAT™ (6x5)

STripFET™ III MOSFET

PRODUCT PREVIEW

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL100NH3LL	30 V	< 0.0035 Ω	25 A (1)

- TYPICAL R<sub>DS(on)</sub> = 0.0032Ω @ 10V
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

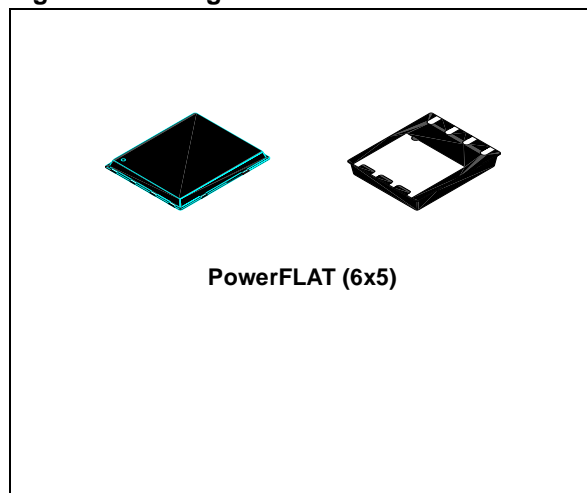
## DESCRIPTION

The STL100NH3LL utilizes the latest advanced design rules of ST's proprietary STripFET™ Technology. This process complete to unique metallization technique realised the most advanced low voltage MOSFET in PowerFLAT(6x5). The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

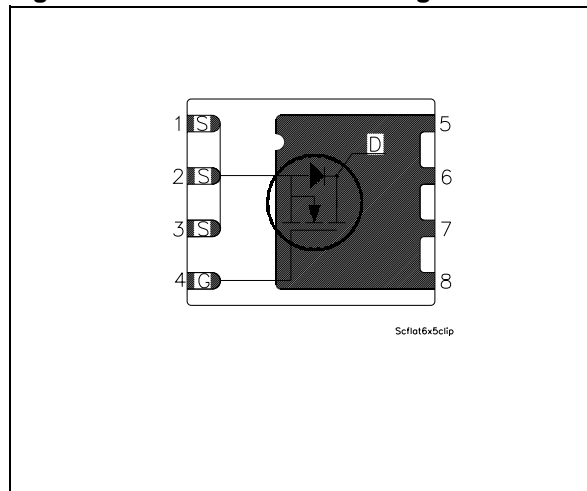
## APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- SYNCHRONOUS RECTIFICATION

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL100NH3LL	L100NH3LL	PowerFLAT™ ( 6x5 )	TAPE & REEL

Rev. 4

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate- source Voltage	$\pm 16$	V
$I_D (2)$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	100	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	15.6	A
$I_{DM} (3)$	Drain Current (pulsed)	100	A
$I_D (1)$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	25	A
$P_{TOT} (2)$	Total Dissipation at $T_C = 25^\circ\text{C}$	80	W
$P_{TOT}(1)$	Total Dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating Factor	0.03	W/ $^\circ\text{C}$
$T_{stg}$ $T_j$	Storage Temperature Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

**Table 4: Thermal Data**

$R_{thj-c}$	Thermal Resistance Junction-case ( Drain) (Steady State)	1.56	$^\circ\text{C}/\text{W}$
$R_{thj-pcb} (4)$	Thermal Operating Junction-pcb	31.3	$^\circ\text{C}/\text{W}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AV}$	Not-Repetitive Avalanche Current (pulse width limited by $T_j$ max)	12.5	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 24\text{ V}$ )	1.3	J

**ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)**
**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 12.5\ \text{A}$ $V_{GS} = 4.5\text{V}$ , $I_D = 12.5\ \text{A}$		0.0032 0.004	0.0035 0.005	$\Omega$ $\Omega$

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (5)	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 12,5\text{ A}$		30		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		4450 655 50		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ , $I_D = 12.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 15)		18 50 75 8		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 15\text{ V}$ , $I_D = 25\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see Figure 17)		30 12.5 10	40	nC nC nC
$R_G$	Gate Input Resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain	1	2	3	$\Omega$

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (3)	Source-drain Current Source-drain Current (pulsed)				25 100	A A
$V_{SD}$ (4)	Forward On Voltage	$I_{SD} = 25\text{ A}$ , $V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, Figure 16)		32 34 2.1		ns nC A

Note:

- (1) The value is according  $R_{thj-pcb}$
- (2) The value is according  $R_{thj-c}$
- (3) Pulse width limited by safe operating area.
- (4) When mounted on FR-4 board of  $1\text{ in}^2$ , 2oz Cu,  $t < 10\text{ sec}$
- (5) Pulsed: Pulse duration =  $300\mu\text{s}$ , duty cycle 1.5%

Figure 3: Safe Operating Area

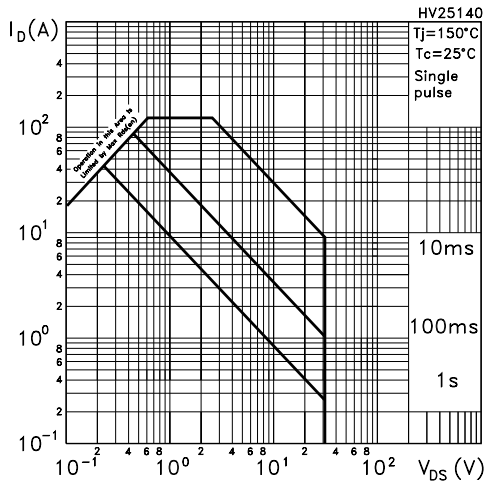


Figure 4: Output Characteristics

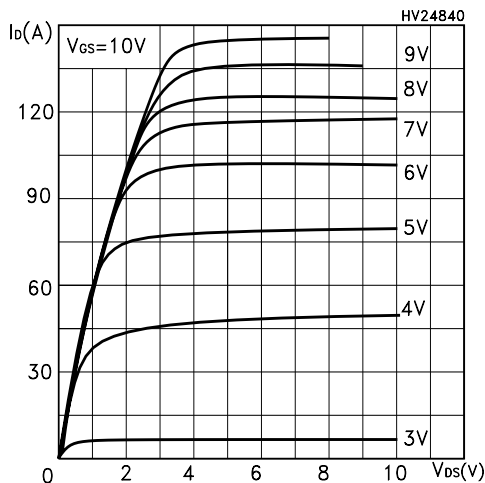


Figure 5: Transconductance

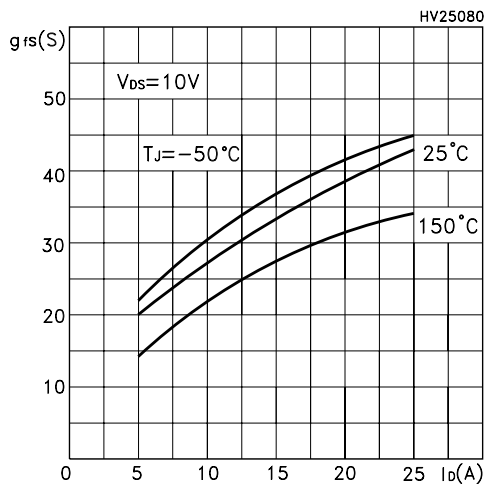


Figure 6: Thermal Impedance

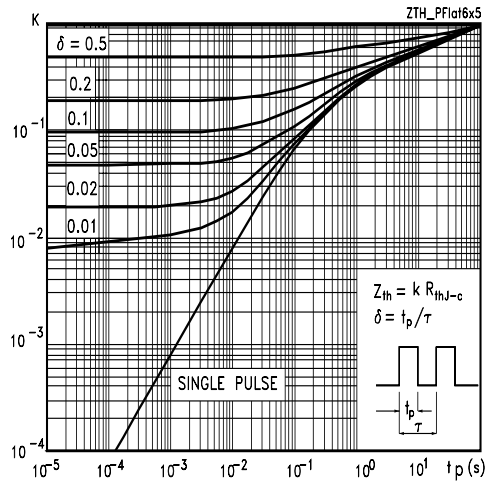


Figure 7: Transfer Characteristics

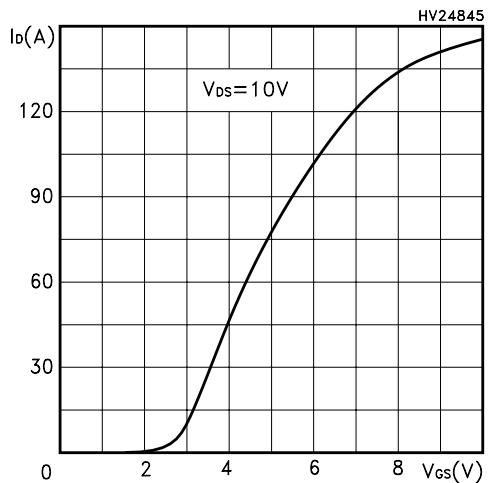


Figure 8: Static Drain-source On Resistance

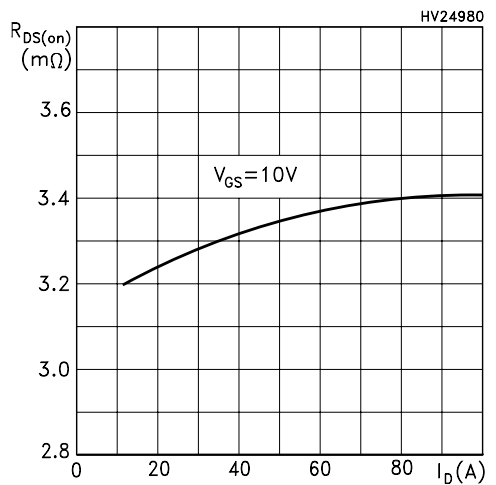


Figure 9: Gate Charge vs Gate-source Voltage

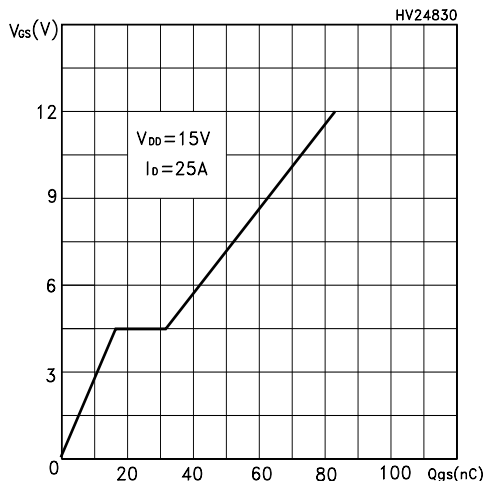


Figure 10: Normalized Gate Threshold Voltage vs Temperature

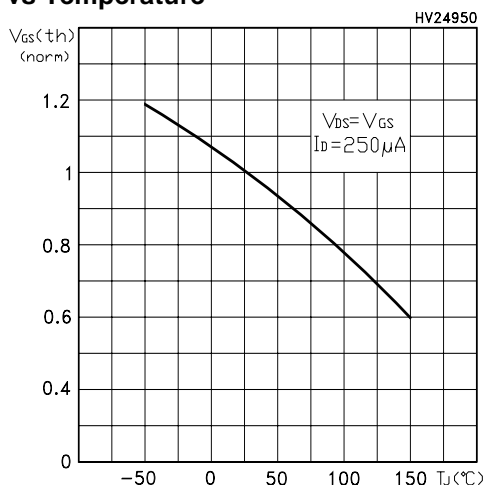


Figure 11: Normalized On Resistance vs Temperature

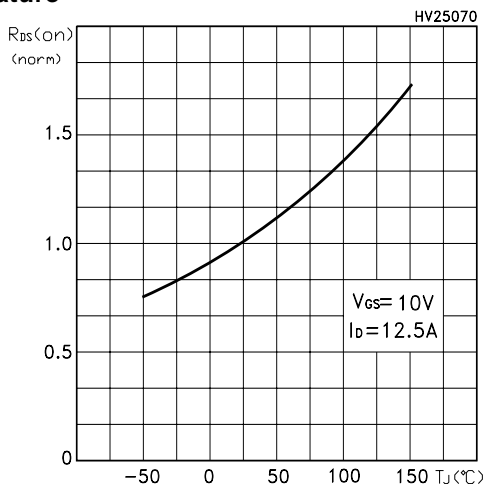


Figure 12: Capacitance Variations

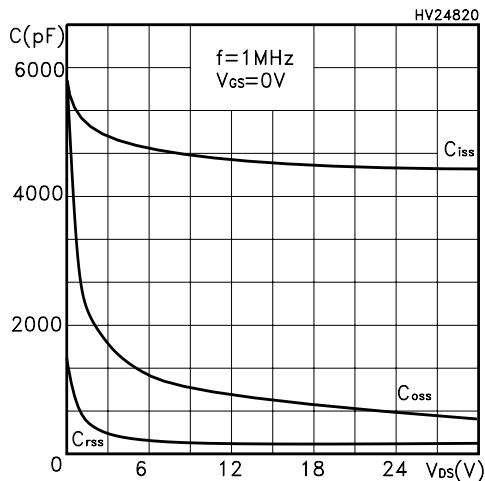


Figure 13: Normalized BVDSS vs Temperature

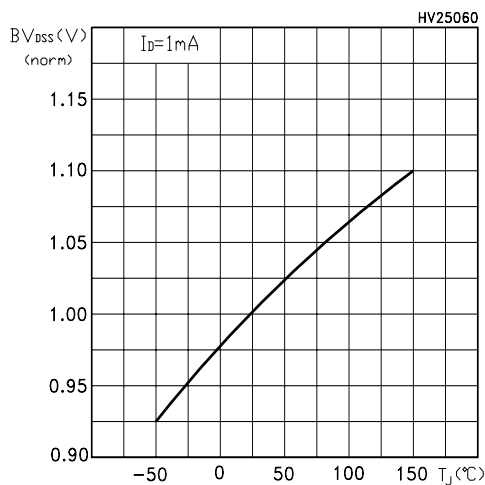


Figure 14: Source-Drain Diode Forward Characteristics

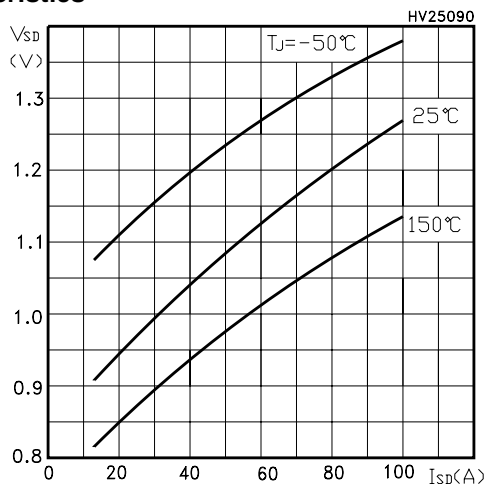


Figure 15: Switching Times Test Circuit For Resistive Load

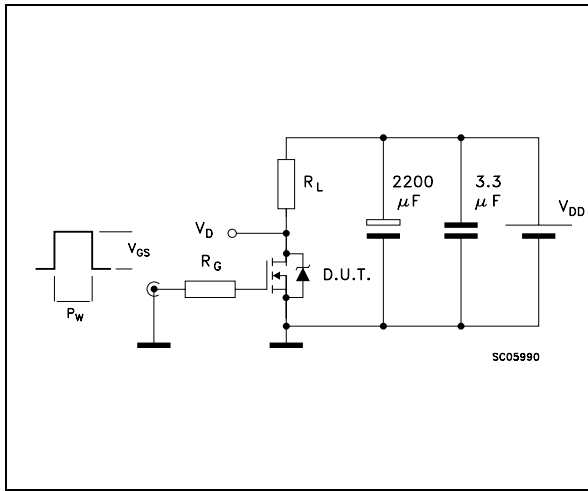


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

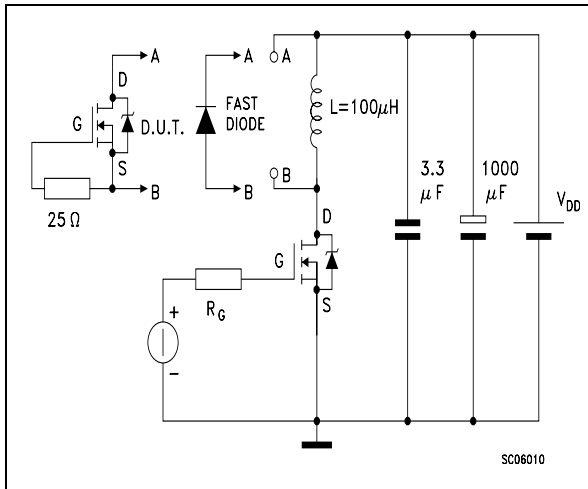
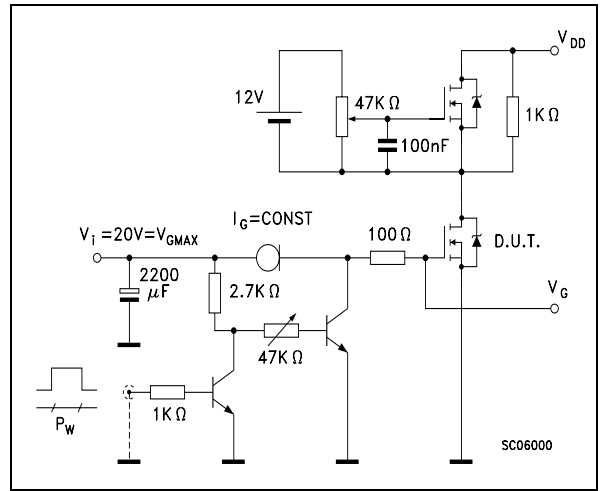


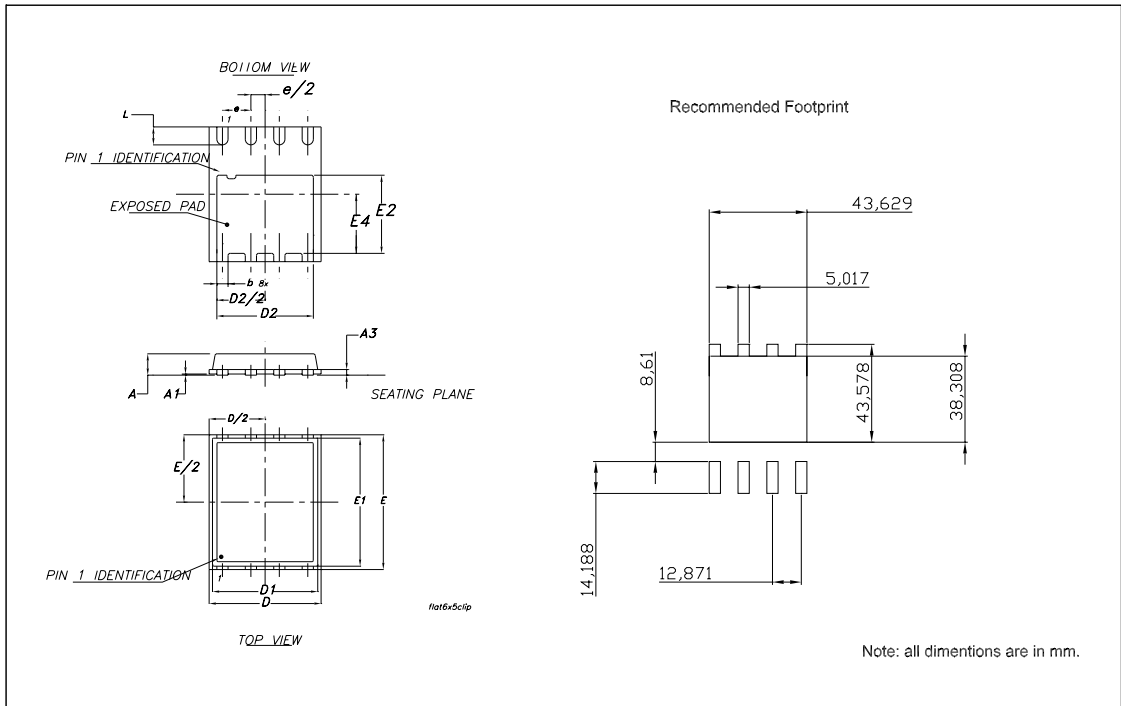
Figure 17: Gate Charge Test Circuit



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**PowerFLAT™ (6x5) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035





**Table 9: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
18-Apr-2005	1	First release
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New $R_G$ value on table 6
10-Oct-2005	4	Inserted Ecopack indication

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