

Evaluation Board for CS5340

Features

- Demonstrates recommended layout and grounding arrangements
- CS8406 generates S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system

Description

The CDB5340 evaluation board is an excellent means for quickly evaluating the CS5340 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, and a power supply.

Also included is a CS8406 digital audio interface transmitter which generates S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB5340

Evaluation Board

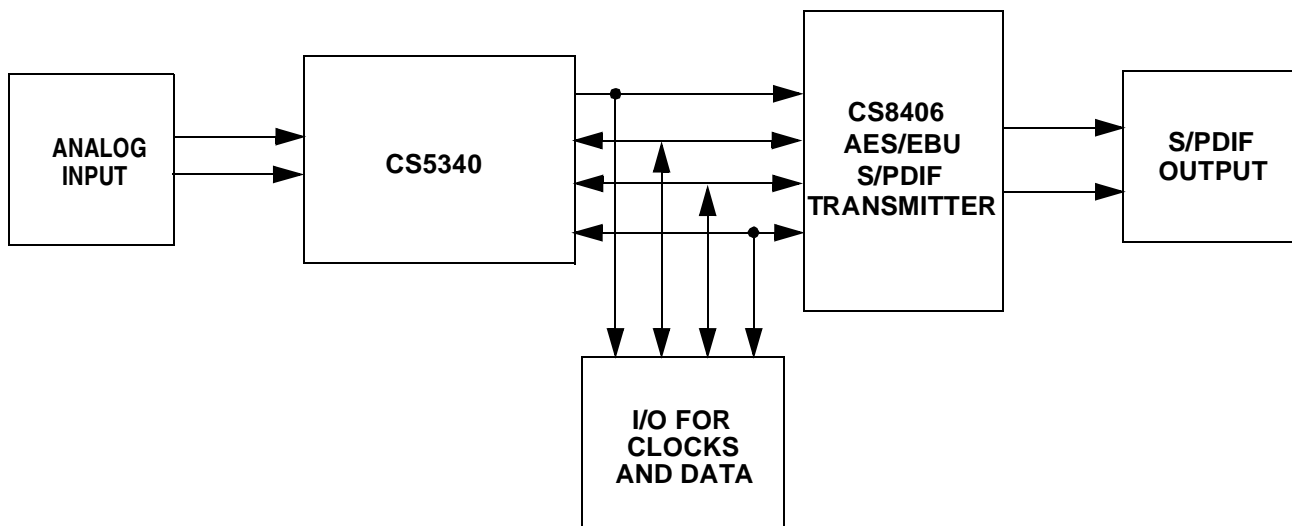


TABLE OF CONTENTS

1. CDB5340 SYSTEM OVERVIEW	3
2. CS8406 DIGITAL AUDIO TRANSMITTER	3
3. INPUT/OUTPUT FOR CLOCKS AND DATA	3
4. POWER SUPPLY CIRCUITRY	3
5. GROUNDING AND POWER SUPPLY DECOUPLING	3
6. ANALOG INPUT FILTER	3

LIST OF FIGURES

Figure 1. System Block Diagram and Signal Flow	5
Figure 2. Analog Audio Input.....	6
Figure 3. CS5340	7
Figure 4. Level Shifters	8
Figure 5. CS8406 Digital Audio Interface	9
Figure 6. Power Circuit.....	10
Figure 7. Top Layer Silkscreen	11
Figure 8. Top Layer	12
Figure 9. Bottom Layer.....	13

LIST OF TABLES

Table 1. System Connections	4
Table 2. CDB5340 Jumper and Switch Settings	4

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this material and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan. An export license and/or quota needs to be obtained from the competent authorities of the Chinese Government if any of the products or technologies described in this material is subject to the PRC Foreign Trade Law and is to be exported or taken out of the PRC.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS (INCLUDING MEDICAL DEVICES, AIRCRAFT SYSTEMS OR COMPONENTS AND PERSONAL OR AUTOMOTIVE SAFETY OR SECURITY DEVICES). INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

1. CDB5340 SYSTEM OVERVIEW

The CDB5340 evaluation board is an excellent means of quickly evaluating the CS5340. The CS8406 digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB5340 schematic has been partitioned into 5 schematics shown in Figure 2 through Figure 6. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS8406 DIGITAL AUDIO TRANSMITTER

The system generates and encodes standard S/PDIF data using a CS8406 Digital Audio Transmitter (see Figure 5). The outputs of the CS8406 are RS422 compatible differential line drivers. The CS8406 supports both Left Justified and I²S data formats, as determined by the DIP switch, S2. A description of the CS8406 is included in the CS8406 datasheet.

3. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J11. The schematic for the clock/data input/output is shown in Figure 4.

The CDB5340 allows some flexibility as to the generation of the clocks. When the CS5340 and CS8406 are in slave mode, the SCLK and LRCK must be provided via the header, J11. MCLK can be generated from the on-board oscillator, Y1 or provided via the header, J11 as determined by the DIP switch, S2. The on-board oscillator is socketed to allow other frequency oscillators to be used. Please note that the on-board oscillator must be removed if an external MCLK is provided through header J11.

4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (VA/VD, VL, GND, +5V), see Figure 6. The VA/VD input supplies the VA and VD pins of the CS5340. VL supplies power to the VL pin of the CS5340 and to the level shifter circuits. The +5V input supplies power to the digital circuitry and the input amplifiers.

5. GROUNDING AND POWER SUPPLY DECOUPLING

The CS5340 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 details the power distribution used on this board. The decoupling capacitors are located as close to the CS5340 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. ANALOG INPUT FILTER

The CDB5340 implements a single-ended analog input buffer, as shown in Figure 2. Note that there is no attenuation or gain associated with the input buffer.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
VA/VD	Input	+3.3V to +5V power for the CS5340
VL	Input	+2.5V to +5V power for the CS5340
GND	Input	Ground connection from power supply
+5V	Input	+ 5 Volt power
AINL	Input	Analog input left channel
AINR	Input	Analog input right channel
Optical Output	Output	Digital audio output
Coax Output	Output	Digital audio output

Table 1. System Connections

JUMPER/SWITCH	PURPOSE	POSITION		FUNCTION SELECTED
J5	VA/VD Power Source	ADJ	Open	Power from the Binding Post (J1)
		*+3.3V	*Closed	Power from the +3.3V Regulator
		+5V		Power from the +5V Supply
J6	VL Power Source	ADJ	Open	Power from the Binding Post (J2)
		*+3.3V	*Closed	Power from the +3.3V Regulator
		+5V		Power from the +5V Supply
J11	Input/Output for clocks/data	-		-
S1	Reset for the CDB5340	-		-
S2	CDB5340 Configuration	M1/M0	Open	Hi
			*Closed	Low
		SCLK/LRCK	Open	Header J11 is an input for clocks.
			*Closed	Header J11 is an output for clocks.
		MCLK	Open	Header J11 is an input for MCLK.
	*Closed	Header J11 is an output for MCLK.		
8406	Open	CS8406 in Master mode		
	*Closed	CS8406 in Slave mode		
DIF	Open	Digital interface format set to I ² S		
	*Closed	Digital interface format set to Left Justified		

Table 2. CDB5340 Jumper and Switch Settings

* denotes default factory settings

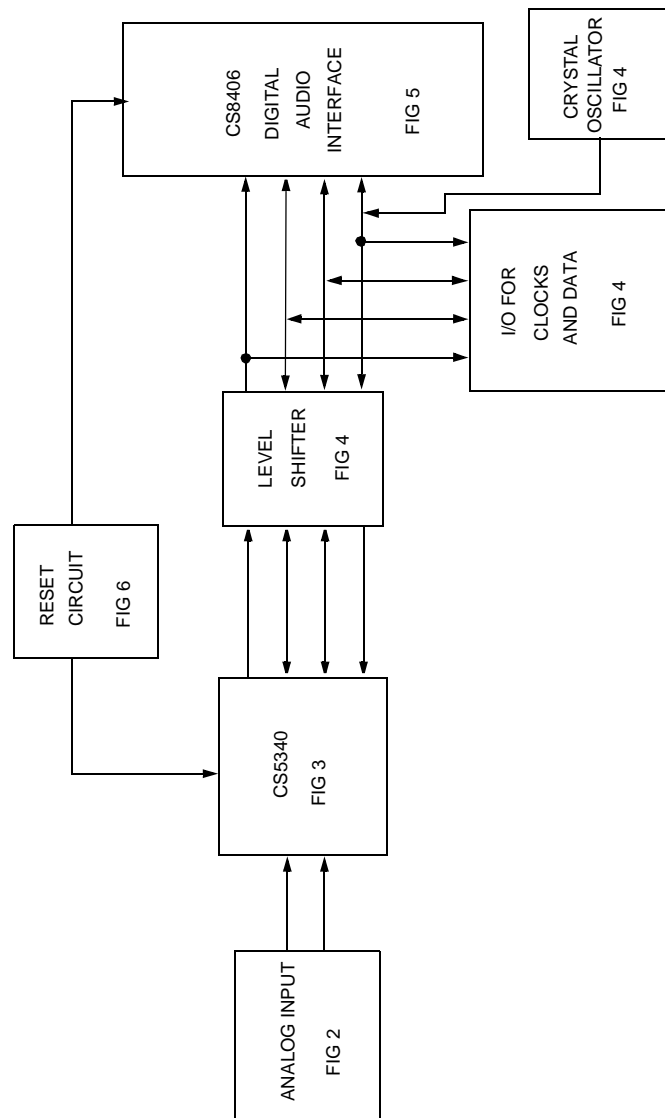
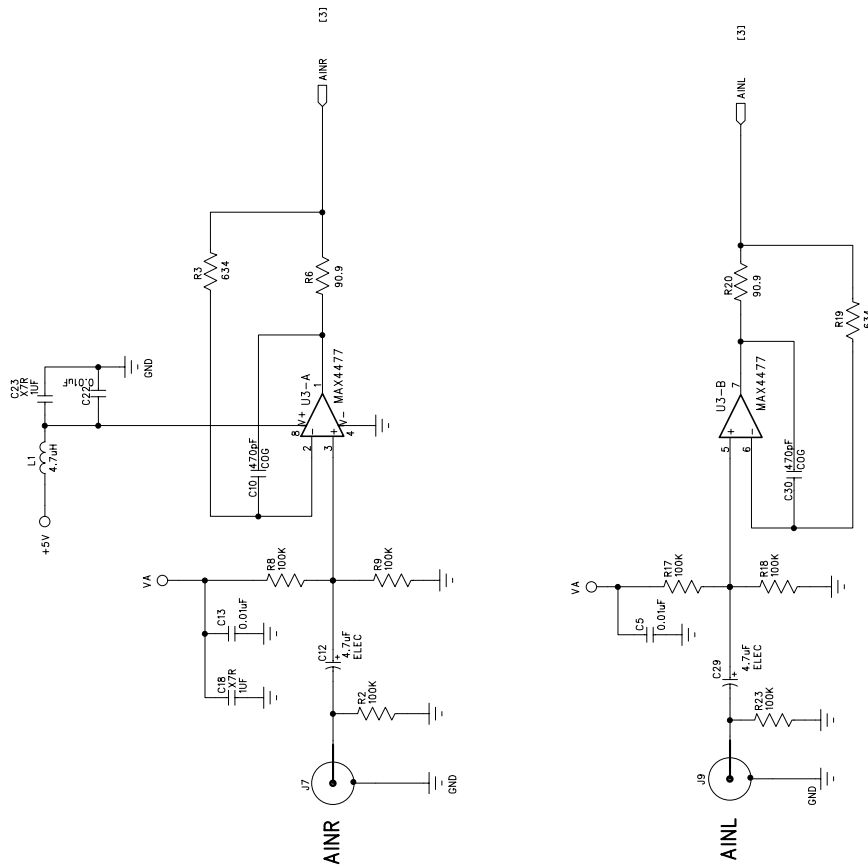
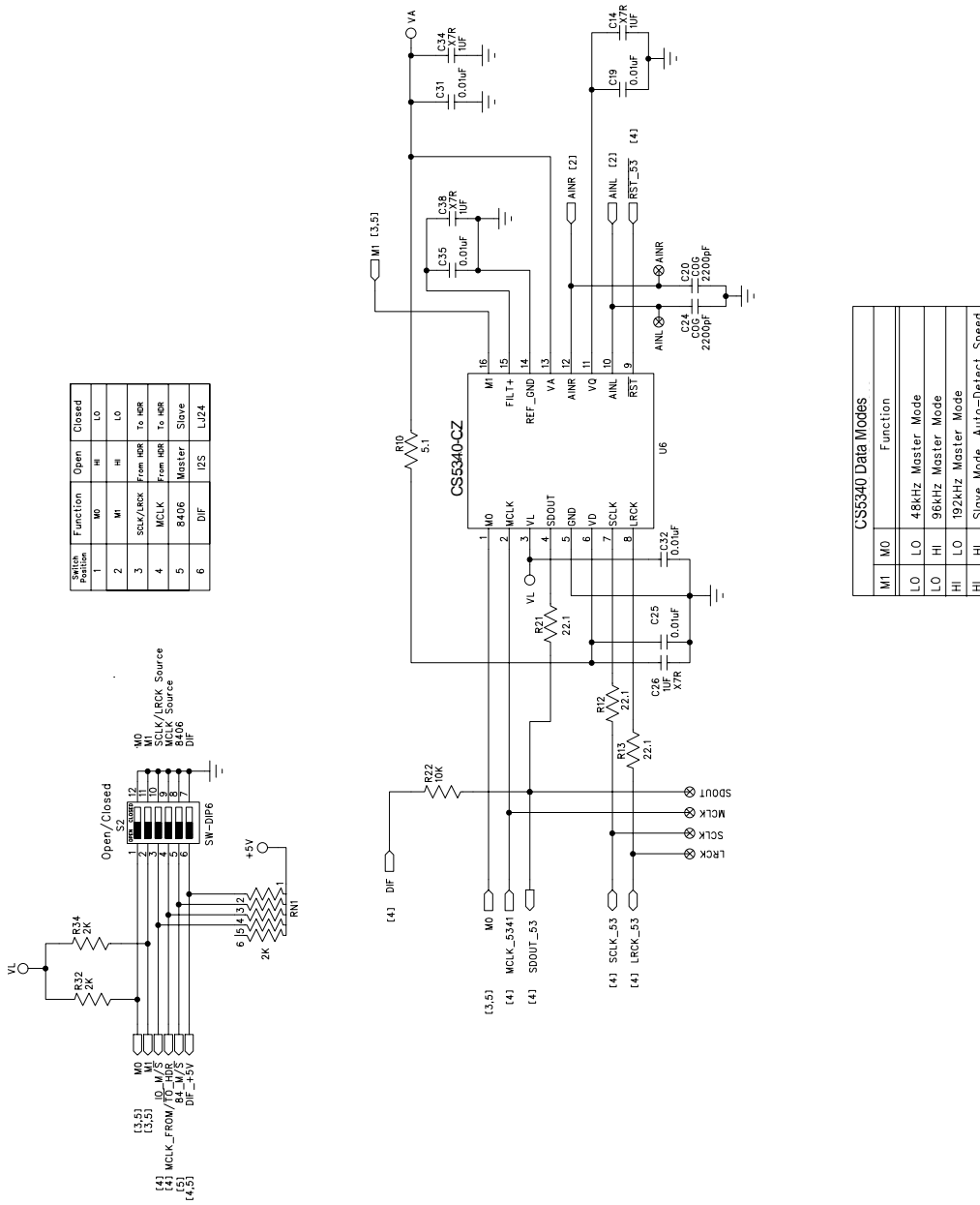


Figure 1. System Block Diagram and Signal Flow


Figure 2. Analog Audio Input


Figure 3. CS5340

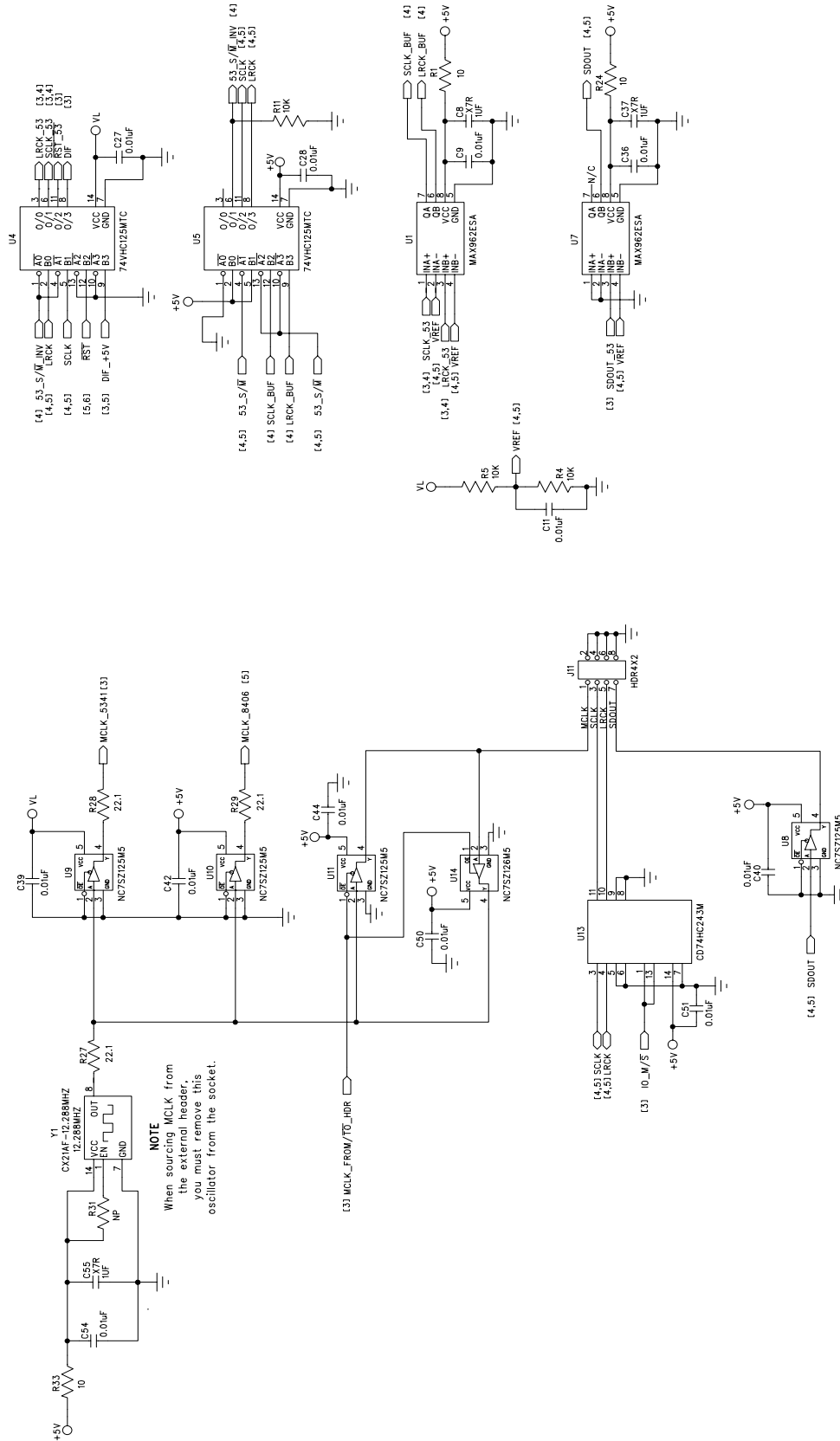
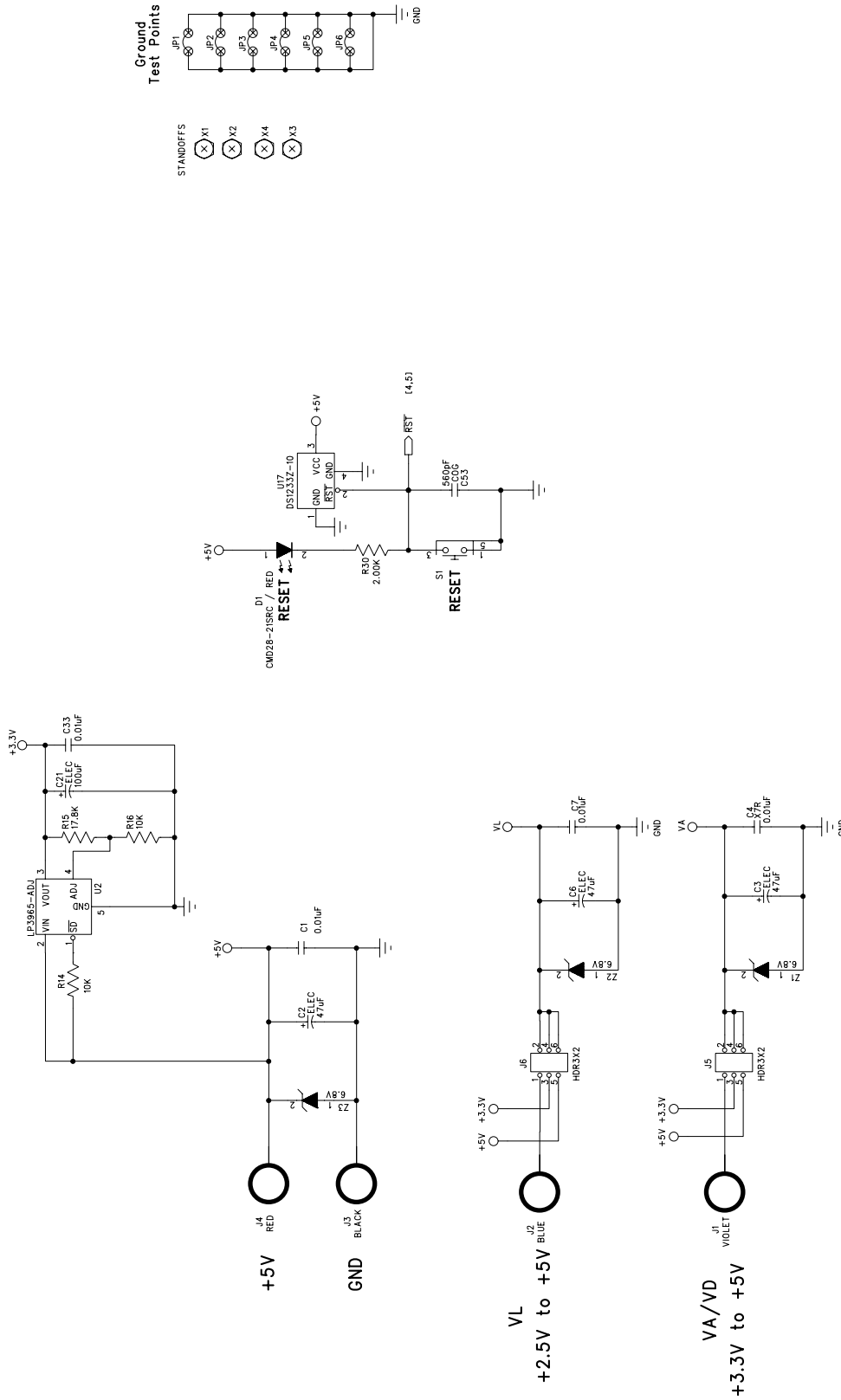
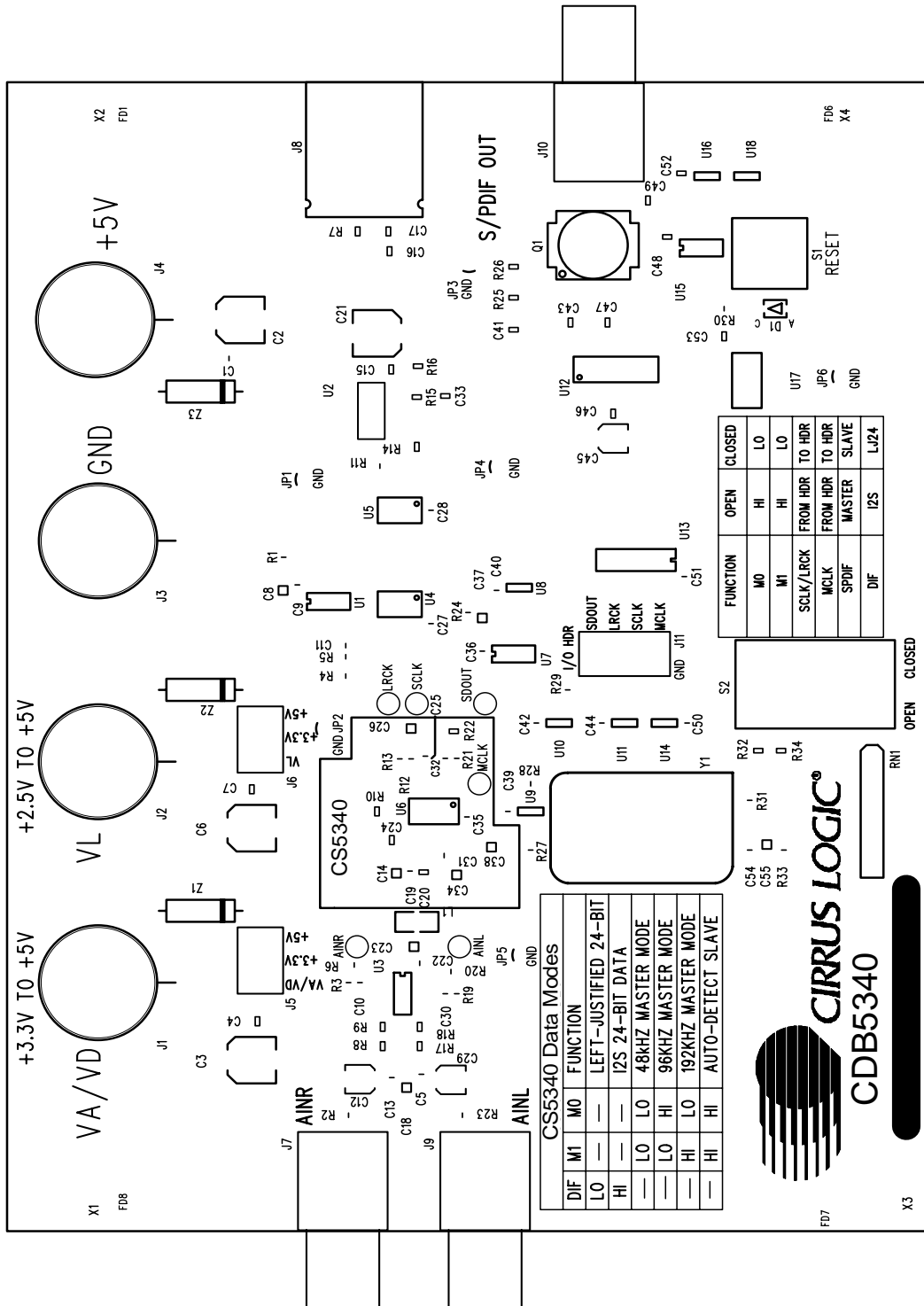


Figure 4. Level Shifters


Figure 6. Power Circuit



SILKSCREEN TOP
Figure 7. Top Layer Silkscreen

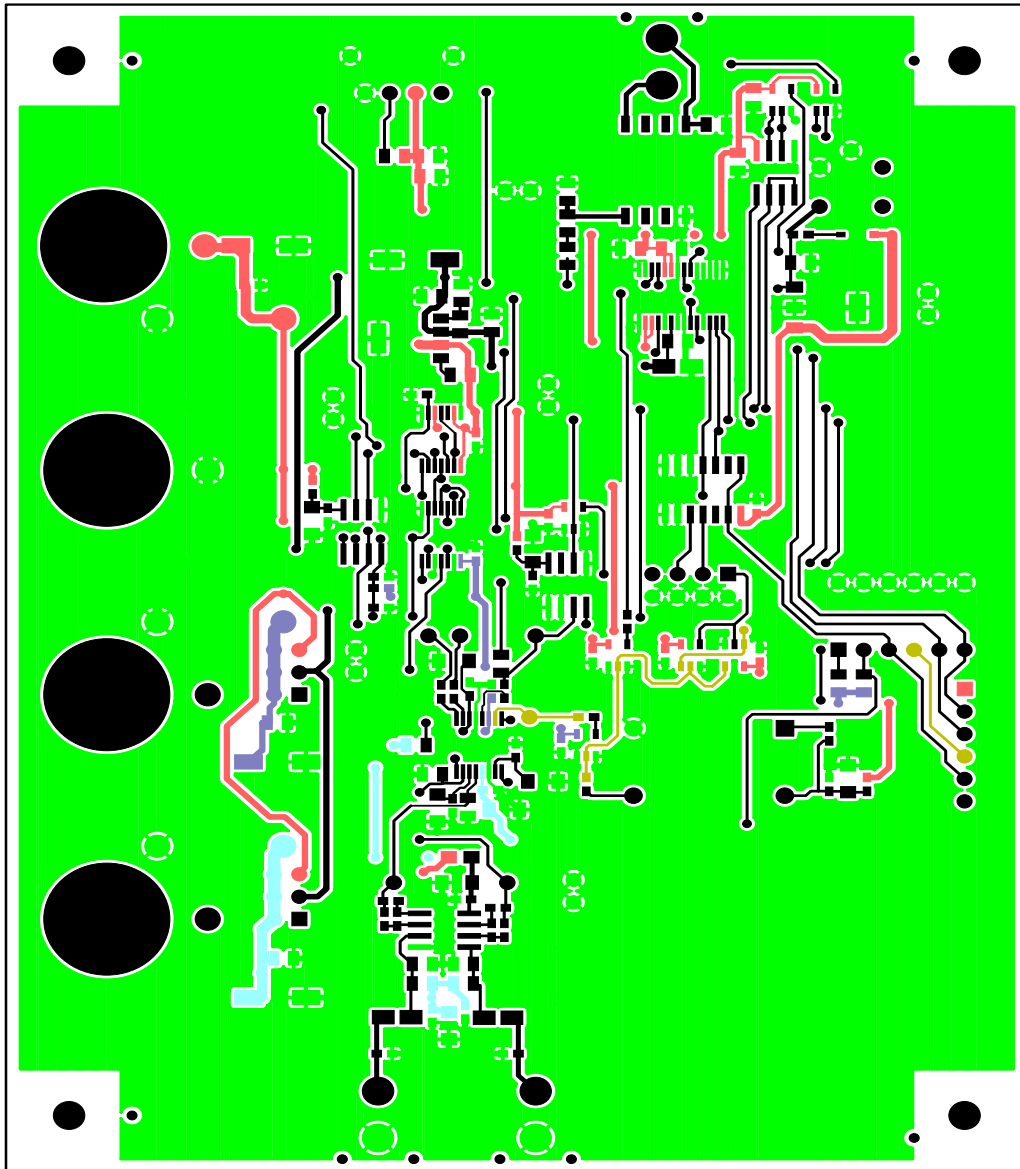


Figure 8. Top Layer

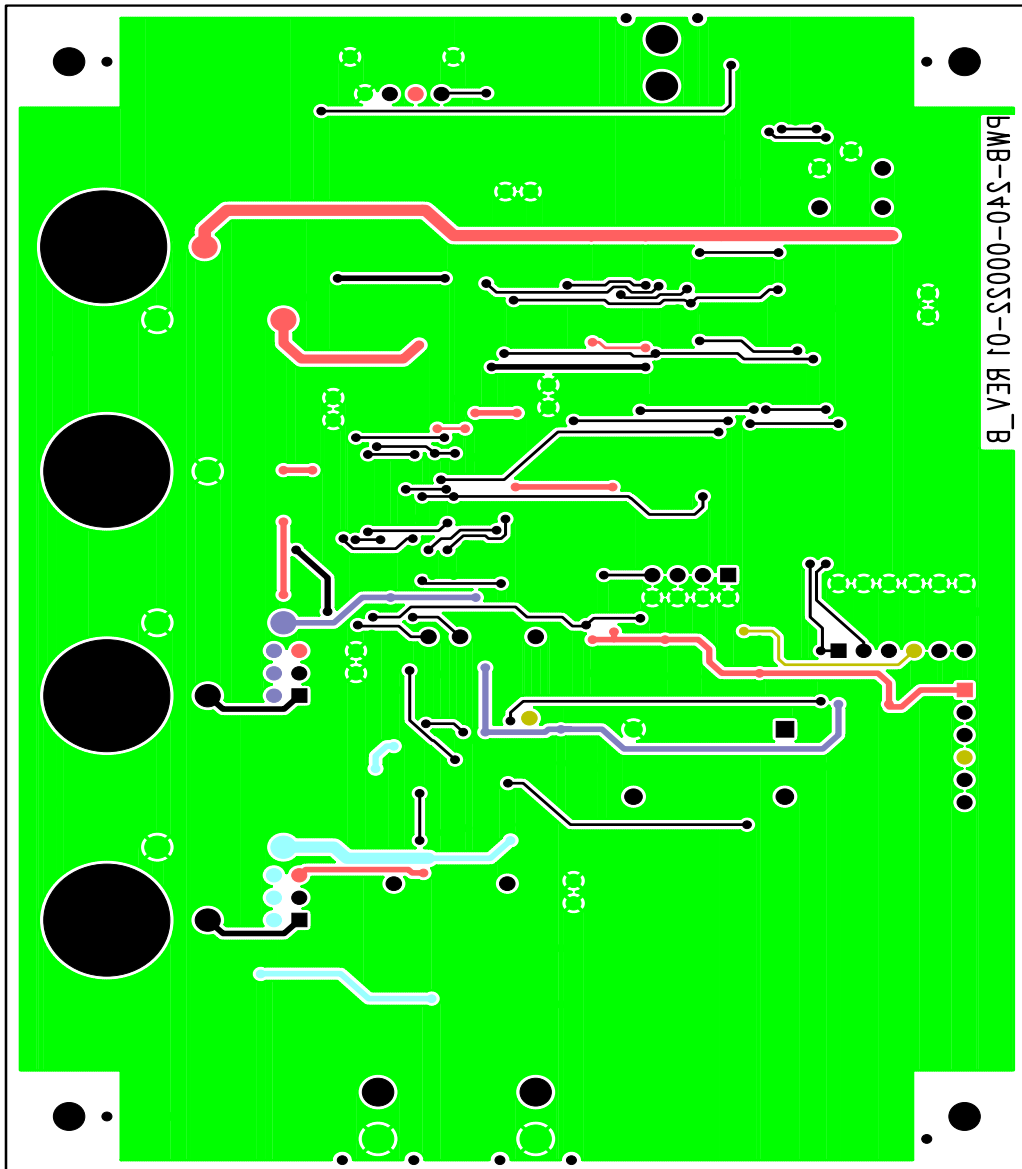


Figure 9. Bottom Layer

