3.3 V, Single Channel RS-232 Line Driver/Receiver

Preliminary Technical Data

ADM3101E

FEATURES

460 kbps data rate
1 Tx and 1 Rx
Meets EIA-232E specifications
0.1 µF charge pump capacitors
ESD protection to IEC1000-4-2 (801.2)
on CMOS and RS-232 I/Os
±8 kV: contact discharge
±15 kV: air gap discharge

APPLICATIONS

General-purpose RS-232 data link
Portable instruments
Handsets
Industrial/Telecom Diagonictics Ports

GENERAL DESCRIPTION

The ADM3101E transceiver is a high speed, single-channel RS-232/V.28 interface devices that operate from a single 3.3 V power supply. Low power consumption make it ideal for battery-powered portable instruments.

The ADM3101E conforms to the EIA-232E and CCITT V.28 specifications and operates at data rates up to 460 kbps.

All RS-232 (T_{OUT} and R_{IN}) and CMOS (T_{IN} and R_{OUT}) inputs and outputs are protected against electrostatic discharges (up to ±15 kV ESD Protection). This ensures compliance with IEC 1000-4-2 requirements.

This device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged/unplugged with the ±15kV ESD protection of the ADM3101E's I/O pins.

Emissions are also controlled to within very strict limits. CMOS technology is used to keep the power dissipation to an absolute minimum, allowing maximum battery life in portable applications.

Four external 0.1 µF charge pump capacitors are used for the voltage doubler/inverter permitting operation from a single 3.3 V supply.

The ADM3101E is available in a 12-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAMS

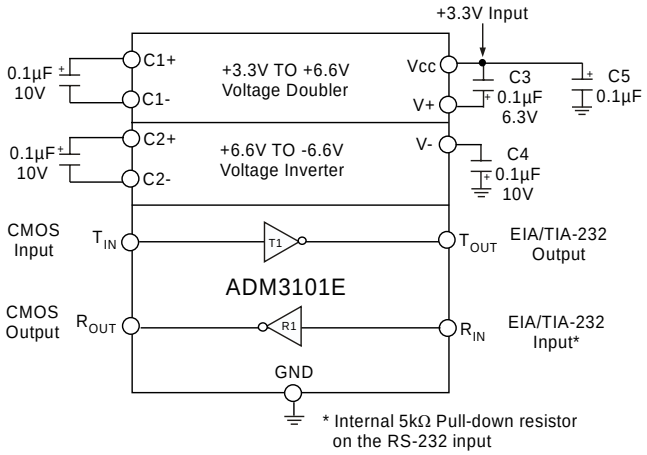

Figure 1. ADM3101E Functional Block Diagram

Rev. PrD

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REVISION HISTORY

SPECIFICATIONS

V_{CC} = 3.3 V ± 0.3 V, C1–C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
Operating Voltage Range	3.0	3.3	5.5	V	
V_{CC} Power Supply Current		1.0	2	mA	No load
		3	5	mA	R_L = 3 kΩ to GND
LOGIC					
Input Logic Threshold Low, V_{INL}			0.6	V	T_{IN}
Input Logic Threshold High, V_{INH}	1.4			V	T_{IN}
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, V_{CC} = 5.0V ± 0.5V
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, V_{CC} = 5.0V ± 0.5V
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
CMOS Output Voltage High, V_{OH}	V_{CC} − 0.6			V	I_{OUT} = −1 mA
Logic Pull-Up Current		5	10	µA	T_{IN} = GND to V_{CC}
RS-232 RECEIVER					
EIA-232 Input Voltage Range	−30		+30	V	Guaranteed by Design
EIA-232 Input Threshold Low	0.6	1.2		V	V_{CC} = 3.0V to 5.5V
EIA-232 Input Threshold High		1.6	2.4	V	
EIA-232 Input Threshold High		TBD	3.0	V	V_{CC} = 5.0V ± 0.5V
EIA-232 Input Hysteresis		0.4		V	
EIA-232 Input Resistance	3	5	7	kΩ	
RS-232 TRANSMITTER					
Output Voltage Swing (RS-232)	±5.0	±5.2		V	V_{CC} = 3.3V to 5.5V. All transmitter outputs loaded with 3 kΩ to ground.
Output Voltage Swing (RS-562)	TBD			V	V_{CC} = 3.0 V
Transmitter Output Resistance	300			Ω	V_{CC} = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±15		mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF.
Receiver Propagation Delay					
TPHL		0.4		µs	
TPLH		0.4		µs	
Transmitter Propagation Delay		300		µs	R_L = 3 kΩ, C_L = 1000 pF
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Transmitter Skew		30		ns	
Receiver Skew		300		ns	
Transition Region Slew Rate	5.5	10	30	V/µs	Guaranteed by Design from +3 V to −3 V or −3 V to +3 V, V_{CC} = +3.3 V, R_L = 3 kΩ, C_L = 1000 pF, T_A = 25°C
ESD Protection (RS-232 and CMOS I/O Pins)					
		±15		kV	Human Body Model
		±15		kV	IEC 1000-4-2 Air Discharge
		±8		kV	IEC 1000-4-2 Air Discharge

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
V+	(V_{CC} − 0.3 V) to +14 V
V−	+0.3 V to −14 V
Input Voltages	
T_{IN}	−0.3 V to (V+, +0.3 V)
R_{IN}	±30 V
Output Voltages	
T_{OUT}	±15 V
R_{OUT}	−0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration	
T_{OUT}	Continuous
Power Dissipation	
Power Dissipation CP-12	TBDmW
(Derate 6 mW/°C above 50°C)	
θ_{JA}, Thermal Impedance	48.7°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead-Free Temperature (Soldering, 10 s)	260°C

This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

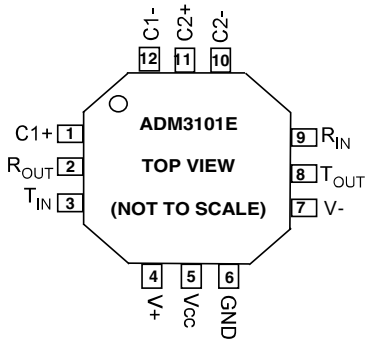

Figure 2. ADM3101E Pin Configuration

Table 3. Pin Function Descriptions

Mnemonic	Function
V_{CC}	Power Supply Input. 3.0 V to 5.5 V.
V+	Internally Generated Positive Supply (+6 V Nominal).
V–	Internally Generated Negative Supply (–6 V Nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+, C1–	External Capacitor 1 is connected between these pins. 0.1 µF capacitor is recommended but larger capacitors up to 47 µF may be used.
C2+, C2–	External Capacitor 2 is connected between these pins. 0.1 µF capacitor is recommended but larger capacitors up to 47 µF may be used.
T_{IN}	Transmitter (Driver) Input. This input accepts TTL/CMOS levels.
T_{OUT}	Transmitter (Driver) Output. This outputs RS-232 signal levels (typically ± 6 V).
R_{IN}	Receiver Input. This input accepts RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on the input.
R_{OUT}	Receiver Output. This outputs CMOS output logic levels.

TYPICAL PERFORMANCE CHARACTERISTICS

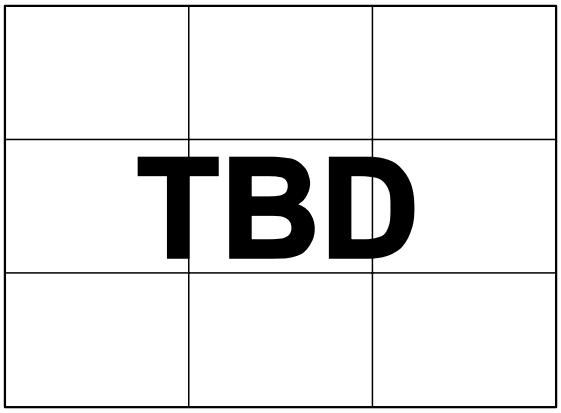

Figure 3. Transmitter Output Voltage High/Low vs. Load Capacitance @ 460 kbps

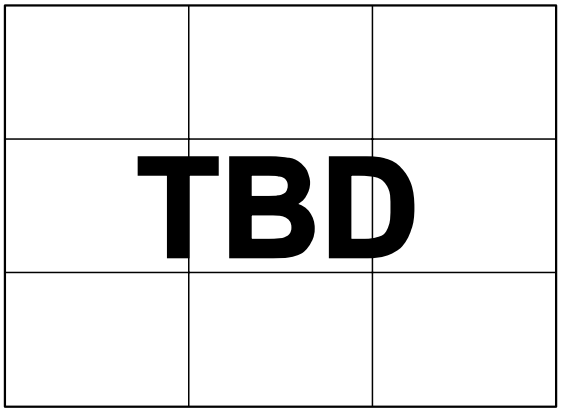

Figure 4. Transmitter Output Voltage vs. V_{CC}, RL = 3kΩ

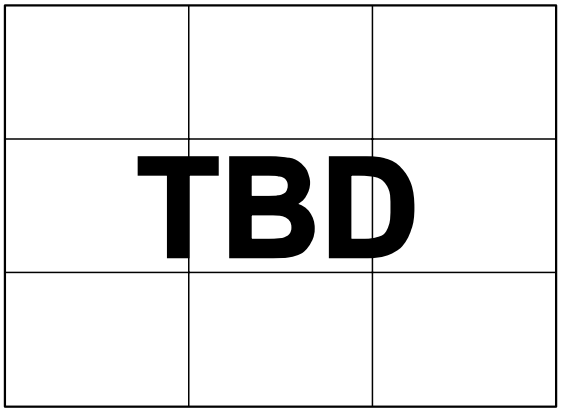

Figure 5. Transmitter Output Voltage Low/High vs. Load

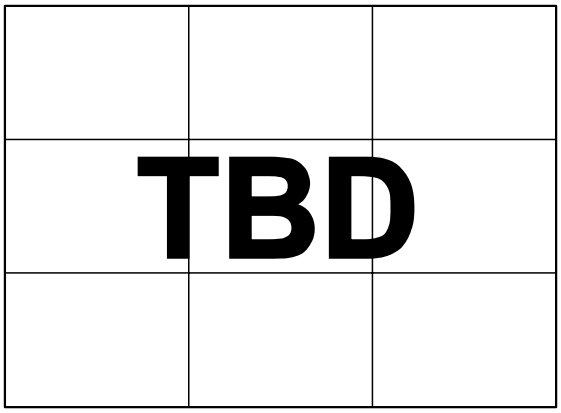

Figure 6. Charge Pump V+, V– vs. Load Current

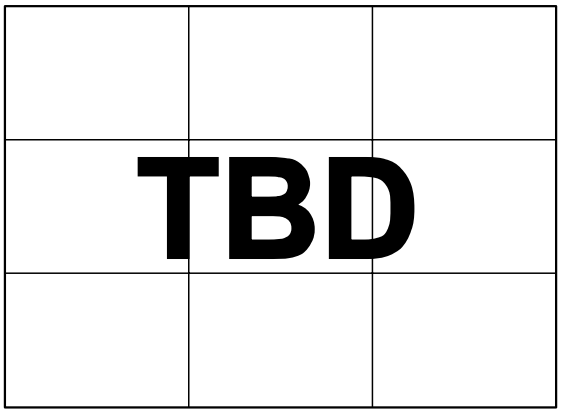

Figure 7. Charge Pump Impedance vs. V_{CC}

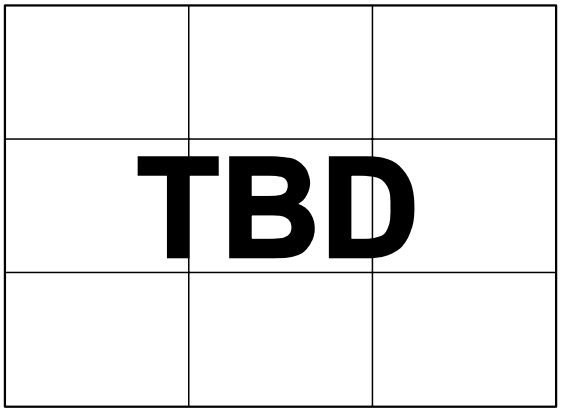

Figure 8. Power Supply Current vs. Load Capacitance

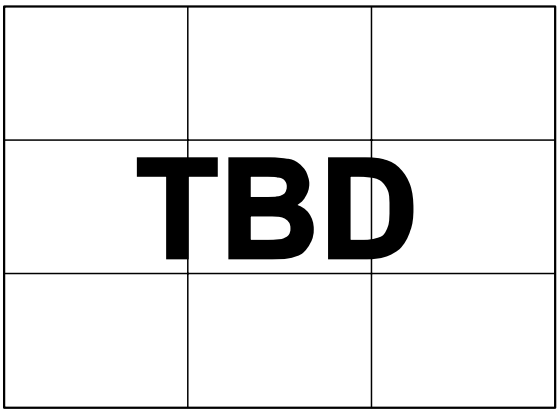

Figure 9. 460 kbps Data Transmission

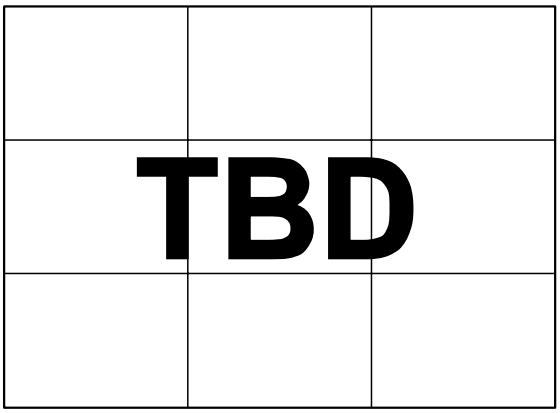

Figure 10. T_{IN} Voltage Threshold vs. Vcc

GENERAL DESCRIPTION

The ADM3101E is a single channel RS-232 line driver/receiver. Step-up voltage converters coupled with level shifting transmitters and receivers allow RS-232 levels to be developed while operating from a single 3.3 V supply.

CMOS technology is used to keep the power dissipation to an absolute minimum, allowing maximum battery life in portable applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of the following main sections:

- A charge pump voltage converter
- A 3.3 V logic to EIA-232 transmitter
- A EIA-232 to 3.3 V logic receiver

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±6.6 V supply from the input 3.3 V level. This is done in two stages by using a switched capacitor technique as illustrated in Figure 12 and Figure 13. First, the 3.3 V input supply is doubled to 6.6 V by using capacitor C1 as the charge storage element. The +6.6 V level is then inverted to generate −6.6 V using C2 as the storage element. C3 is shown connected between V+ and V_{CC}, but is equally effective if connected between V+ and GND.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be increased, if desired. Capacitor C3 is shown connected between V+ and V_{CC}. It is also acceptable to connect this capacitor between V+ and GND.

If desired, larger capacitors (up to 10 µF) can be used for capacitors C1–C4.

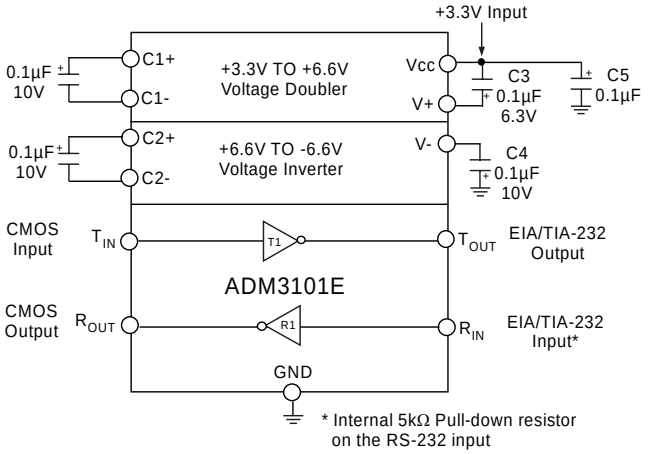

Figure 11. ADM3101E Typical Operating Circuit

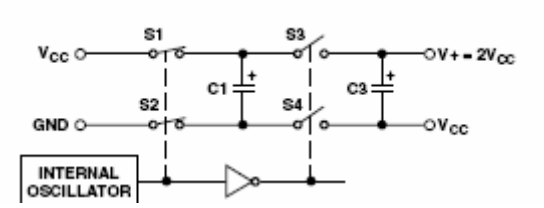

Figure 12. Charge Pump Voltage Doubler

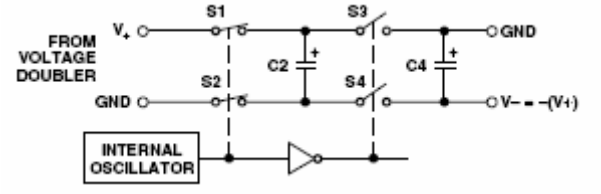

Figure 13. Charge Pump Voltage Inverter

Transmitter (Driver) Section

The driver convert the 3.3 V logic input levels into RS-232 output levels. With V_{CC} = 3.3 V and driving an RS-232 load, the output voltage swing is typically ±6 V. The T_{IN} pin has internally a weak pull-up which allows it to be driven by an open drain output, but the maximum operating datarate is reduced when the T_{IN} pin is been driven by a open drain pin.

Receiver Section

The receiver is an inverting level-shifters that accept RS-232 input level and translate it into a 3.3 V logic output level. The input has an internal 5 kΩ pull-down resistors to ground and is also protected against overvoltages of up to ±30 V. An unconnected input is pulled to 0 V by the internal 5 kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for an unconnected input or for an input connected to GND.

The receiver has a Schmitt-trigger input with a hysteresis level of 0.4 V. This ensures error-free reception for both a noisy input and for an input with slow transition times.

CMOS Input Voltage Thresholds

The ADM3101E CMOS input and output pins (T_{IN} and R_{OUT}) are designed to interface with 1.8V logic thresholds when the ADM3101E's Vcc = 3.3V.

The ADM3101E CMOS input and output pins (T_{IN} and R_{OUT}) are designed to interface with TTL/CMOS logic thresholds when the ADM3101E's Vcc = 5V.

ESD Protection on RS-232 and CMOS I/O pins

All RS-232 (T_{OUT} and R_{IN}) and CMOS (T_{IN} and R_{OUT}) inputs and outputs are protected against electrostatic discharges (up to ±15 kV). This ensures compliance with IEC 1000-4-2 requirements.

HIGH BAUD RATE

The ADM3101E features high slew rates permitting data transmission at rates well in excess of the EIA/RS-232 specifications. The RS-232 voltage levels are maintained at data rates up to 460 kbps even under worst case loading conditions, when T_{IN} is been driven by a push-pull output. This allows high speed data links between two terminals, or indeed it is suitable for the new generation ISDN modem standards that requires data rates of 230 kbps. The slew rate is internally controlled to less than 30 V/μs to minimize EMI interference.

OUTLINE DIMENSIONS

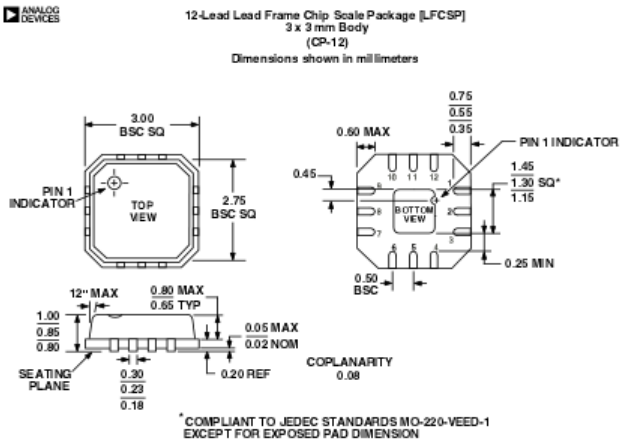

Figure 14. 12-Lead Frame Chip Scale package [LFCSP] (CP-12)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Options[1]
ADM3101EACPZ[1]	–40°C to +85°C	CP-12

[1] Z = Pb Free