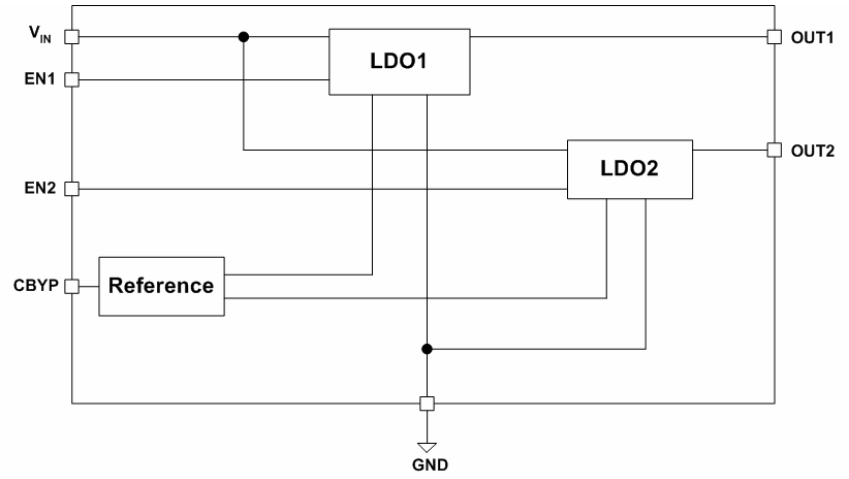
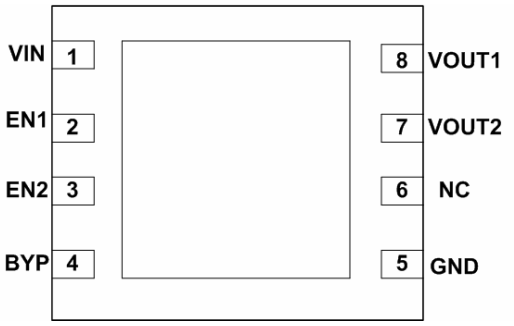
Block Diagram



Pin Configurations

Part Number	Pin Configurations
EUP7211 DFN-8	

Pin Description

PIN	Pin	DESCRIPTION
V_{IN}	1	Input voltage of the LDO
EN1	2	Enable input to regulator 1
EN2	3	Enable input logic, enable high
BYPASS	4	Optional bypass capacitor for noise reduction
GND	5	Ground
NC	6	No connection
V_{OUT2}	7	Output of regulator 2: 300mA output current
V_{OUT1}	8	Output of regulator 1: 150mA output current

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUP7211-1.5/2.8JIR1 EUP7211-1.5/2.8JIR0	DFN-8	CEXX P7211	-40 °C to 125°C
EUP7211-1.8/2.8JIR1 EUP7211-1.8/2.8JIR0	DFN-8	DEXX P7211	-40 °C to 125°C
EUP7211-1.8/3.3JIR1 EUP7211-1.8/3.3JIR0	DFN-8	DHXX P7211	-40 °C to 125°C
EUP7211-2.5/2.8JIR1 EUP7211-2.5/2.8JIR0	DFN-8	BEXX P7211	-40 °C to 125°C
EUP7211-2.85/2.85JIR1 EUP7211-2.85/2.85JIR0	DFN-8	FFXX P7211	-40 °C to 125°C

EUP7211□□□/□□□ □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: DFN

Output Voltage Option

Absolute Maximum Ratings

- V_{IN},V_{EN} ---------- -0.3V to 6V
- Power Dissipation (P_D) ---------- Internally Limited
- Junction Temperature ---------- -40°C to +125°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp ---------- 260°C

Operating Ratings

- V_{IN} ---------- 2.5 to 5.5V
- V_{EN} ---------- 0V to V_{IN}
- Junction Temperature ---------- -40°C to +125°C
- Thermal Resistance θ_{JA}(DFN-8) ---------- 60°C/W

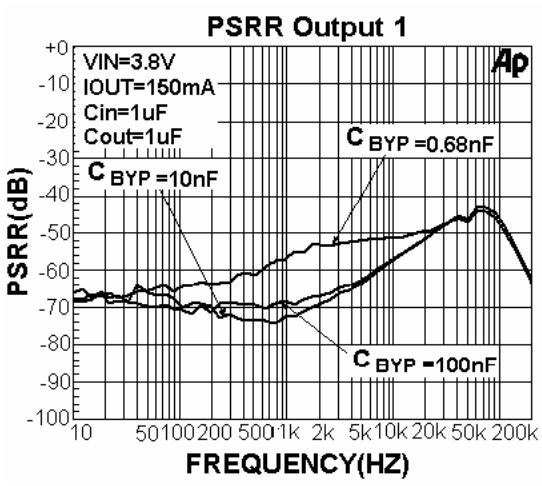
Electrical Characteristics

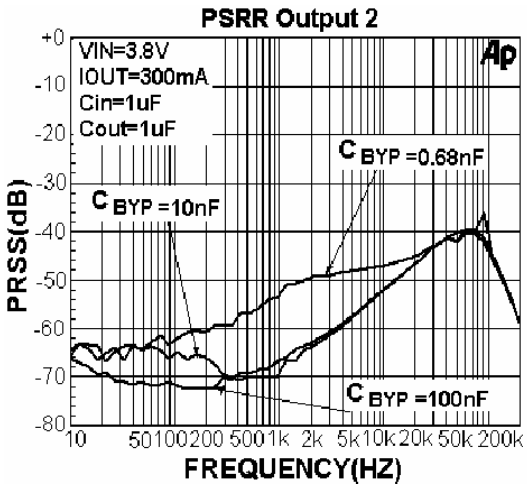
V_{IN}= V_{OUT} +1.0V, I_{OUT}=1mA, C_{OUT}=1µF. Typical values and limits appearing in standard typeface are for T_J= 25°C

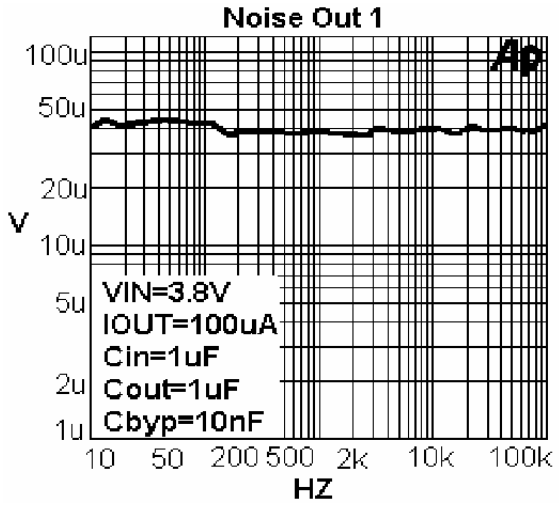
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\triangle V_{OUT}$	Output Voltage Accuracy	Variation from nominal Vout	-1.5		1.5	%
Reg Line	Line Regulation	Input range Vin=Vout+1V to 5.5V	-0.2	0.02	0.2	%/V
Reg Load	Load Regulation	Iout=100µA to 150mA(Vout 1 & Vout 2)		0.7	2	%
		Iout=100µA to 300mA(Vout)		1	2.5	
V_{Drop}	Dropout Voltage	Iout=150mA(Vout 1)		120	180	mV
		Iout=300mA(Vout 2)		240	350	
I_Q	Ground Pin Current	Iout 1=Iout2=0		150	170	µA
		Iout 1=150mA & Iout=300mA		250	300	
IQ_SD	Ground Pin Current in Shutdown	V_{EN}≦0.4V		3	5	µA
PSRR	Ripple Rejection	Freq.=1Khz; Cout=1.0µF; C_{BYP}=10nF		70		dB
Iout(Max)	Current Limit	Output 1 Short to Ground	150	340		mA
		Output 2 Short to Ground	300	580		
Noise	Output Voltage Noise	Cout=1.0µF;C_{BYP}=10nF; BW=10~100KHz		40		µVrms
Enable Input						
V_{EN}	Enable Input voltage	Logic Low (Regulator Shutdown)			0.6	V
		Logic High(Regulator Enable)	1.8			
I_{EN}	Enable Input Current	V_{IL}<0.6V (Regulator Shutdown)	-0.5	0.01	0.5	µA
		V_{IH}>1.8V (Regulator Enable)	-0.5	0.01	0.5	

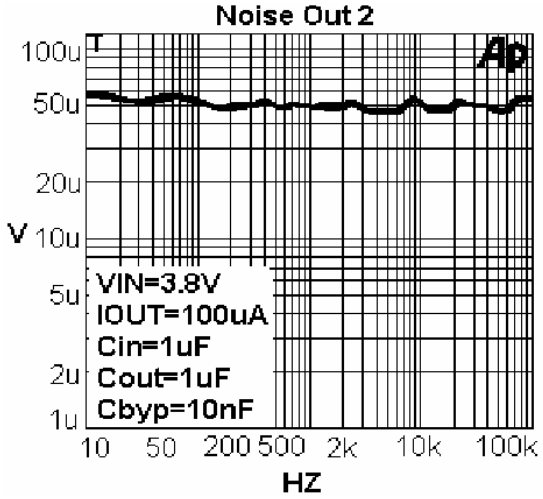
Typical Operating Characteristics

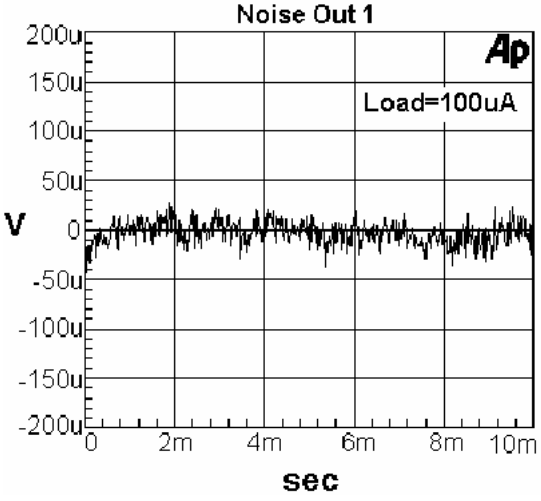
Unless otherwise specified, C_{IN}=C_{COUT}=1µF Ceramic, C_{BYPASS}=100nF, V_{IN}=V_{OUT}+1V, I_{OUT}= 100µA T_A=25°C, Enable pin is tied to V_{IN}.

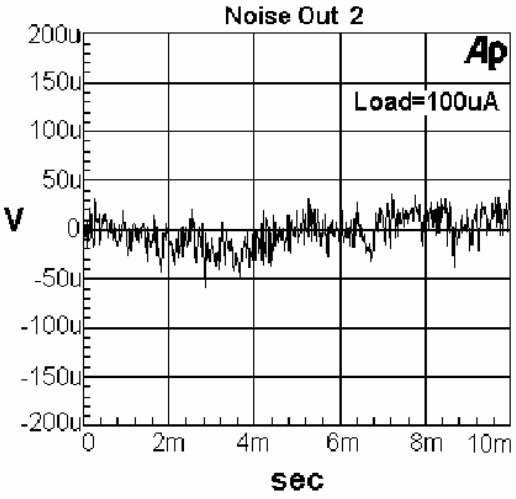


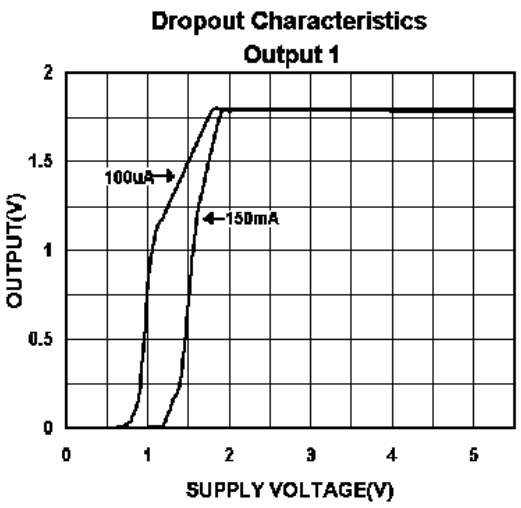


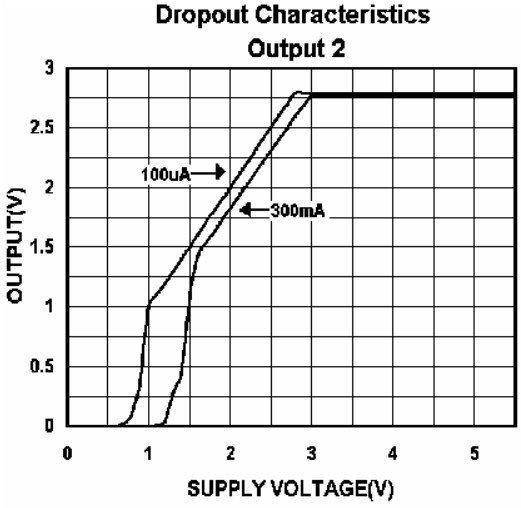


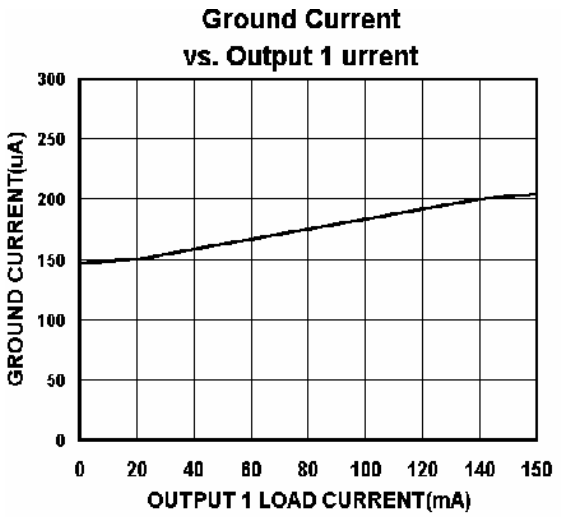


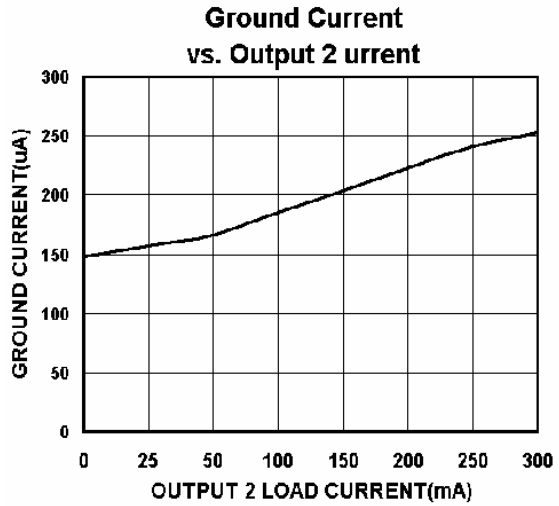


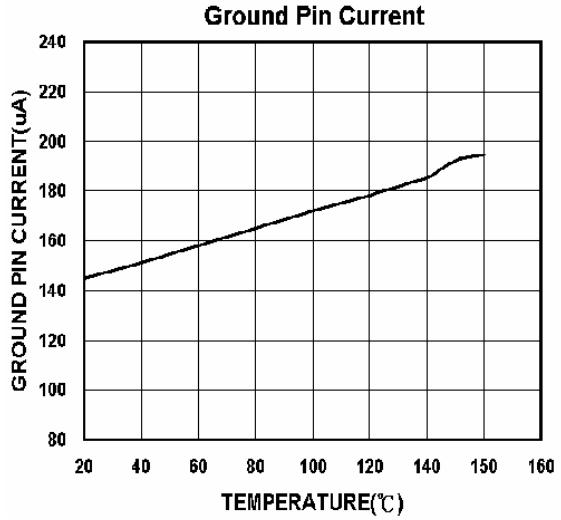


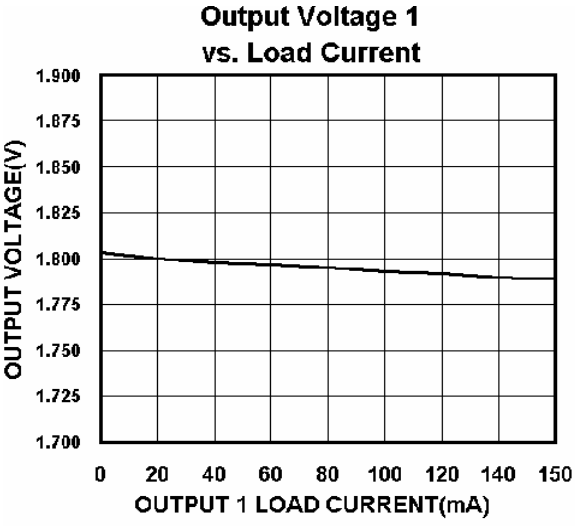

Dropout Characteristics
Output 1
OUTPUT(V)
SUPPLY VOLTAGE(V)
100uA
150mA
0
0.5
1
1.5
2
0
1
2
3
4
5

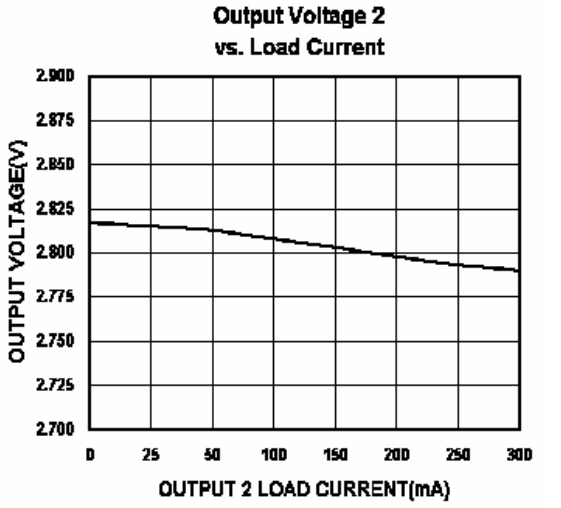

Dropout Characteristics
Output 2
OUTPUT(V)
SUPPLY VOLTAGE(V)
100uA
300mA
0
0.5
1
1.5
2
2.5
3
0
1
2
3
4
5

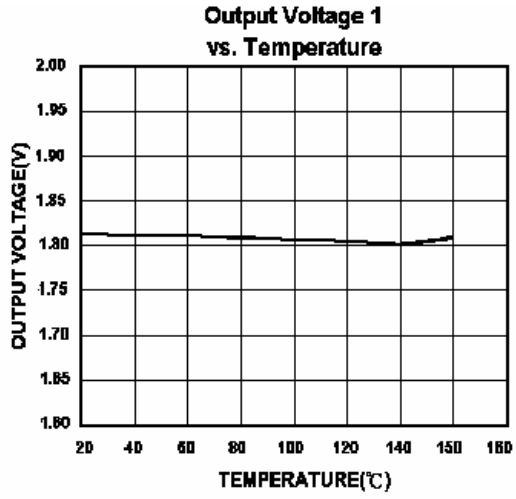

Ground Current
vs. Output 1 urrent
GROUND CURRENT(uA)
OUTPUT 1 LOAD CURRENT(mA)
0
50
100
150
200
250
300
0
20
40
60
80
100
120
140
150

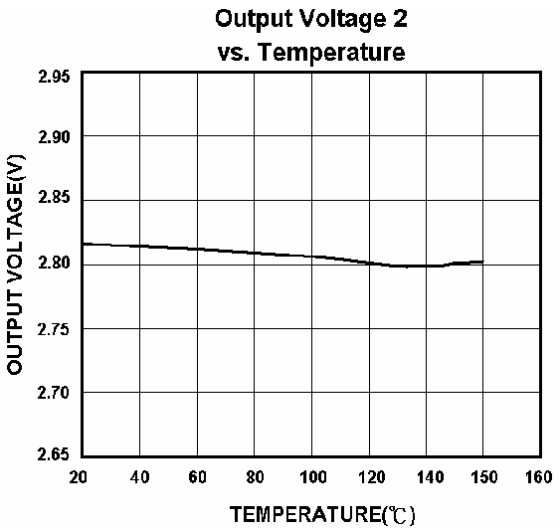

Ground Current
vs. Output 2 urrent
GROUND CURRENT(uA)
OUTPUT 2 LOAD CURRENT(mA)
0
50
100
150
200
250
300
0
25
50
100
150
200
250
300

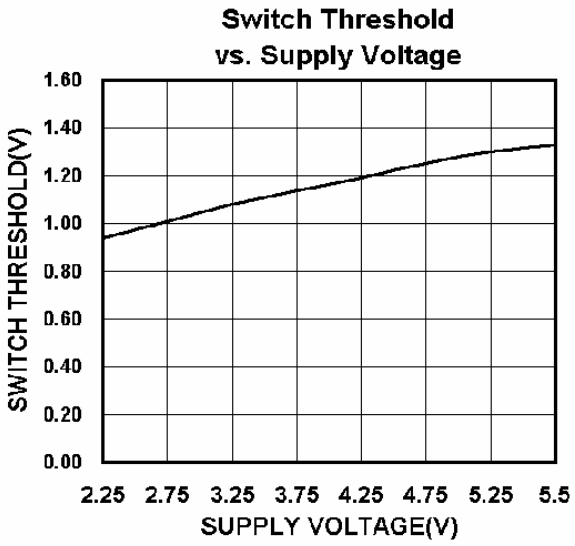

Ground Pin Current
GROUND PIN CURRENT(uA)
TEMPERATURE(℃)
80
100
120
140
160
180
200
220
240
20
40
60
80
100
120
140
150
160

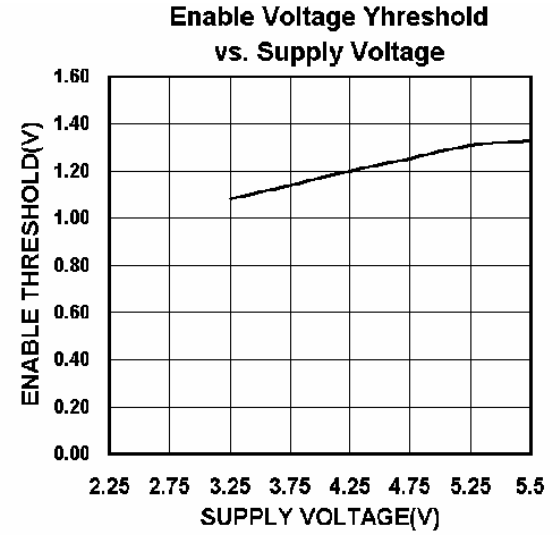

Output Voltage 1
vs. Load Current
OUTPUT VOLTAGE(V)
OUTPUT 1 LOAD CURRENT(mA)
1.700
1.725
1.750
1.775
1.800
1.825
1.850
1.875
1.900
0
20
40
60
80
100
120
140
150

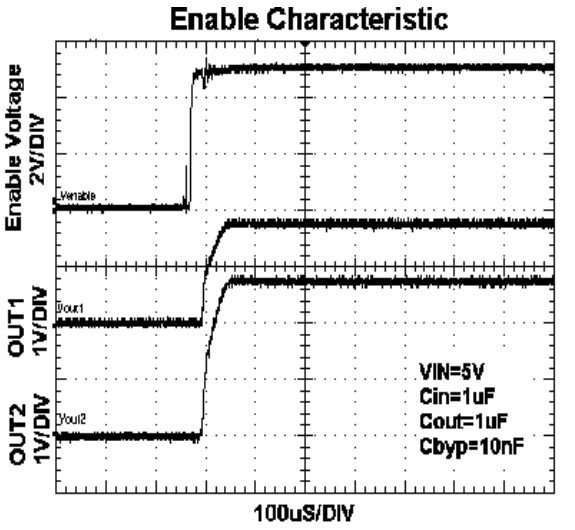

Output Voltage 2
vs. Load Current
OUTPUT VOLTAGE(V)
2.900
2.875
2.850
2.825
2.800
2.775
2.750
2.725
2.700
0
25
50
100
150
200
250
300
OUTPUT 2 LOAD CURRENT(mA)


Output Voltage 1
vs. Temperature
OUTPUT VOLTAGE(V)
2.00
1.95
1.90
1.85
1.80
1.75
1.70
1.65
1.60
20
40
60
80
100
120
140
150
160
TEMPERATURE(℃)

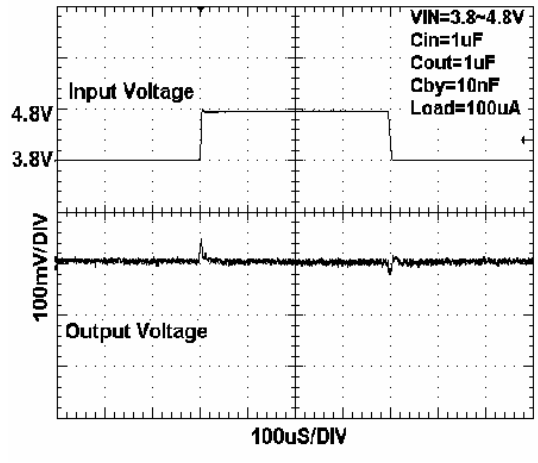

Output Voltage 2
vs. Temperature
OUTPUT VOLTAGE(V)
2.95
2.90
2.85
2.80
2.75
2.70
2.65
20
40
60
80
100
120
140
150
160
TEMPERATURE(℃)


Switch Threshold
vs. Supply Voltage
SWITCH THRESHOLD(V)
1.60
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
2.25
2.75
3.25
3.75
4.25
4.75
5.25
5.5
SUPPLY VOLTAGE(V)

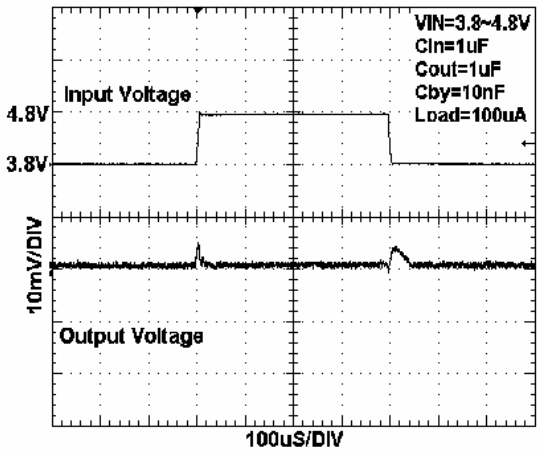

Enable Voltage Yhreshold
vs. Supply Voltage
ENABLE THRESHOLD(V)
1.60
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
2.25
2.75
3.25
3.75
4.25
4.75
5.25
5.5
SUPPLY VOLTAGE(V)


Enable Characteristic
Enable Voltage
2V/DIV
OUT1
1V/DIV
OUT2
1V/DIV
VIN=5V
Cin=1uF
Cout=1uF
Cbyp=10nF
100uS/DIV

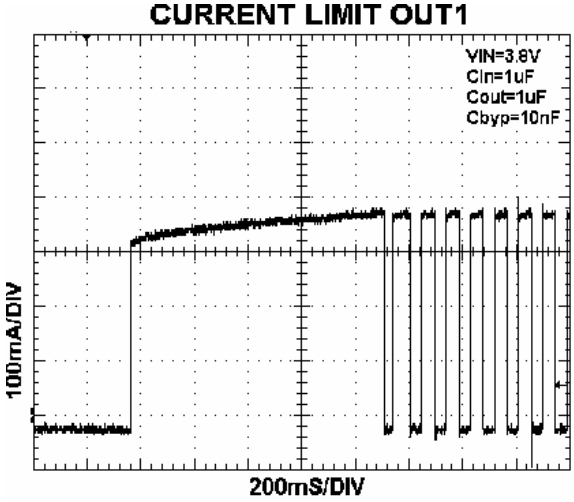
LINE TRANSIENT RESPONSE OUT1



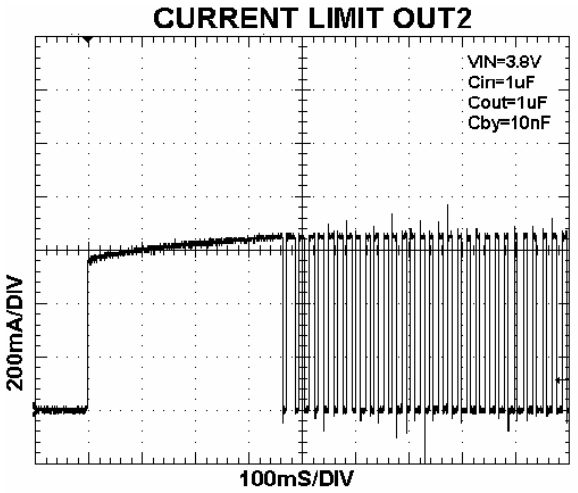
LINE TRANSIENT RESPONSE OUT2



CURRENT LIMIT OUT1



CURRENT LIMIT OUT2



Application Note

Function Description

The EUP7211 is a high performance, low quiescent current power management IC consisting of two μCap low dropout regulators, a power-on reset (POR) circuit and an open-drain driver. The first regulator is capable of sourcing 150mA at output voltages from 1.25V to 5V. The second regulator is capable of sourcing 300mA of current at output voltages from 1.25V to 5V. The second regulator has a POR circuit that monitors its output voltage and indicates when the output voltage is within 5% of nominal. The POR offers a delay time that is externally programmable with a single capacitor to ground. An open-drain driver completes the power management chipset, offering the capability of driving LEDs for keypad backlighting in applications such as cellphones.

Enable 1 and 2

The enable inputs allow for logic control of both output voltages with individual enable inputs. The EUP7211 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

External Capacitors

Like any low-dropout regulator, the EUP7211 requires external capacitors for regulator stability. The EUP7211 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitance of $\gtrsim$1μF or greater is required between the EUP7211 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Output Capacitor

The EUP7211 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (temperature characteristics X7R, X5R, Z5U, or Y5V) in 1 to 22μF range with 5mΩ to 500mΩ ESR range is suitable in the EUP7211 application circuit.

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5mΩ to 500mΩ)

No-Load Stability

The EUP7211 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

Capacitor Characteristics

The EUP7211 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1μF to 4.7μF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1μF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability by the EUP7211.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. Most large value ceramic capacitors ($\gtrsim$2.2μF) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25°C to 85°C. Therefore, X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

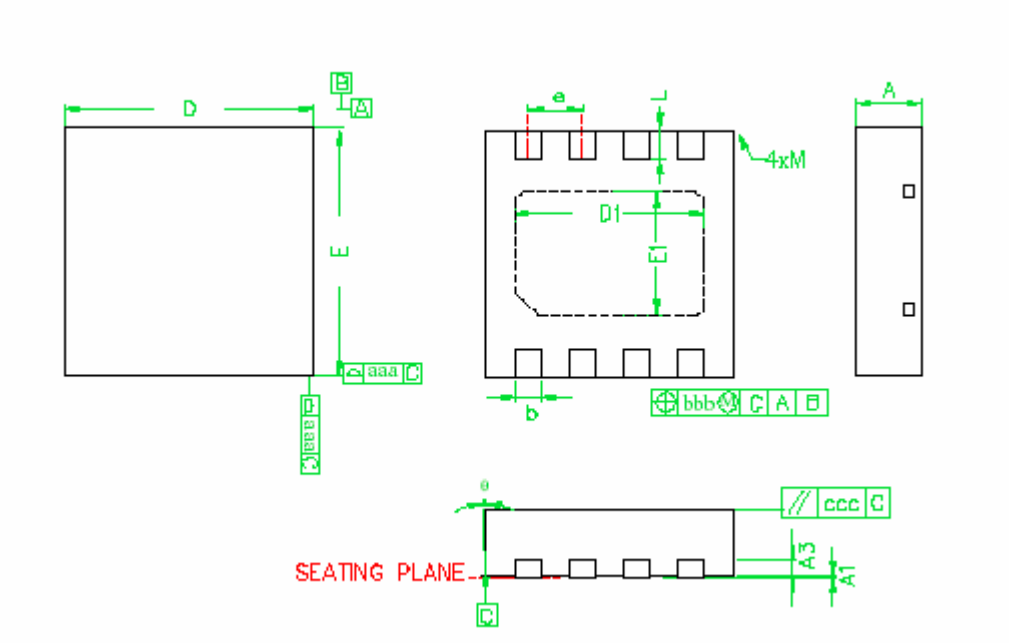
Noise Bypass Capacitor

Connecting a 0.01μF capacitor between the C_{BYPASS} pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the bandgap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The types of capacitors best suited for the noise bypass capacitor are ceramic and film.

Unlike many other LDO's, addition of a noise reduction capacitor does not effect the load transient response of the device

Packaging Information

DFN-8



NOTE

1. All dimensions are in millimeters, θ is in degrees
2. M: The maximum allowable corner on the molded plastic body corner
3. Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.15mm per side
4. Dimension E does not include interterminal mold protrusions or terminal protrusions. Interminal mold protrusions and/or terminal protrusions shall not exceed 0.20mm per side
5. Dimension b applies to plated terminals. Dimension A1 is primarily Y terminal plating, but may or may not include a small protrusion of terminal below the bottom surface of the package
6. Burr shall not exceed 0.060mm
7. JEDEC MO-229

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.81	0.9	1.00
A1	0	0.015	0.03
A3	------	0.20 REF	------
B	0.25	0.30	0.37
D	2.85	3.00 BSC	3.15
D1	------	2.3 BSC	------
E	2.85	3.00 BSC	3.15
E1	------	1.5 BSC	------
e	------	0.65 BSC	-----
L	0.25	0.35	0.45
aaa	------	0.25	------
bbb	------	0.10	------
ccc	------	0.10	------
M	------	------	0.05
θ	-12	------	0