December 4, 2001 FN7178

8ns High-Speed Comparator

The EL5181 comparator is designed for operation in single supply and dual supply applications with 5V to 12V between V_S+ and V_S-. For single supplies, the inputs can operate from 0.1V below ground for use in ground sensing applications.

The output side of the comparator can be supplied from a single supply of 2.7V to 5V. The rail-to-rail output swing enables direct connection of the comparator to both CMOS and TTL logic circuits.

The latch input of the EL5181 can be used to hold the comparator output value by applying a low logic level to the pin.

The EL5181 is available in the 8-pin SO package and is specified for operation over the full -40°C to +85°C temperature range. Also available are a dual (EL5281), a window comparator (EL5283), and quad versions (EL5481 and EL5482).

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. NO.
EL5181CS	8-Pin SO	-	MDP0027
EL5181CS-T7	8-Pin SO	7”	MDP0027
EL5181CS-T13	8-Pin SO	13”	MDP0027

Features

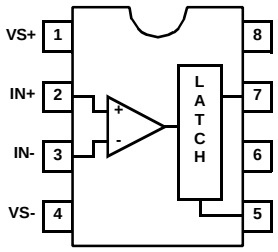
- 8ns Typ. propagation delay
- 5V to 12V input supply
- +2.7V to +5V output supply
- True-to-ground input
- Rail-to-rail outputs
- Active low latch
- Dual available (EL5281)
- Window comparator (EL5283)
- Quad available (EL5481 & EL5482)
- Pin-compatible 4ns family available (EL5x85, EL5287 & EL5486)

Applications

- Threshold detection
- High speed sampling circuits
- High speed triggers
- Line receivers
- PWM circuits
- High speed V/F converters

Pinout

EL5181
(8-PIN SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Analog Supply Voltage (V_S+ to V_S-) . . . . . +12.6V
Digital Supply Voltage (V_{SD} to GND) . . . . . +7V
Differential Input Voltage . . . . . [(V_S-) -0.2V] to [(V_S+) +0.2V]
Common-mode Input Voltage . . . . . [(V_S-) -0.2V] to [(V_S+) +0.2V]
Latch Input Voltage . . . . . -0.2V to [(V_{SD}) +0.2V]

Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . 125°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

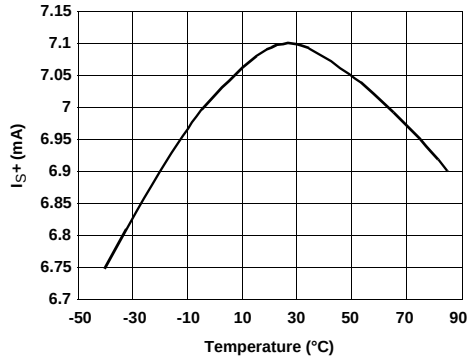
Electrical Specifications

V_S = ±5V, V_{SD} = 5V, R_L = 2.3kΩ, C_L = 15pF, T_A = 25°C, unless otherwise specified.

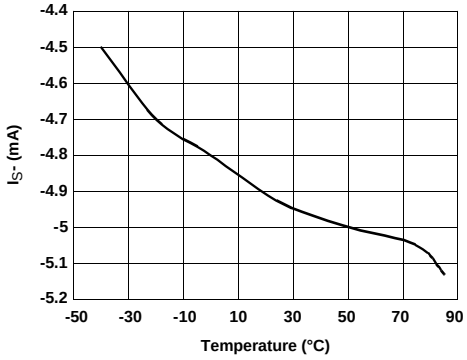
PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT						
V_{OS}	Input Offset Voltage	V_{CM} = 0V, V_O = 2.5V		1	4	mV
I_B	Input Bias Current		-6	-3.5		µA
C_{IN}	Input Capacitance			5		pF
I_{OS}	Input Offset Current	V_{CM} = 0V, V_O = 2.5V	-2.5	0.5	2.5	µA
V_{CM}	Input Voltage Range		(V_S-) - 0.1		(V_S+) - 2.25	V
CMRR	Common-mode Rejection Ratio	-5.1V < V_{CM} < +2.75V	65	90		dB
OUTPUT						
V_{OH}	Output High Voltage	V_{IN} > 250mV	V_{SD} - 0.6	V_{SD} - 0.4		V
V_{OL}	Output Low Voltage	V_{IN} > 250mV		GND + 0.25	GND + 0.5	V
DYNAMIC PERFORMANCE						
t_{PD}+	Positive Going Delay Time	V_{IN} = 1V_{P-P}, V_{OD} = 50mV		8	12	ns
t_{PD}-	Negative Going Delay Time	V_{IN} = 1V_{P-P}, V_{OD} = 50mV		8	12	ns
SUPPLY						
I_S+	Positive Analog Supply Current			7	8.2	mA
I_S-	Negative Analog Supply Current			5	6.5	mA
I_{SD}	Digital Supply Current	Output high		4	5	mA
		Output low		0.75	1	mA
PSRR	Power Supply Rejection Ratio		60	80		dB
LATCH						
V_{LH}	Latch Input Voltage High				2.0	V
V_{LL}	Latch Input Voltage Low		0.8			V
I_{LH}	Latch Input Current High	V_{LH} = 3.0V	-30	-18		µA
I_{LL}	Latch Input Current Low	V_{LL} = 0.3V	-30	-24		µA
t_d+	Latch Disable to High Delay			6		ns
t_D-	Latch Disable to Low Delay			6		ns
t_S	Minimum Setup Time			2		ns
t_H	Minimum Hold Time			1		ns
t_{PW}(D)	Minimum Latch Disable Pulse Width			10		ns

Typical Performance Curves

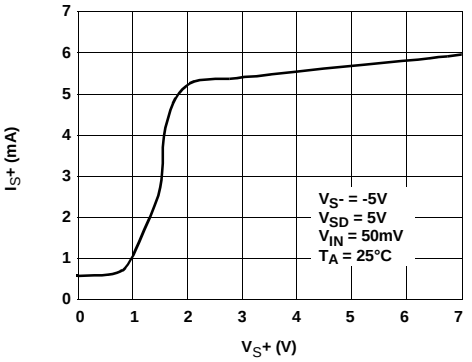
Positive Supply Current vs Temperature



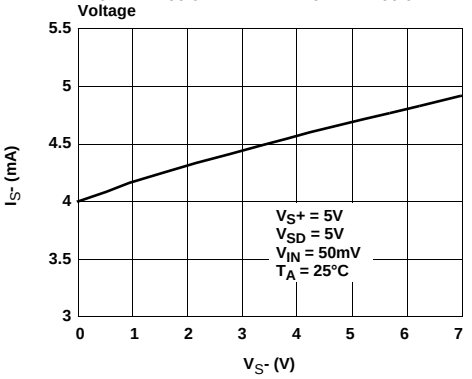
Negative Supply Current vs Temperature



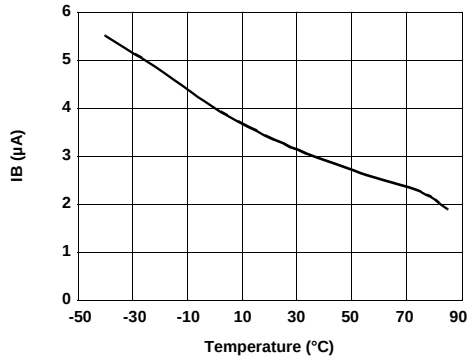
Positive Supply Current vs Supply Voltage



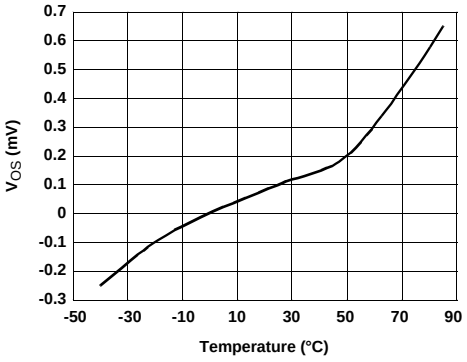
Negative Supply Current vs Negative Supply Voltage



Input Bias Current vs Temperature

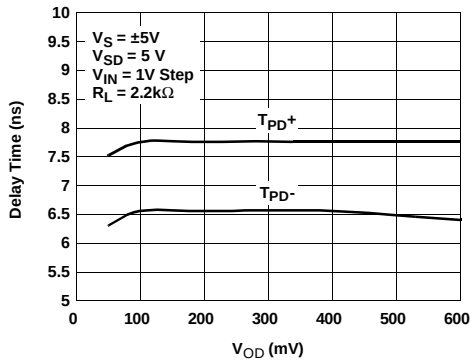


Offset Voltage vs Temperature

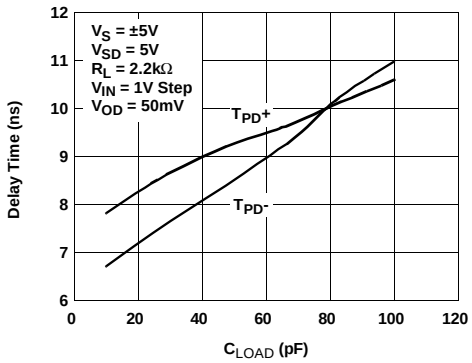


Typical Performance Curves (Continued)

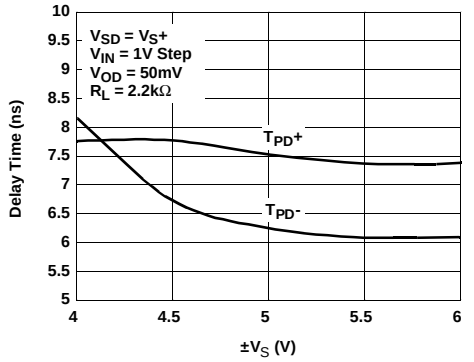
Propagation Delay vs Overdrive



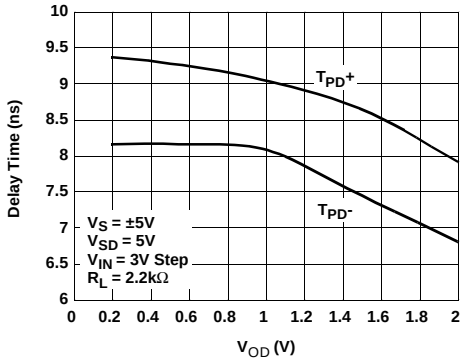
Propagation Delay vs Load Capacitance



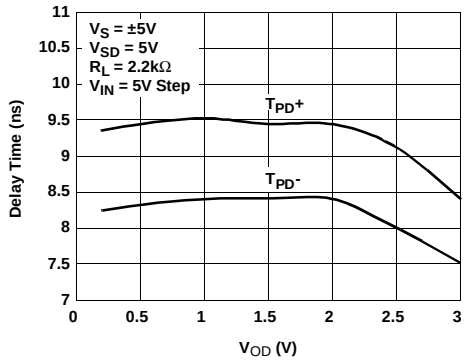
Propagation Delay vs Supply Voltage



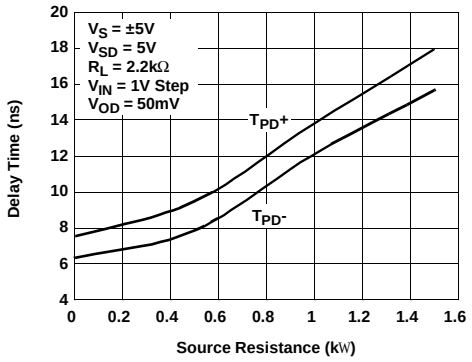
Propagation Delay vs Overdrive



Propagation Delay vs Overdrive

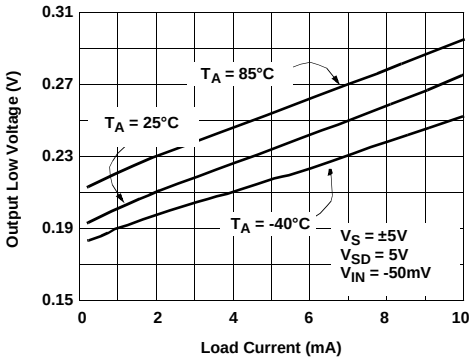


Propagation Delay vs Source Resistance

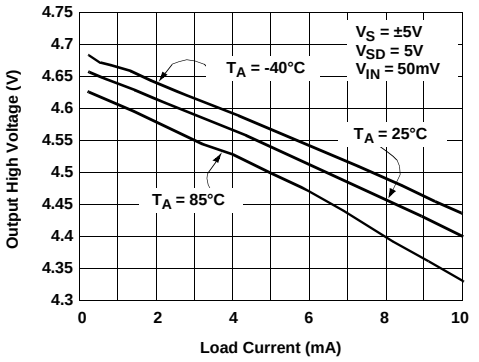


Typical Performance Curves (Continued)

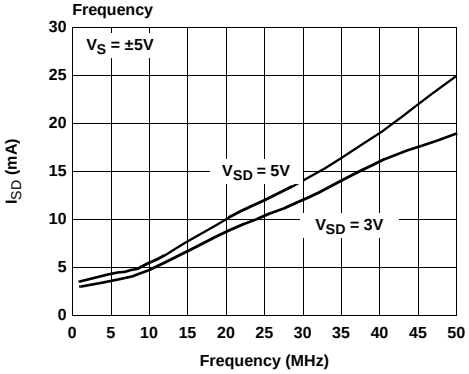
Output Low Voltage vs Load Current



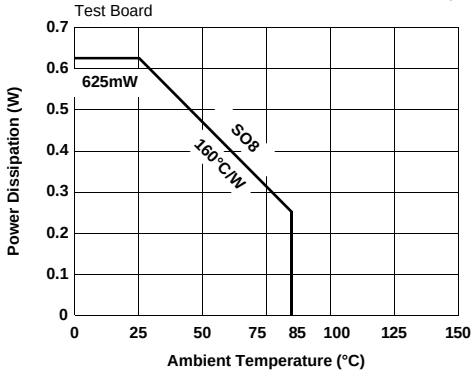
Output High Voltage vs Load Current



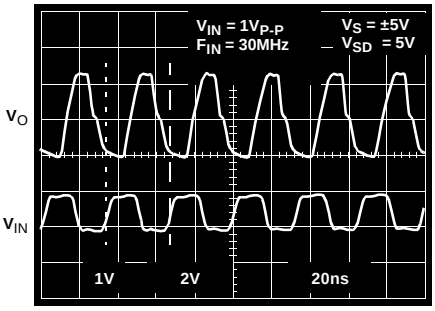
Digital Supply Current vs Input Switching Frequency



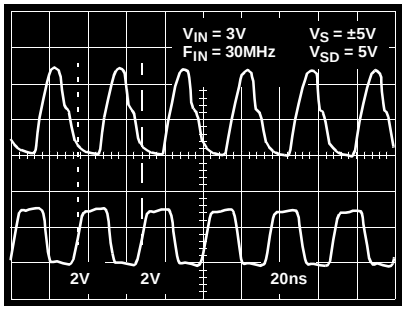
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 Low Effective Thermal Conductivity Test Board



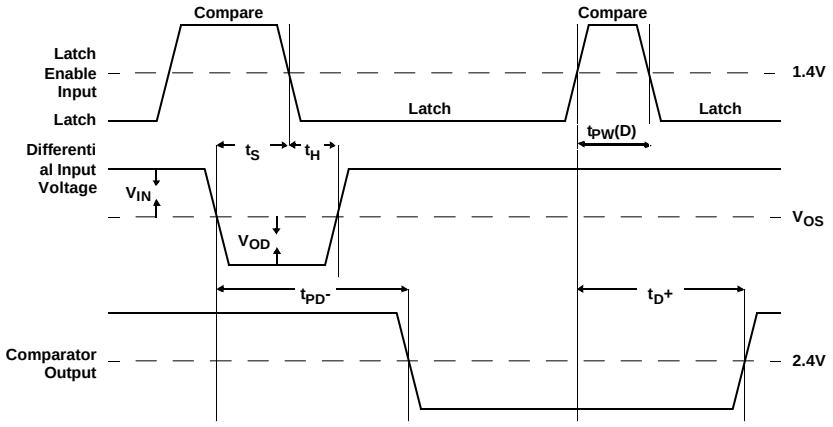
Output with 30MHz Input
$V_{IN} = 1V_{P-P}$



Output with 30MHz Input
$V_{IN} = 3V_{P-P}$



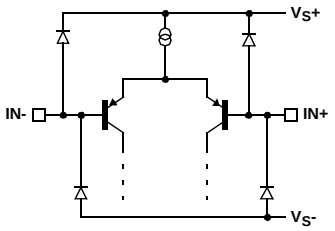
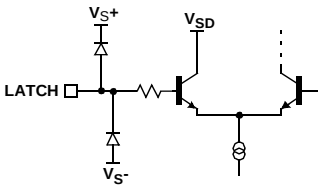
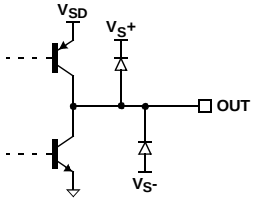
Timing Diagram



Definition of Terms

TERM	DEFINITION
V_{OS}	Input Offset Voltage - Voltage applied between the two input terminals to obtain CMOS logic threshold at the output
V_{IN}	Input Voltage Pulse Amplitude - Usually set to 1V for comparator specifications
V_{OD}	Input Voltage Overdrive - Usually set to 50mV and in opposite polarity to V_{IN} for comparator specifications
$t_{PD}+$	Input to Output High Delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the CMOS logic threshold of an output low to high transition
$t_{PD}-$	Input to Output Low Delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the CMOS logic threshold of an output high to low transition
t_D+	Latch Disable to Output High Delay - The propagation delay measured from the latch signal crossing the CMOS threshold in a low to high transition to the point of the output crossing CMOS threshold in a low to high transition
t_D-	Latch Disable to Output Low Delay - The propagation delay measured from the latch signal crossing the CMOS threshold in a low to high transition to the point of the output crossing CMOS threshold in a high to low transition
t_S	Minimum Setup Time - The minimum time before the negative transition of the latch signal that an input signal change must be present in order to be acquired and held at the outputs
t_H	Minimum Hold Time - The minimum time after the negative transition of the latch signal that an input signal must remain unchanged in order to be acquired and held at the output
t_{PW} (D)	Minimum Latch Disable Pulse Width - The minimum time that the latch signal must remain high in order to acquire and hold an input signal change

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	V_S+	Positive supply voltage	
2	IN+	Positive input	 Circuit 1
3	IN-	Negative input	(Reference Circuit 1)
4	V_S-	Negative supply voltage	
5	LATCH	Latch input	 Circuit 2
6	GND	Digital ground	
7	OUT	Output	 Circuit 3
8	V_{SD}	Digital Supply	

Applications Information

Power Supplies and Circuit Layout

The EL5181 comparator operates with single and dual supply with 5V to 12V between V_S+ and V_S-. The output side of the comparator is supplied by a single supply from 2.7V to 5V. The rail to rail output swing enables direct connection of the comparator to both CMOS and TTL logic circuits. As with many high speed devices, the supplies must be well bypassed. Elantec recommends a 4.7µF tantalum in parallel with a 0.1µF ceramic. These should be placed as close as possible to the supply pins. Keep all leads short to reduce stray capacitance and lead inductance. This will also minimize unwanted parasitic feedback around the comparator. The device should be soldered directly to the PC board instead of using a socket. Use a PC board with a good, unbroken low inductance ground plane. Good ground plane construction techniques enhance stability of the comparators.

Input Voltage Considerations

The EL5181 input range is specified from 0.1V below V_S- to 2.25V below V_S+. The criterion for the input limit is that the output still responds correctly to a small differential input signal. The differential input stage is a pair of PNP transistors, therefore, the input bias current flows out of the device. When either input signal falls below the negative input voltage limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on, resulting in a significant increase of input bias current. If one of the inputs goes above the positive input voltage limit, the output will still maintain the correct logic level as long as the other input stays within the input range. However, the propagation delay will increase. When both inputs are outside the input voltage range, the output becomes unpredictable. Large differential voltages greater than the supply voltage should be avoided to prevent damages to the input stage.

Input Slew Rate

Most high speed comparators oscillate when the voltage of one of the inputs is close to or equal to the voltage on the other input due to noise or undesirable feedback. For clean output waveform, the input must meet certain minimum slew rate requirements. In some applications, it may be helpful to apply some positive feedback (hysteresis) between the output and the positive input. The hysteresis effectively causes one comparator's input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. For the EL5181, the propagation delay increases when the input slew rate increases for low overdrive voltages. With high overdrive voltages, the propagation delay does not change much with the input slew rate.

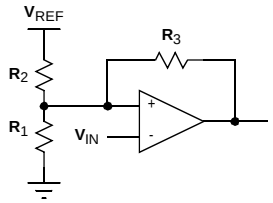
Latch Pin Dynamics

The EL5181 contains a “transparent” latch for each channel. The latch pin is designed to be driven with either a TTL or CMOS output. When the latch is connected to a logic high level or left floating, the comparator is transparent and immediately responds to the changes at the input terminals. When the latch is switched to a logic low level, the comparator output remains latched to its value just before the latch’s high-to-low transition. To guarantee data retention, the input signal must remain the same state at least 1ns (hold time) after the latch goes low and at least 2ns (setup time) before the latch goes low. When the latch goes high, the new data will appear at the output in approximately 6ns (latch propagation delay).

Hysteresis

Hysteresis can be added externally. The following two methods can be used to add hysteresis.

Inverting comparator with hysteresis:



R_3 adds a portion of the output to the threshold set by R_1 and R_2. The calculation of the resistor values are as follows:

Select the threshold voltage V_{TH} and calculate R_1 and R_2. The current through R_1/R_2 bias string must be many times greater than the input bias current of the comparator:

$$V_{TH} = V_{REF} \times \frac{R_1}{R_1 + R_2}$$

Let the hysteresis be V_H, and calculate R_3:

$$R_3 = \frac{V_O}{V_H} \times (R_1 \parallel R_2)$$

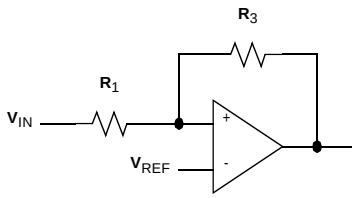
where:

V_O=V_{SD}-0.8V (swing of the output)

Recalculate R_2 to maintain the same value of V_{TH}:

$$R_2 1 = ((V_{REF}) - \left(V_{TH}\right) \div \left(\frac{V_{TH}}{R_1}\right) + \frac{V_{TH} - 0.5V_{SD}}{R_3}\right)$$

Non inverting comparator with hysteresis:



R_3 adds a portion of the output to the positive input. Note that the current through R_3 should be much greater than the input bias current in order to minimize errors. The calculation of the resistor values as follows:

Pick the value of R_1. R_1 should be small (less than 1kΩ) in order to minimize the propagation delay time.

Choose the hysteresis V_H and calculate R_3:

$$R_3 = (V_{SD} - 0.8) \times \frac{R_1}{V_H}$$

Check the current through R_3 and make sure that it is much greater than the input bias current as follows:

$$I = \frac{0.5V_{SD} - V_{REF}}{R_3}$$

The above two methods will generate hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R_3 is low enough to affect the bias string and adjustment of R_1 may be required.

Power Dissipation

When switching at high speeds, the comparator's drive capability is limited by the rise in junction temperature caused by the internal power dissipation. For reliable operation, the junction temperature must be kept below T_{JMAX} (125°C).

An approximate equation for the device power dissipation is as follows. Assume the power dissipation in the load is very small:

$$P_{DISS} = (V_S \times I_S + V_{SD} \times I_{SD})$$

where:

V_S is the analog supply voltage from V_S+ to V_S-

I_S is the analog quiescent supply current per comparator

V_{SD} is the digital supply voltage from V_{SD} to ground

I_{SD} is the digital supply current per comparator

I_{SD} strongly depends on the input switching frequency. Please refer to the performance curve to choose the input driving frequency. Having obtained the power dissipation, the maximum junction temperature can be determined as follows:

$$T_{JMAX} = T_{MAX} + \Theta_{JA} \times P_{DISS}$$

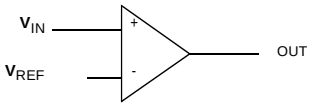
where:

T_{MAX} is the maximum ambient temperature

θ_{JA} is the thermal resistance of the package

Threshold Detector

The inverting input is connected to a reference voltage and the non-inverting input is connected to the input. As the input passes the V_{REF} threshold, the comparator's output changes state. The non-inverting and inverting inputs may be reversed.



Crystal Oscillator

A simple crystal oscillator using one comparator of an EL5181 is shown below. The resistors R_1 and R_2 set the bias point at the comparator's non-inverting input. Resistors R_3, R_4, and C_1 set the inverting input node at an appropriate DC average voltage based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. Although the EL5181 will give the correct logic output when an input is outside the common mode range, additional delays may occur when it is so operated. Therefore, the DC bias voltages at the inputs are set about 500mV below the center of the common mode range and the 200Ω resistor attenuates the feedback to the non-inverting input. The circuit will operate with most AT-cut crystal from 1MHz to 8MHz over a 2V to 7V supply range. The output duty cycle for this circuit is roughly 50% at 5V V_{CC}, but it is affected by the tolerances of the resistors. The duty cycle can be adjusted by changing V_{CC} value.