

**OVERVIEW**

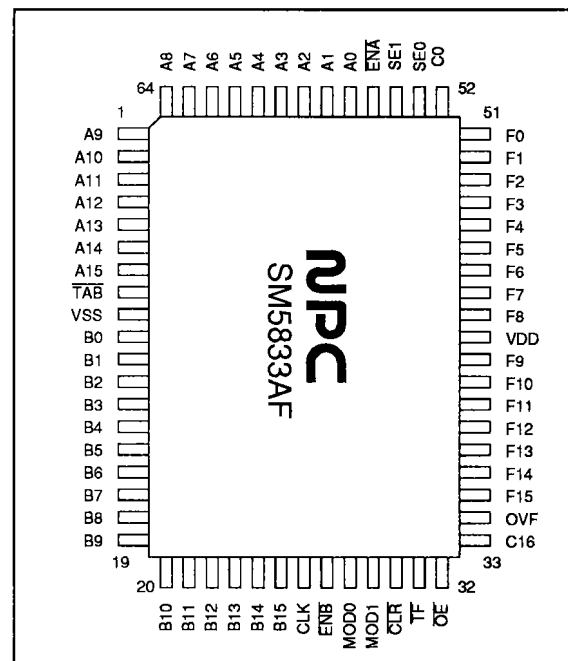
The SM5833AF is a 16-bit adder fabricated in Molybdenum-gate CMOS. It performs addition, subtraction and accumulation of 2s-complement data at a maximum operating speed of 25 MHz. It features input and output registers that can be programmed independently for transparent operation.

The SM5833AF can be employed as the input/output adder in a video-bandwidth digital filter, enabling two-dimensional filtering and other high-speed signal processing.

**FEATURES**

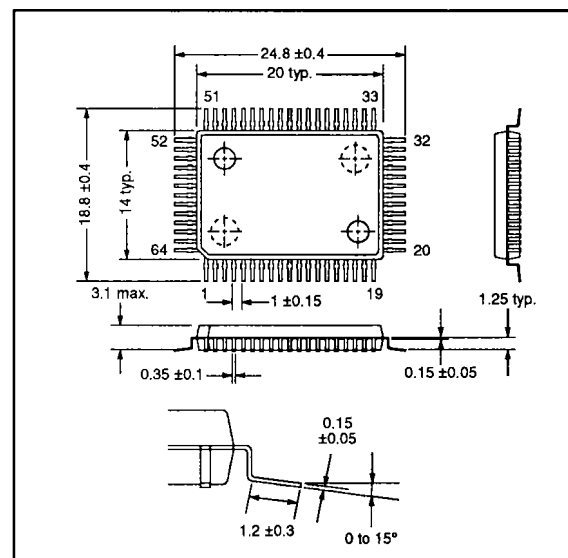
- 16-bit 2s-complement input/output data
- Comprises
  - 16-bit CLA adder
  - 1 × 16-bit parallel output register
  - 2 × 16-bit parallel input registers
- 25 MHz maximum operating frequency (register mode only)
- Adder, subtractor and accumulator operating modes
- Overflow detected flag
- Input data sign bit extension
- Input/output register transparent operation
- Two SM5833AFs can be cascaded to form a 32-bit adder.
- TTL-compatible input/output levels
- Molybdenum-gate CMOS process
- Single 5 V supply
- 64-pin flat plastic package

**PINOUT**



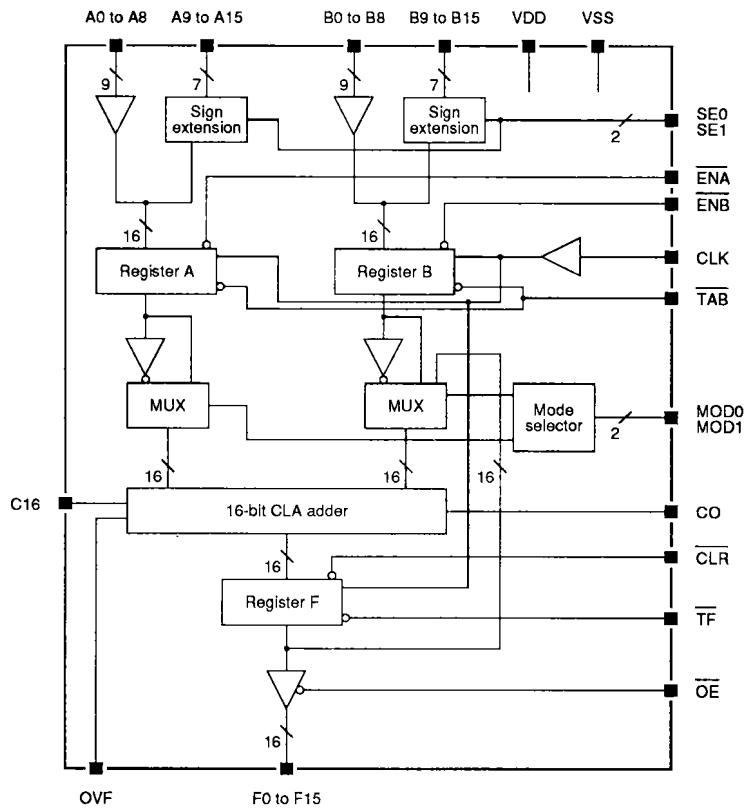
**PACKAGE DIMENSIONS**

Unit: mm



SM5833AF

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	A9	ip	Input A (bit 9)
2	A10	ip	Input A (bit 10)
3	A11	ip	Input A (bit 11)
4	A12	ip	Input A (bit 12)
5	A13	ip	Input A (bit 13)
6	A14	ip	Input A (bit 14)
7	A15	ip	Input A (MSB)
8	TAB	ip	Register A and B transparent-mode select
9	VSS		Ground
10	B0	ip	Input B (LSB)
11	B1	ip	Input B (bit 1)
12	B2	ip	Input B (bit 2)
13	B3	ip	Input B (bit 3)
14	B4	ip	Input B (bit 4)
15	B5	ip	Input B (bit 5)
16	B6	ip	Input B (bit 6)

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Number	Name	I/O	Description
17	B7	ip	Input B (bit 7)
18	B8	ip	Input B (bit 8)
19	B9	ip	Input B (bit 9)
20	B10	ip	Input B (bit 10)
21	B11	ip	Input B (bit 11)
22	B12	ip	Input B (bit 12)
23	B13	ip	Input B (bit 13)
24	B14	ip	Input B (bit 14)
25	B15	ip	Input B (MSB)
26	CLK	i	Clock input (rising-edge trigger)
27	ENB	ip	Register B enable
28	MOD0	ip	Mode select pins
29	MOD1	ip	
30	CLR	ip	Output register clear
31	TF	ip	Output register transparent-mode select
32	OE	ip	Output enable
33	C16	o	Carry output
34	OVF	o	Overflow detected flag
35	F15	o	Sum operation output (MSB)
36	F14	o	Sum operation output (bit 14)
37	F13	o	Sum operation output (bit 13)
38	F12	o	Sum operation output (bit 12)
39	F11	o	Sum operation output (bit 11)
40	F10	o	Sum operation output (bit 10)
41	F9	o	Sum operation output (bit 9)
42	VDD		Supply voltage
43	F8	o	Sum operation output (bit 8)
44	F7	o	Sum operation output (bit 7)
45	F6	o	Sum operation output (bit 6)
46	F5	o	Sum operation output (bit 5)
47	F4	o	Sum operation output (bit 4)
48	F3	o	Sum operation output (bit 3)
49	F2	o	Sum operation output (bit 2)
50	F1	o	Sum operation output (bit 1)
51	F0	o	Sum operation output (LSB)
52	C0	i	Carry input
53	SE0	ip	Sign extension bit select pins
54	SE1	ip	

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Number	Name	I/O	Description
55	$\overline{\text{EN}}\text{A}$	ip	Register A enable
56	A0	ip	Input A (LSB)
57	A1	ip	Input A (bit 1)
58	A2	ip	Input A (bit 2)
59	A3	ip	Input A (bit 3)
60	A4	ip	Input A (bit 4)
61	A5	ip	Input A (bit 5)
62	A6	ip	Input A (bit 6)
63	A7	ip	Input A (bit 7)
64	A8	ip	Input A (bit 8)

### Note

i = input pin, ip = input pin with pull-up resistance, o = output pin

## SPECIFICATIONS

### Absolute Maximum Ratings

$V_{SS} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD}$	-3.0 to 7.0	V
Input voltage range	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	$P_D$	250	mW
Storage temperature range	$T_{stg}$	-40 to 125	deg. C
Soldering temperature	$T_{sld}$	255	deg. C
Soldering time	$t_{sld}$	10	s

### Recommended Operating Conditions

$V_{SS} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD}$	4.75 to 5.25	V
Operating temperature range	$T_{opr}$	-20 to 70	deg. C

### DC Electrical Characteristics

$V_{DD} = 4.75 \text{ to } 5.25 \text{ V}$ ,  $T_a = -20 \text{ to } 70 \text{ deg. C}$ ,  $V_{SS} = 0 \text{ V}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby supply current	$I_S$	$V_{IN} = V_{DD} \text{ or } 0 \text{ V}$	-	1.0	10.0	$\mu\text{A}$
Operating supply current	$I_{DD}$	$V_{DD} = 5 \text{ V}$ , $f = 25 \text{ MHz}$ , all outputs open	-	30	60	mA
HIGH-level input voltage	$V_{IH}$	See notes 1 and 2.	2.4	-	-	V
LOW-level input voltage	$V_{IL}$		-	-	0.5	V

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
F0 to F15, C16 and OVF HIGH-level output voltage	$V_{OH}$	$I_{OH} = -0.1$ mA. See note 3.	2.5	–	–	V
F0 to F15, C16 and OVF LOW-level output voltage	$V_{OL}$	$I_{OL} = 4.0$ mA. See note 3.	–	–	0.4	V
LOW-level input current	$I_{IL}$	$V_{IN} = 0$ V. See note 2.	–	10	20	$\mu$ A
HIGH-level input leakage current	$I_{LH}$	$V_{IN} = V_{DD}$ . See notes 1 and 2.	–	–	1.0	$\mu$ A
LOW-level input leakage current	$I_{LL}$	$V_{IN} = 0$ V. See note 1.	–	–	1.0	$\mu$ A
F0 to F15 high-impedance HIGH-level output leakage current	$I_{ZH}$	$\overline{V_{OE}} = V_{IH}$ , $V_{OUT} = V_{DD}$	–	–	5.0	$\mu$ A
F0 to F15 high-impedance LOW-level output leakage current	$I_{ZL}$	$\overline{V_{OE}} = V_{IH}$ , $V_{OUT} = 0$ V	–	–	5.0	$\mu$ A

### Notes

1. Pins CLK and C0 are TTL-level inputs.
2. Pins A0 to A15, B0 to B15, MOD0, MOD1, SE0, SE1,  $\overline{CLR}$ ,  $\overline{TAB}$ ,  $\overline{TF}$ ,  $\overline{ENA}$ ,  $\overline{ENB}$  and  $\overline{OE}$  are TTL-level inputs with pull-up resistances.
3. Pins F0 to F15, C16 and OVF are TTL-level outputs.

## AC Electrical Characteristics

### Standard register mode

$V_{DD} = 4.75$  to  $5.25$  V,  $T_a = -20$  to  $70$  deg. C,  $V_{SS} = 0$  V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	$f_{CLK}$	50% duty, $\overline{TAB} = \text{HIGH}$ , $\overline{TF} = \text{HIGH}$	0	–	25	MHz
Clock pulsewidth	$t_{W1}$	See figure 1.	15	–	–	ns
Clock rise time	$t_r$		–	–	100	ns
Clock fall time	$t_f$		–	–	100	ns
A0 to A15 and B0 to B15 data setup time	$t_{S1}$	$\overline{TAB} = \text{HIGH}$ . See figure 2.	12	–	–	ns
A0 to A15 and B0 to B15 data hold time	$t_{H1}$		3	–	–	ns
C0 carry setup time	$t_{S2}$	$\overline{TF} = \text{HIGH}$ . See figure 3.	22	–	–	ns
C0 carry hold time	$t_{H2}$		0	–	–	ns
$\overline{CLR}$ clear setup time	$t_{S3}$	$\overline{TF} = \text{HIGH}$ . See figure 4.	15	–	–	ns
$\overline{CLR}$ clear hold time	$t_{H3}$		15	–	–	ns
$\overline{ENA}$ and $\overline{ENB}$ enable setup time	$t_{S4}$	$\overline{TAB} = \text{HIGH}$ . See figure 5.	15	–	–	ns
$\overline{ENA}$ and $\overline{ENB}$ enable hold time	$t_{H4}$		3	–	–	ns
MOD0 and MOD1 mode setup time	$t_{S5}$	$\overline{TF} = \text{HIGH}$	100	–	–	ns
MOD0 and MOD1 mode hold time	$t_{H5}$		0	–	–	ns

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CLK to $F_n$ data output delay time	$t_{PLH1}$	$\overline{TF} = \text{HIGH}$ . See figure 6. See note 1.	–	–	28	ns
	$t_{PHL1}$		–	–	28	
CLK to C16 carry output delay time	$t_{PLH2}$	$\overline{TAB} = \text{HIGH}$ . See figure 7. See note 1.	–	–	50	ns
	$t_{PHL2}$		–	–	50	
CLK to C16 carry output hold time	$t_{OH1}$		15	–	–	ns
CLK to OVF overflow output delay time	$t_{PLH3}$	$\overline{TAB} = \text{HIGH}$ . See figure 9. See note 1.	–	–	56	ns
	$t_{PHL3}$		–	–	56	
CLK to OVF overflow output hold time	$t_{OH2}$		15	–	–	ns
C0 to C16 carry output delay time	$t_{PLH4}$	See figure 7. See note 1.	–	–	40	ns
	$t_{PHL4}$		–	–	40	
C0 to OVF overflow output delay time	$t_{PLH5}$	See figure 9. See note 1.	–	–	40	ns
	$t_{PHL5}$		–	–	40	
F0 to F15 output enable delay time	$t_{PZL}$	See figure 13. See note 2.	–	–	35	ns
	$t_{PZH}$		–	–	35	
F0 to F15 output disable delay time	$t_{PLZ}$	See figure 13. See note 2.	–	–	35	ns
	$t_{PHZ}$		–	–	35	
$\overline{OE}$ pulsewidth	$t_{W2}$	See figure 13.	20	–	–	ns
Input capacitance	$C_{IN}$	$f = 1 \text{ MHz}$	–	–	10	pF
Output capacitance	$C_{OUT}$	$f = 1 \text{ MHz}, V_{OE} = V_{IH}$	–	–	20	pF

### Notes

1. Measurement circuit 1
2. Measurement circuit 2
3. Typical values are measured at  $V_{DD} = 5 \text{ V}$  and  $T_a = 25 \text{ deg. C}$ .

### Transparent register mode

$\overline{TAB} = \text{LOW}, \overline{TF} = \text{HIGH}$

$V_{DD} = 4.75 \text{ to } 5.25 \text{ V}, T_a = -20 \text{ to } 70 \text{ deg. C}, V_{SS} = 0 \text{ V}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
A0 to A15 and B0 to B15 data setup time	$t_{SS}$	See figure 2.	42	–	–	ns
A0 to A15 and B0 to B15 data hold time	$t_{HS}$		0	–	–	ns
CLK to $F_n$ data output delay time	$t_{PLH1}$	See figure 6. See note 1.	–	–	28	ns
	$t_{PHL1}$		–	–	28	
C0 to C16 carry output delay time	$t_{PLH4}$	See figure 8. See note 1.	–	–	40	ns
	$t_{PHL4}$		–	–	40	

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
C0 to OVF overflow output delay time	t <sub>PLH5</sub>	See figure 10. See note 1.	–	–	40	ns
	t <sub>PHL5</sub>		–	–	40	
A and B to C16 carry output delay time	t <sub>PLH6</sub>	See figure 8. See note 1.	–	–	57	ns
	t <sub>PHL6</sub>		–	–	57	
A and B to OVF overflow output delay time	t <sub>PLH7</sub>	See figure 10. See note 1.	–	–	63	ns
	t <sub>PHL7</sub>		–	–	63	

Notes

1. Measurement circuit 1
2. Measurement circuit 2

$\overline{\text{TAB}}$  = HIGH,  $\overline{\text{TF}}$  = LOW

V<sub>DD</sub> = 4.75 to 5.25 V, T<sub>a</sub> = –20 to 70 deg. C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
A0 to A15 and B0 to B15 data setup time	t <sub>S1</sub>	See figure 2.	12	–	–	ns
A0 to A15 and B0 to B15 data hold time	t <sub>H1</sub>		3	–	–	
CLK to C16 carry output delay time	t <sub>PLH2</sub>	See figure 7. See note 1.	–	–	50	ns
	t <sub>PHL2</sub>		–	–	50	
CLK to C16 carry output hold time	t <sub>OH1</sub>		15	–	–	ns
CLK to OVF overflow output delay time	t <sub>PLH3</sub>	See figure 9. See note 1.	–	–	56	ns
	t <sub>PHL3</sub>		–	–	56	
CLK to OVF overflow output hold time	t <sub>OH2</sub>		15	–	–	ns
C0 to C16 carry output delay time	t <sub>PLH4</sub>	See figure 7. See note 1.	–	–	40	ns
	t <sub>PHL4</sub>		–	–	40	
C0 to OVF overflow output delay time	t <sub>PLH5</sub>	See figure 9. See note 1.	–	–	40	ns
	t <sub>PHL5</sub>		–	–	40	
CLK to F <sub>n</sub> data output delay time	t <sub>PLH8</sub>	See figure 11. See note 1.	–	–	58	ns
	t <sub>PHL8</sub>		–	–	58	
CLK to F <sub>n</sub> data output hold time	t <sub>OH3</sub>		15	–	–	ns
C0 to F <sub>n</sub> data output delay time	t <sub>PLH9</sub>	See figure 11. See note 1.	–	–	48	ns
	t <sub>PHL9</sub>		–	–	48	

Notes

1. Measurement circuit 1
2. Measurement circuit 2

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$\overline{\text{TAB}} = \text{LOW}$ ,  $\overline{\text{TF}} = \text{LOW}$

$V_{\text{DD}} = 4.75$  to  $5.25$  V,  $T_a = -20$  to  $70$  deg. C,  $V_{\text{SS}} = 0$  V

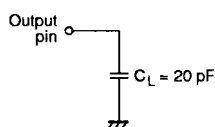
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
C0 to C16 carry output delay time	$t_{\text{PLH4}}$	See figure 8.	–	–	40	ns
	$t_{\text{PHL4}}$	See note 1.	–	–	40	
C0 to OVF overflow delay time	$t_{\text{PLH5}}$	See figure 10.	–	–	40	ns
	$t_{\text{PHL5}}$	See note 1.	–	–	40	
A and B to C16 carry output delay time	$t_{\text{PLH6}}$	See figure 8.	–	–	57	ns
	$t_{\text{PHL6}}$	See note 1.	–	–	57	
A and B to OVF overflow output delay time	$t_{\text{PLH7}}$	See figure 10.	–	–	63	ns
	$t_{\text{PHL7}}$	See note 1.	–	–	63	
C0 to $F_n$ data output delay time	$t_{\text{PLH9}}$	See figure 12.	–	–	48	ns
	$t_{\text{PHL9}}$	See note 1.	–	–	48	
A and B to $F_n$ data output delay time	$t_{\text{PLH10}}$	See figure 12.	–	–	60	ns
	$t_{\text{PHL10}}$	See note 1.	–	–	60	

### Notes

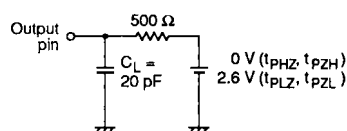
1. Measurement circuit 1
2. Measurement circuit 2

### Measurement Circuits

#### Measurement circuit 1



#### Measurement circuit 2



### Timing Diagrams

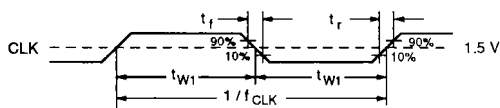


Figure 1. CLK input waveform

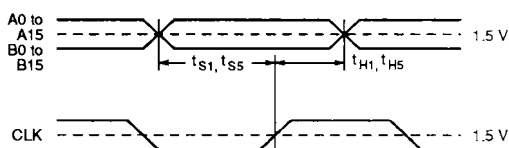


Figure 2. A and B data input timing

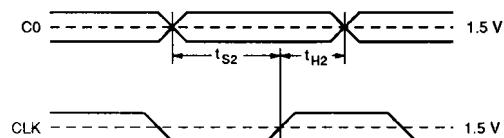


Figure 3. Carry input timing

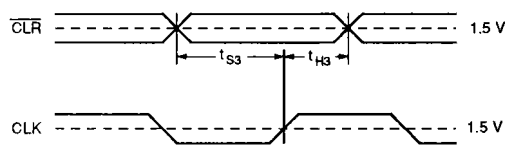


Figure 4. Clear input timing



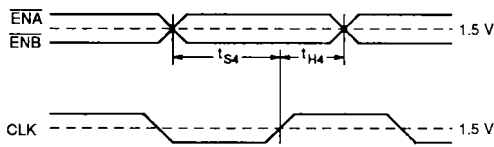


Figure 5. Enable input timing

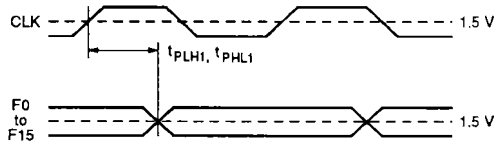


Figure 6. Output data timing ( $\overline{TF} = \text{HIGH}$ )

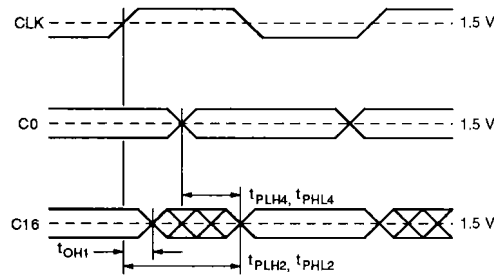


Figure 7. Carry output timing ( $\overline{TAB} = \text{HIGH}$ )

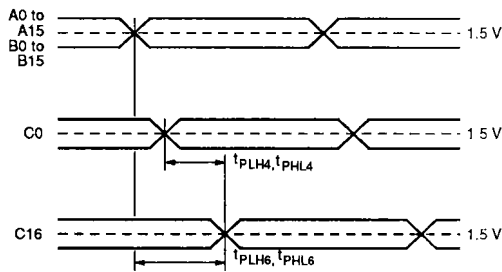


Figure 8. Carry output timing ( $\overline{TAB} = \text{LOW}$ )

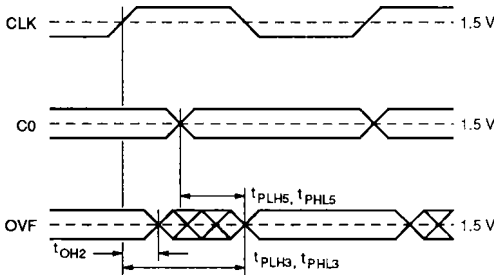


Figure 9. Overflow output timing ( $\overline{TAB} = \text{HIGH}$ )

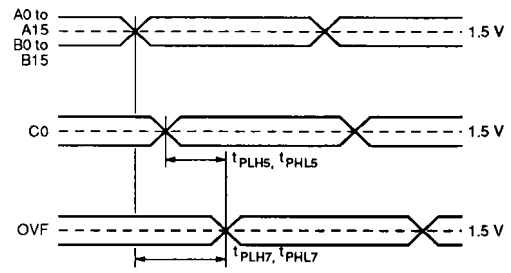


Figure 10. Overflow output timing ( $\overline{TAB} = \text{LOW}$ )

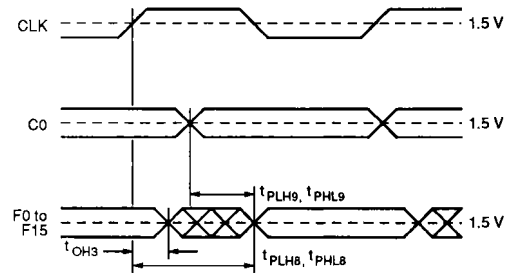


Figure 11. Output data timing ( $\overline{TAB} = \text{HIGH}$ ,  $\overline{TF} = \text{LOW}$ )

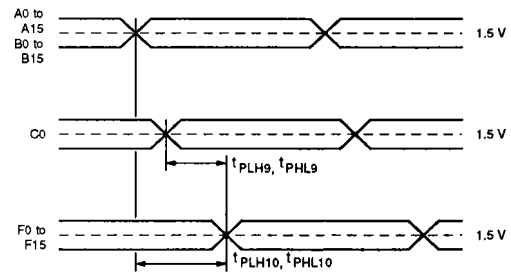


Figure 12. Output data timing ( $\overline{TAB} = \text{LOW}$ ,  $\overline{TF} = \text{LOW}$ )

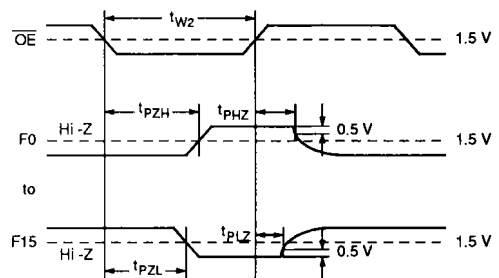


Figure 13. Output enable control timing

## FUNCTIONAL DESCRIPTION

### Operating Mode Selection (MOD0, MOD1, C0)

MOD0 and MOD1 select the operating mode as shown in the following table. These pins have internal pull-up resistances, and adder mode is selected if they are left open.

The C0 input on the LSB end needs to be switched to correspond to the selected operating mode. C0 must be LOW for adder mode, and HIGH for subtraction mode.

MOD0	MOD1	C0 (See note)	Operating mode
HIGH	HIGH	LOW	$A + B \rightarrow F$
HIGH	LOW	HIGH	$A - B \rightarrow F$
LOW	HIGH	HIGH	$-A + B \rightarrow F$
LOW	LOW	LOW	$A + F \rightarrow F$

#### Note

For cascade connections, this is the input level on C0 pin on the lowest device in the cascade (LSB end).

### Cascade Connection (C16, C0)

A 32-bit adder can be configured using two SM5833AFs by connecting the carry output C16 of the lower 16-bit adder to the carry input C0 of the upper 16-bit adder. Note that because the 32-bit adder operates as a ripple-carry adder, operating speed is reduced.

### Overflow Detect (OVF)

OVF goes HIGH when an arithmetic overflow is detected. It is driven directly from the CLA adder and is not latched. Note must be taken of the clock rate and OVF output delay when interfacing circuitry to this pin.

### Sign Extension (SE0, SE1)

Input data words shorter than 16 bits can be used by the SM5833AF by setting the SE0 and SE1 control pins as shown in the following table. Word lengths of 10, 12, 14 and 16 bits can be selected; the most-significant bit of the selected word length is sign-extended to 16 bits. Note that both inputs must have the same input word length.

SE0 and SE1 have internal pull-up resistances, so 16-bit input words are selected if they are left open.

SE0	SE1	MSB before sign extension		Input data length
		Input A	Input B	
LOW	LOW	A9	B9	10 bits
HIGH	LOW	A11	B11	12 bits
LOW	HIGH	A13	B13	14 bits
HIGH	HIGH	A15	B15	16 bits

### Register Control

#### Transparent mode ( $\overline{TAB}$ , $\overline{TF}$ )

Input registers A and B and output register F support a transparent mode of operation. Note that after selecting transparent mode, the previous register contents are corrupted.

$\overline{TAB}$	Input registers A and B
HIGH	Register mode
LOW	Transparent mode

$\overline{TF}$	Input register F
HIGH	Register mode
LOW	Transparent mode

#### Input register enable control ( $\overline{ENA}$ , $\overline{ENB}$ )

$\overline{ENA}$  and  $\overline{ENB}$  function as the latch clock enables for input registers A and B, respectively. Neither register can be updated while it is in the disabled state; they maintain the previously-latched data. Accordingly, these control signals allow data input to both registers from a single bus.

$\overline{ENA}$	Input register A
HIGH	Disable
LOW	Enable

$\overline{ENB}$	Input register B
HIGH	Disable
LOW	Enable

**Tristate output enable control ( $\overline{OE}$ )**

$\overline{OE}$  controls the output tristate buffers. This allows inputs and outputs to be connected to a single data bus.

$\overline{OE}$	Output operation
HIGH	High impedance
LOW	Output

**Output register clear ( $\overline{CLR}$ )**

Output register F is cleared by setting  $\overline{CLR}$  LOW. In accumulator mode, this function must be used to initialize the output register before starting an accumulation.

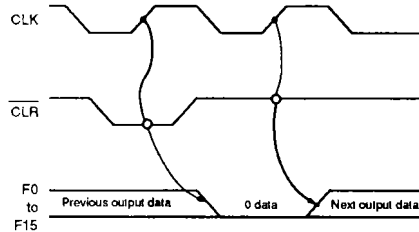



Figure 14. Clear operation timing

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