DUAL J-K FLIP-FLOP
(COMMON CLOCK)

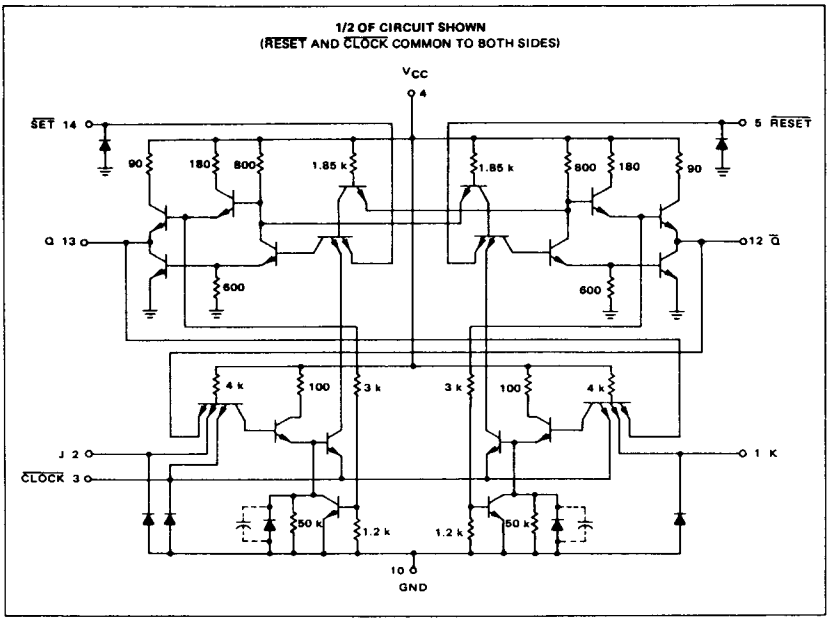
MC524 • MC574
MC424 • MC474

These devices are dual clocked flip-flops that trigger on the negative edge of the clock pulse and perform the J-K logic function. Each flip-flop in the package has one clocked J, one clocked K, and one direct $\overline{SET}$ input. A direct $\overline{RESET}$ and the $\overline{CLOCK}$ input are common to both flip-flops. Both Q and $\overline{Q}$ outputs are available on each flip-flop.

Information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is transferred into a temporary memory when the clock goes to the high state. When the clock returns low, the information is transferred to the bistable section and the Q and $\overline{Q}$ outputs. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

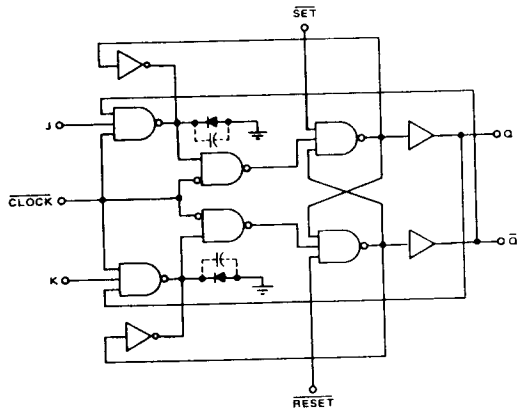
Since these flip-flops are charge-storage devices, there is a restriction on the clock fall time that must be observed.

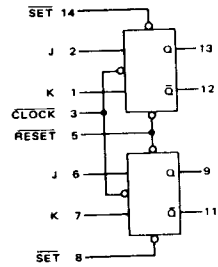
TYPE NO.	INPUT LOADING FACTOR				(I_F)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	$\overline{CLOCK}$	$\overline{SET}$	$\overline{RESET}$	J, K	$\overline{CLOCK}$	$\overline{SET}$	$\overline{RESET}$	J, K		
MC524 MC574	3.0	1.8	3.6	1.0	(−2.66 mA)	(−2.4 mA)	(−4.8 mA)	(−1.33 mA)	16 MC500 series Gates (22.0 mA) 8 MC500 series Gates (12.0 mA)	−55°C to +125°C
MC424 MC474	3.0	1.7	3.4	1.0	(−3.32 mA)	(−2.8 mA)	(−5.6 mA)	(−1.66 mA)	13 MC400 series Gates (22.5 mA) 7 MC400 series Gates (12.5 mA)	0°C to +75°C



559

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN





t_n		t_{n+1}	
J	K	Q	Q̄
0	0	Q_n	$\bar{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_n$	Q_n

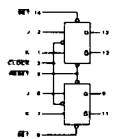
Total Power Dissipation = 110 mW typ/pkg
Switching Times
t_{pd-} = 12 ns typ
t_{pd+} = 10 ns typ
Operating Frequency = 45 MHz typ

560

560

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES														
		mA							Volts							
		I_{OL}		I_{OH}												
		P.*	Std	P.*	Std	I_{in}	$2I_{in}$	$4I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}
MC524*, MC574	−55°C	22	12	-2.2	-1.2	1.0	2.0	4.0	0.45	2.8	4.5	2.0	0.9	5.5	5.0
	+25°C	22	12	-2.2	-1.2	1.0	2.0	4.0	0.45	2.8	4.5	1.8	1.1	5.5	5.0
	+125°C	22	12	-2.2	-1.2	1.0	2.0	4.0	0.45	2.8	4.5	1.5	0.9	5.5	5.0
MC424*, MC474	0°C	22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.0	5.5	5.0
	+25°C	22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.1	5.5	5.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.0	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC524, MC574 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC424, MC474 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	$4I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	Gnd
Input																											
Forward Current J	I_F	2	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	-	1,3,14	-	-	-	4	2,5,6,7,10
K		1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66		-	-	-	-	-	-	-	2,3,5	-	-	-		1,6,7,10,14
Set		14	-	-2.4	-	-2.4	-	-2.4	-	-2.8	-	-2.8	-	-2.8		-	-	-	-	-	-	-	1,2,3,5	-	-	-		6,7,10,14
Reset		5	-	-4.8	-	-4.8	-	-4.8	-	-5.6	-	-5.6	-	-5.6		-	-	-	-	-	-	-	1,2,3,14	-	-	-		5,6,7,10
Clock		3	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32		-	-	-	-	-	3	-	1,2,5,6, 7,8,14	-	-	-		10
Leakage Current J	I_R	2	-	70	-	70	-	70	-	70	-	70	-	70	μAdc	-	-	-	-	-	-	-	2	-	-	-	4	3,10,14†
K		1	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	-	-	-	1	-	-	-		3,5†,10
Set		14	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	-	-	-	14†	-	-	-		3,10
Reset		5	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	-	5†	-	-	-		3,10
Clock		3	-	280	-	280	-	280	-	280	-	280	-	280		-	-	-	-	-	-	-	3	-	-	-	↓	1,2,6,7,10
Inverse Beta Current J	I_L	2	-	70	-	70	-	70	-	70	-	70	-	70	μAdc	-	-	-	-	-	-	-	2	-	-	-	4	5,6,7,10
K		1	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	-	-	-	1	-	-	-		6,7,10,14
Set		14	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	-	-	-	14	-	-	-		5,6,7,10
Reset		5	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	-	5	-	-	-		8,10,14
Clock		3	-	280	-	280	-	280	-	280	-	280	-	280		-	-	-	-	-	-	-	3	-	-	-		10,14
		3	-	280	-	280	-	280	-	280	-	280	-	280		-	-	-	-	-	-	-	3	-	-	-	↓	5,10
Breakdown Voltage J	BV_{in}"0"	2	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	2	-	-	-	-	-	-	-	-	4	5,6,7,10
K		1	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-		-	-	1	-	-	-	-	-	-	-	-		6,7,10,14
Set		14		-		-		-		-		-		-		-	-	14	-	-	-	-	-	-	-	-		5,6,7,10
Reset		5		-		-		-		-		-		-		-	-	-	5	-	-	-	-	-	-	-		8,10,14
Clock		3		-		-		-		-		-		-		-	-	-	-	3	-	-	-	-	-	-		10,14
		3		-		-		-		-		-		-		-	-	-	-	3	-	-	-	-	-	-	↓	5,10
	BV_{in}"1"	2	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	2	-	-	-	-	-	-	-	-	4	3,10,14†
K		1	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-		-	-	1	-	-	-	-	-	-	-	-		3,5†10
Set		14		-		-		-		-		-		-		-	-	14†	-	-	-	-	-	-	-	-		3,10
Reset		5		-		-		-		-		-		-		-	-	-	5†	-	-	-	-	-	-	-		3,10
Clock		3		-		-		-		-		-		-		-	-	-	-	3	-	-	-	-	-	-	↓	1,2,6,7,10

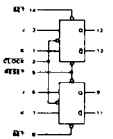
*Prime Fan-Out

†Momentarily ground pin prior to taking measurement to set flip-flop in desired state, then release or set to the indicated voltage prior to taking measurement.

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES														
		mA							Volts							
		I_{OL}		I_{OH}		I_{in}	$2I_{in}$	$4I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}
		P.*	Std	P.*	Std										
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Output																												
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	5	-	-	4	3,8,10,14
		13	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	13	-	-	-	-	-	-	-	14	-	-	4	3,5,10
	V_{out} "1"	12	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	-	-	5	-	4	3,10,14
		13	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	13	-	-	-	-	-	-	-	14	-	4	3,5,10
Leakage Current	I_{OLK}	12	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	-	-	-	-	-	-	-	6,14	-	-	12	4	1,2,3,5,6,7,10,
		13	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	-	-	-	-	-	-	-	5,8	-	-	13	4	1,2,3,6,7,10,14
Short-Circuit Current	I_{SC}	12	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mAdc	-	-	-	-	-	-	-	6,14	-	-	-	4	1,2,3,5,6,7,10,12
		13	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mAdc	-	-	-	-	-	-	-	5,8	-	-	-	4	1,2,3,6,7,10,13,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	-	-	5	-	-	-	-	4	3,10,14
		13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	-	-	14	-	-	-	-	4	3,5,10
	V_{OH}	12	2.8	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	Vdc	-	12	-	-	-	5	-	-	-	-	-	4	3,10,14
		13	2.8	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	Vdc	-	13	-	-	-	14	-	-	-	-	-	4	3,5,10
Power Requirements (Total Device)																												
Power Supply Drain	I_{PD}	4	-	-	-	28	-	-	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	3,8,10,14
	I_{PD}	4	-	-	-	28	-	-	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	3,5,10

*Prime Fan-Out

†Momentarily ground pin prior to taking measurement to set flip-flop in desired state, then release or set to the indicated voltage prior to taking measurement

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 12 ns.

Provides direct $\overline{SET}$ and $\overline{RESET}$ inputs. The application of a "0" state to the $\overline{SET}$ will cause Q to go to the "1" state; application of a "0" state to the $\overline{RESET}$ will cause both $\bar{Q}$ pins to go to the "1" state. The $\overline{SET}$ or $\overline{RESET}$ can be applied 20 ns after the clock has changed to the low state. It should not be applied when the clock is in the high state.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 1.0 μs to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop typically requires 10 ns to recognize a "0" state to a "1" state change.

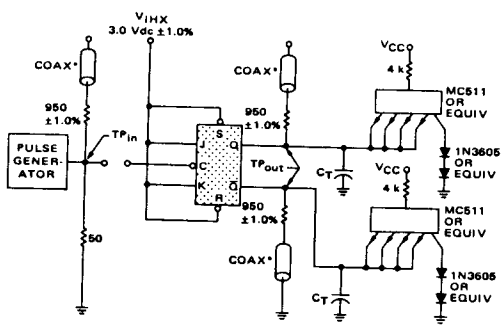
Negative edge triggering - When the clock changes from the high state to the low state, the information in the temporary storage section is transferred to the bistable network and the Q and $\bar{Q}$ outputs. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to a voltage between 2.0 and 5.0 Vdc. Unused $\overline{SET}$ or $\overline{RESET}$ inputs must be tied to a voltage between 2.0 and 5.0 Vdc.

The maximum allowable skew time for these devices is 9.0 ns. This is the total of the minimum propagation delay (5.0 ns) and the minimum time to recognize a "0" to "1" state information change (4.0 ns).

Operating frequency of the flip-flops is not significantly affected by capacitive loading due to the buffered outputs.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

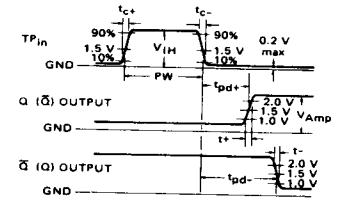
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	X	–	20	ns
Delay Time On	t_{pd-}	X	–	20	ns
Rise Time	t_{+}	X	–	4.0	ns
Fall Time	t_{-}	X	–	2.5	ns
Amplitude	V_{Amp}	X	3.0	–	Volt

WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	35 MHz max	W
Pulse Width	PW	12 ns min	X
Input High Voltage	V_{IH}	2.4 V min	Y
Fall Time	t_{c-}	100 ns max	Z

VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	W	X	Y	Z	UNIT
PRF	35	5.0	5.0	1.0	MHz
PW	12	12	15	200	ns
t_{c+}	≤ 2.0	≤ 2.0	≤ 5.0	≤ 50	ns
t_{c-}	≤ 2.0	≤ 2.0	≤ 5.0	100	ns
V_{IH}	3.0	3.0	2.4	3.0	Volt

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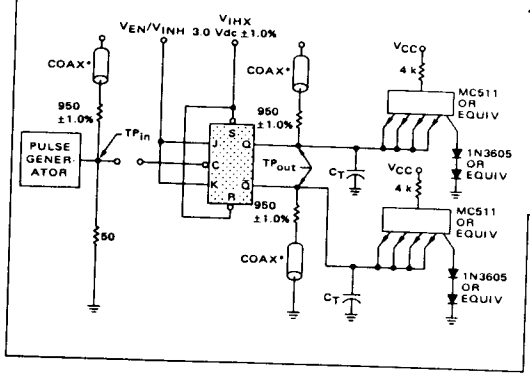
FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT 070 50 or equivalent.

C_T = 15 pF ± total parasitic capacitance, which includes probe, wiring, and load capacitances.

Enable Mode Test:
The device under test shall toggle when V_{EN} = 1.8 Vdc ± 1.0% is applied.

Inhibit Mode Test:
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ± 1.0% is applied.

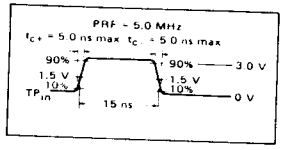
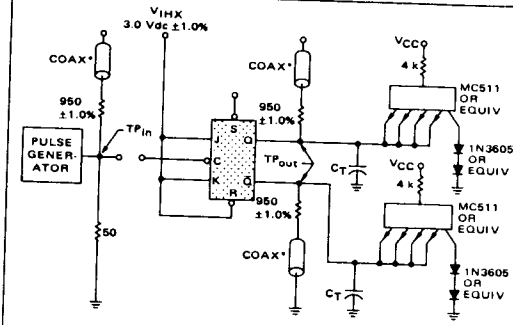


FIGURE 3 – SET-RESET TERMINAL CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT 070 50 or equivalent.

C_T = 15 pF ± total parasitic capacitance, which includes probe, wiring, and load capacitances.

Two pulse generators are required and must be slaved together to provide the waveforms shown.

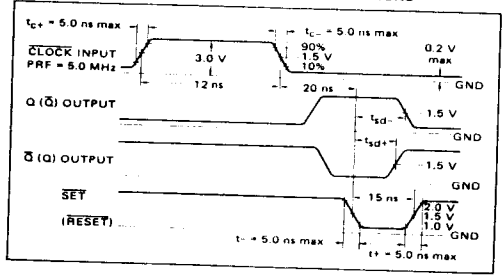
TEST PARAMETERS

SYMBOL	VALUE	UNIT
t_{sd-}	20	ns max
t_{sd+}	20	ns max

NOTE:

Connections shown for measuring times related to $\overline{SET}$ terminal only. To measure times at $\overline{RESET}$ terminals, apply the input pulse to Pin 13.

VOLTAGE WAVEFORMS AND DEFINITIONS



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