



## N-Channel 12-V (D-S) MOSFET

### PRODUCT SUMMARY

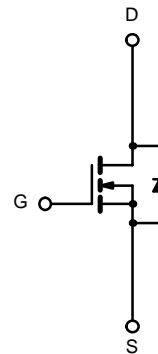
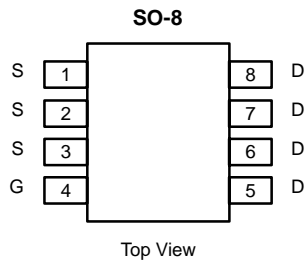
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
12	0.003 @ $V_{GS} = 4.5$ V	25
	0.004 @ $V_{GS} = 2.5$ V	22
	0.005 @ $V_{GS} = 1.8$ V	19

### FEATURES

- TrenchFET® Power MOSFET
- PWM Optimized
- 100%  $R_G$  Tested

### APPLICATIONS

- Low Voltage Synchronous Rectification
- Low Voltage LDO Pass Transistor



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		$V_{DS}$	12		V
Gate-Source Voltage		$V_{GS}$	$\pm 8$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	25	17	A
	$T_A = 70^\circ\text{C}$		20	13	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)		$I_{DM}$	60		
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	2.9	1.3	
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	3.5	1.6	W
	$T_A = 70^\circ\text{C}$		2.2	1	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$	29	35	$^\circ\text{C/W}$
	Steady State		67	80	
Maximum Junction-to-Foot (Drain)	Steady State		$R_{thJF}$	13	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

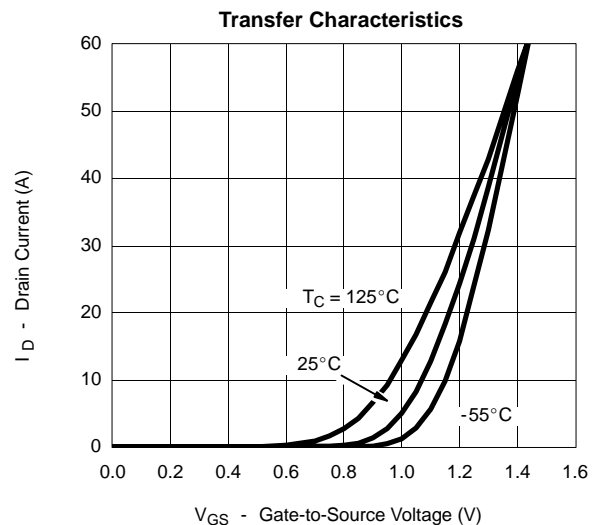
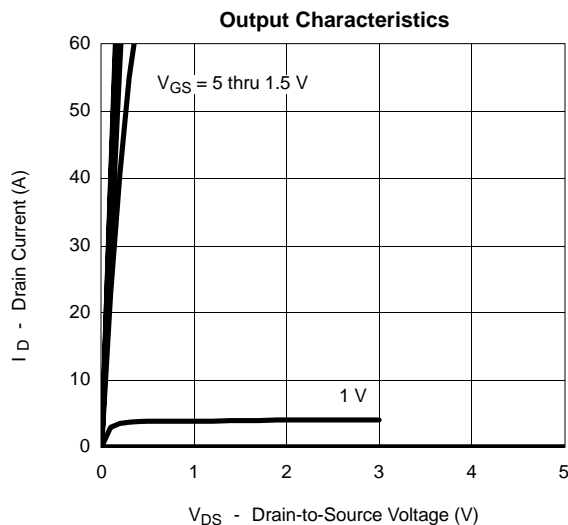


SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.40			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 9.6 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 9.6 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A		0.0025	0.003	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 22 A		0.0031	0.004	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 19 A		0.004	0.005	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 6 V, I <sub>D</sub> = 25 A		80		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.9 A, V <sub>GS</sub> = 0 V		0.56	1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A		51	75	nC
Gate-Source Charge	Q <sub>gs</sub>			6.6		
Gate-Drain Charge	Q <sub>gd</sub>			9.1		
Gate Resistance	R <sub>G</sub>		1.0	1.6	2.7	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 6 V, R <sub>L</sub> = 6 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		35	55	ns
Rise Time	t <sub>r</sub>			41	65	
Turn-Off Delay Time	t <sub>d(off)</sub>			190	290	
Fall Time	t <sub>f</sub>			115	175	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.9 A, di/dt = 100 A/μs		60	90	

## Notes

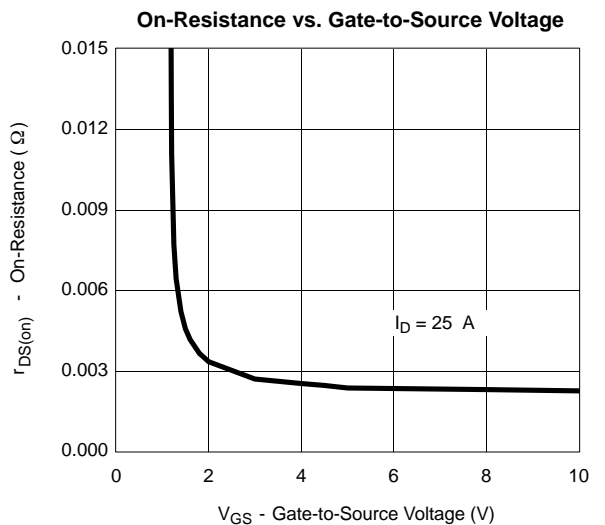
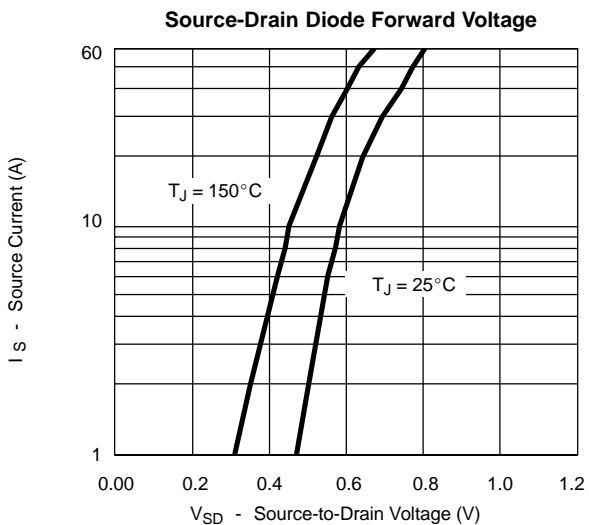
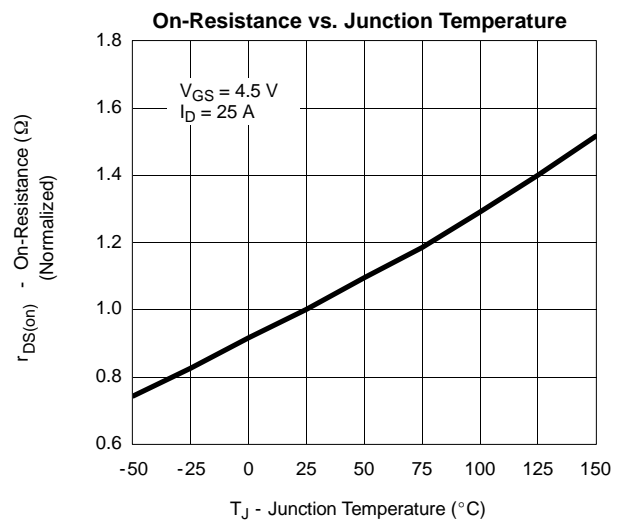
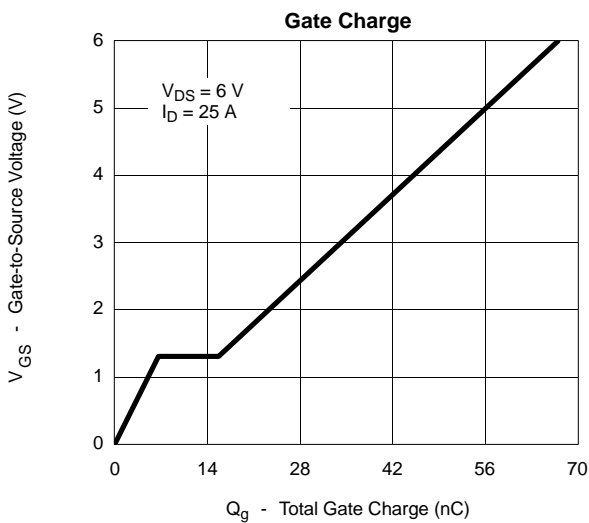
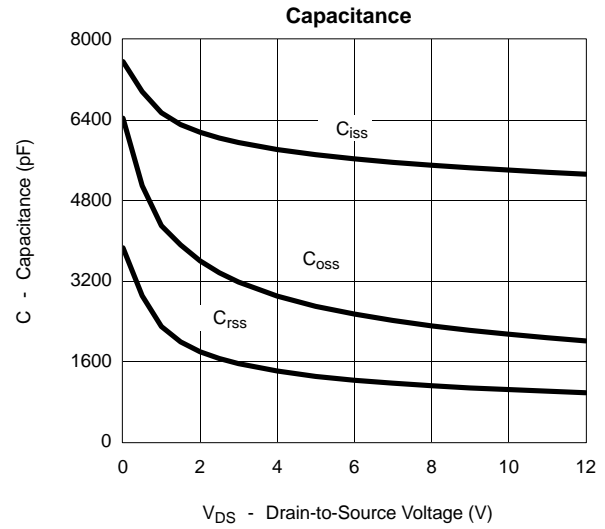
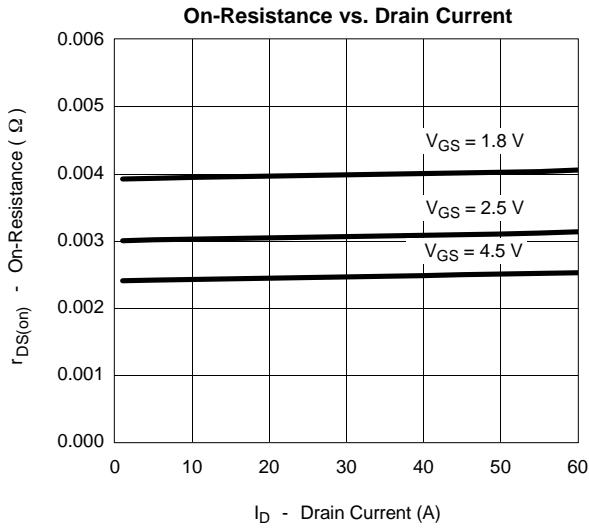
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
 b. Guaranteed by design, not subject to production testing.

## TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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