Description

The GM71V(S)17403B/BL is the new generation dynamic RAM organized 4,194,304 words x 4 bit. GM71V(S)17403B/BL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)17403B/BL offers Extended Data Out (EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)17403B/BL to be packaged in a standard 300 mil 24(26) pin SOJ and standard 300mil 24(26)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 3.3V ± 0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 4,194,304 Words x 4 Bit Organization
- Extended Data Out Mode Capability
- Single Power Supply (3.3V ± 0.3V)
- Fast Access Time & Cycle Time

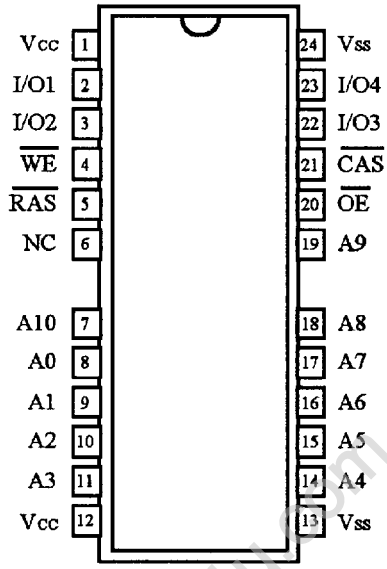
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71V(S)17403B/BL-6	60	15	104	25
GM71V(S)17403B/BL-7	70	18	124	30
GM71V(S)17403B/BL-8	80	20	144	35

- Low Power
  Active : 369/360/324mW (MAX)
  Standby : 7.2mW (CMOS level : MAX)
  0.36mW (L-version : MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 2048 Refresh Cycles/32ms
- 2048 Refresh Cycles/128ms (L-version)
- Self Refresh Operation (L-version)
- Battery Back Up Operation (L-version)
- Test function : 16bit parallel test mode

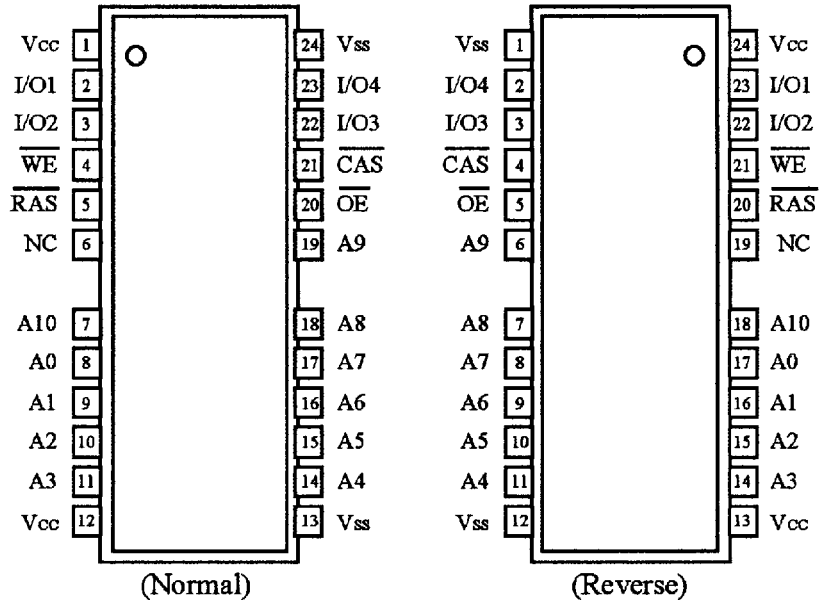
Pin Configuration

24 (26) SOJ



(Top View)

24 (26) TSOP II



(Normal) (Reverse)

(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A10	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A10	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input / Data Output	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe	Vss	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)17403BJ/BLJ-6 GM71V(S)17403BJ/BLJ-7 GM71V(S)17403BJ/BLJ-8	60ns 70ns 80ns	300 Mil 24 (26) Pin Plastic SOJ
GM71V(S)17403BT/BLT-6 GM71V(S)17403BT/BLT-7 GM71V(S)17403BT/BLT-8	60ns 70ns 80ns	300 Mil 24 (26) Pin Plastic TSOP II (Normal Type)
GM71V(S)17403BR/BLR-6 GM71V(S)17403BR/BLR-7 GM71V(S)17403BR/BLR-8	60ns 70ns 80ns	300 Mil 24 (26) Pin Plastic TSOP II (Reverse Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-0.5 ~ Vcc+0.5 (≤4.6V(MAX))	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-0.5 ~ 4.6	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

DC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, T_A = 0 ~ 70℃)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.0	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	60ns	-	110	mA	1, 2
		70ns	-	100		
		80ns	-	90		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode (t_{RC} = t_{RC} min)	60ns	-	110	mA	2
		70ns	-	100		
		80ns	-	90		
I_{CC4}	Extended Data Out Mode Current Average Power Supply Current EDO Page Mode (t_{HPC} = t_{HPC} min)	60ns	-	110	mA	1, 3
		70ns	-	100		
		80ns	-	90		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} - 0.2V, D_{OUT} = High-Z)		-	1	mA	
			-	100	μA	5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	110	mA	
		70ns	-	100		
		80ns	-	90		
I_{CC7}	Battery Back Up Operating Current (Standby with CBR Refresh) (t_{RC}=62.5μs, t_{RAS}≤0.3μs, D_{OUT}=High-Z)		-	300	μA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{CAS}$≤0.2V, D_{OUT}=High-Z)		-	200	μA	5
$I_{I(L)}$	Input Leakage Current Any Input (0V≤V_{IN}≤7V)		-10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V≤V_{OUT}≤7V)		-10	10	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $\overline{CAS}$ = L (≤0.2V) while $\overline{RAS}$ = L (≤0.2V)
5. L-version

Capacitance (V_{CC} = 3.3V ± 0.3V, T_A = 25℃)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 3.3V ± 0.3V, T_A = 0 ~ 70℃, Notes 1, 2, 18)

Test Conditions
Input rise and fall times: 2ns
Input levels: V_{IL}= 0V, V_{IH}=3V
Input timing reference levels: 0.8V, 2.4V
Output timing reference levels: 0.8V, 2.0V
Output load : 1 TTL gate + C_L (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	144	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	13	-	15	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	21
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	13	10,000	15	10,000	ns	22
t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	13	-	15	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	20	60	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	48	-	58	-	68	-	ns	24
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Set-up Time from D_{IN}	0	-	0	-	0	-	ns	6
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	7
t_{REF}	Refresh Period	-	32	-	32	-	32	ms	
	Refresh Period (L-version)	-	128	-	128	-	128	ms	

Read Cycle

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	8.9.19
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	9,10, 17,19
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,11, 17,19
t_{OAC}	Access Time from $\overline{OE}$	-	15	-	18	-	20	ns	9,19
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	12
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	0	-	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	18	-	23	-	28	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in low-Z	0	-	0	-	0	-	ns	
t_{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	3	-	3	-	3	-	ns	
t_{OEZ}	Output Buffer Turn-off Time to $\overline{OE}$	-	15	-	15	-	15	ns	13
t_{OFF}	Output Buffer Turn-off Time	-	15	-	15	-	15	ns	13,23
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	5
t_{OHR}	Output Data Hold Time from $\overline{RAS}$	3	-	3	-	3	-	ns	
t_{OFR}	Output Buffer Turn-off Time to $\overline{RAS}$	-	15	-	15	-	15	ns	13,23
t_{WEZ}	Output Buffer Turn-off to $\overline{WE}$	-	15	-	15	-	15	ns	13
t_{WDD}	$\overline{WE}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	
t_{RDD}	$\overline{RAS}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	

Write Cycle

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	14
t_{WCH}	Write Command Hold Time	10	-	13	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	15
t_{DH}	Data-in Hold Time	10	-	15	-	15	-	ns	15

Read- Modify-Write Cycle

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	149	-	175	-	199	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	82	-	95	-	107	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	37	-	43	-	47	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	52	-	60	-	67	-	ns	14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	-	18	-	20	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	-	0	-	0	-	ns	
t_{WRP}	$\overline{WE}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	0	-	0	-	0	-	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	

EDO Mode Cycle

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPC}	EDO Mode Cycle Time	25	-	30	-	35	-	ns	20
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	9,17,19
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{DOH}	Output Data Hold Time from $\overline{CAS}$ Low	3	-	3	-	3	-	ns	9,17
t_{COL}	$\overline{CAS}$ Hold Time Referred $\overline{OE}$	10	-	13	-	15	-	ns	
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ Setup time	5	-	5	-	5	-	ns	
t_{RCHP}	Read command hold time from $\overline{CAS}$ precharge	35	-	40	-	45	-	ns	

EDO Read-Modify-Write Cycle

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPRWC}	EDO Mode Read-Modify-Write Cycle Time	79	-	90	-	99	-	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	54	-	62	-	69	-	ns	14

Test Mode Cycle *19

Symbol	Parameter	GM71V(S)17403 B/BL-6		GM71V(S)17403 B/BL-7		GM71V(S)17403 B/BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WTS}	Test Mode $\overline{WE}$ Setup Time	0	-	0	-	0	-	ns	
t_{WTH}	Test Mode $\overline{WE}$ Hold Time	10	-	10	-	10	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time in Counter Test Cycle	20	-	30	-	30	-	ns	

Self Refresh Mode (L-Version)

Symbol	Parameter	GM71VS17403 BL-6		GM71VS17403 BL-7		GM71VS17403 BL-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width (Self-Refresh)	100	-	100	-	100	-	us	
t_{RPS}	$\overline{RAS}$ Precharge Time (Self-Refresh)	110	-	130	-	150	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time (Self-Refresh)	-50	-	-50	-	-50	-	ns	

Notes:

1. AC Measurements assume $t_T = 2ns$.
2. An initial pause of 200μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
8. Assume that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100pF.
10. Assume that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
11. Assume that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF}(max) and t_{OEZ}(max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), the $t_{CWD} \geq t_{CWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), or $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPW} \geq t_{CPW}$(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO Mode cycles.
17. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}

18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each I/O.

19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M x 4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O. If 4 bits of each I/O are equal (all 1s or 0s), data output pin is high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.

20. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

21. $t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T$ in Read - Modify - Write cycle.

22. $t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T$ in Read - Modify - Write cycle.

23. t_{OFF} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.

24. $t_{CSH}(min)$ can be achieved when $t_{RCD} \leq t_{CSH}(min) - t_{CAS}(min)$.

25. EDO Hi-Z control by $\overline{OE}$ or $\overline{WE}$. $\overline{OE}$ rising edge disables data outputs. When $\overline{OE}$ goes high during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access. When $\overline{WE}$ goes low during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access.

26. $t_{HPC}(min)$ can be achieved during a series of EDO mode write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode $\overline{RAS}$ cycle(EDO mode mix cycle (1),(2)) minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified $t_{HPC}(min)$ value.The value of $\overline{CAS}$ cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).

Timing Waveforms

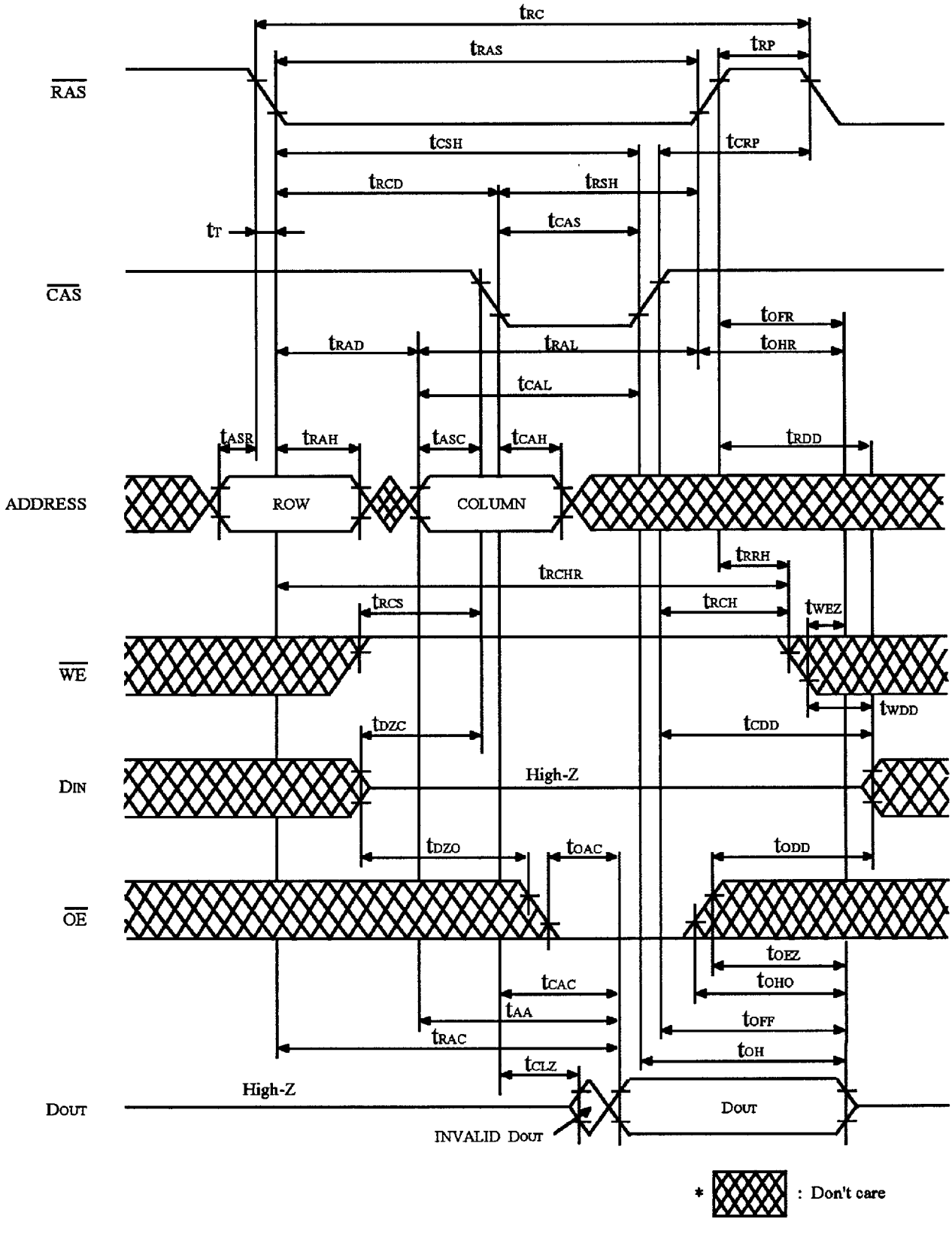


FIGURE 1. READ CYCLE

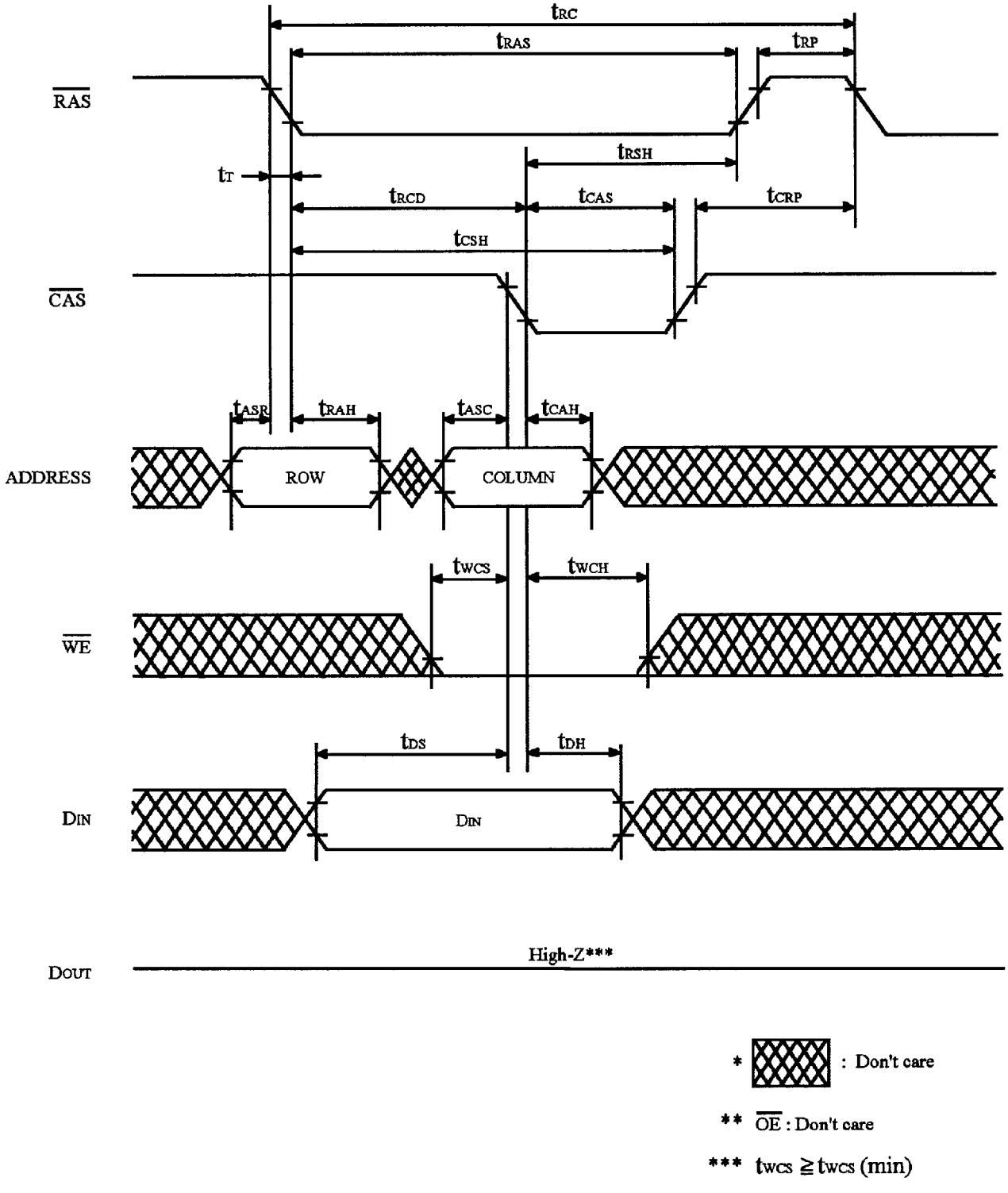


FIGURE 2. EARLY WRITE CYCLE

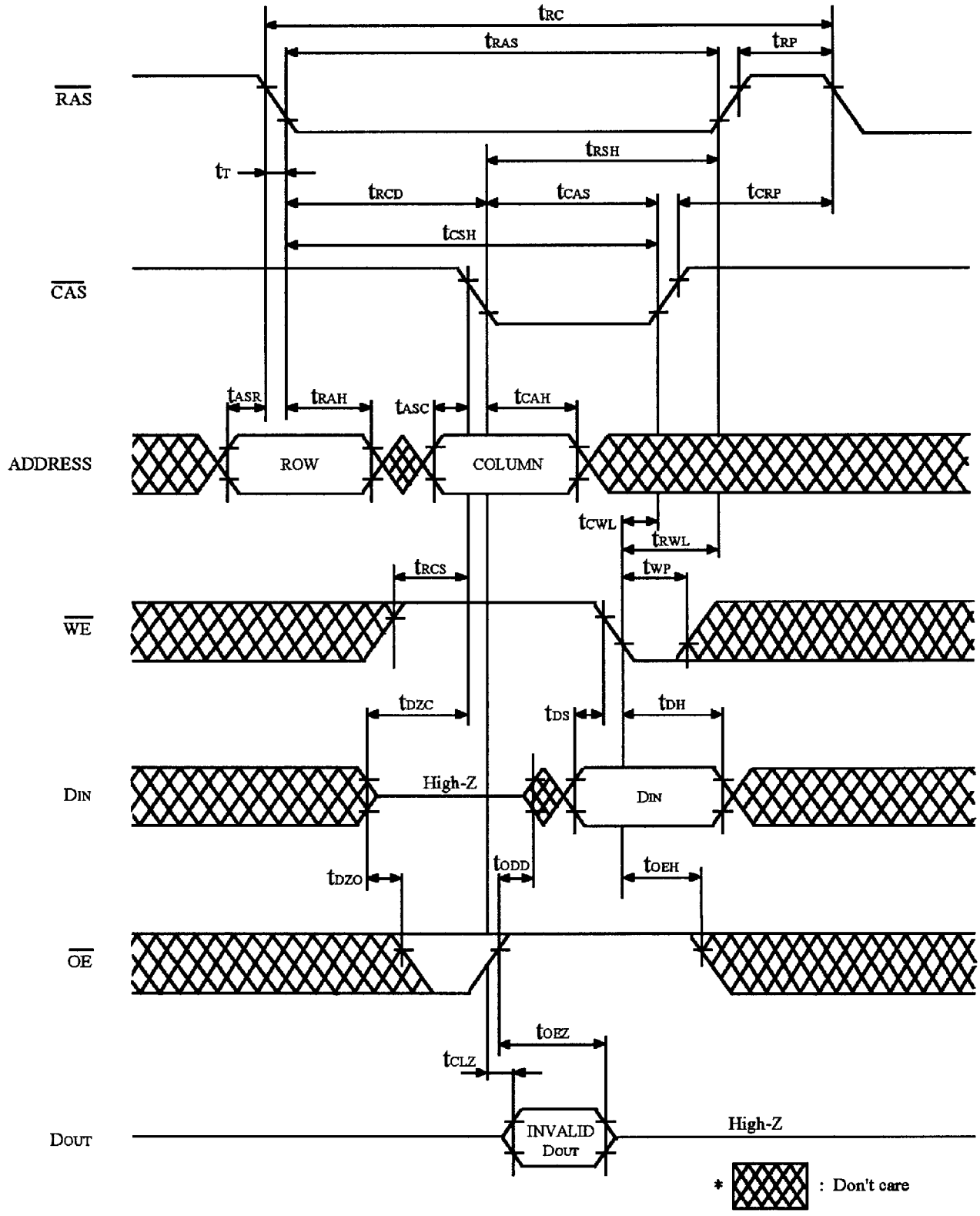


FIGURE 3. DELAYED WRITE CYCLE *18

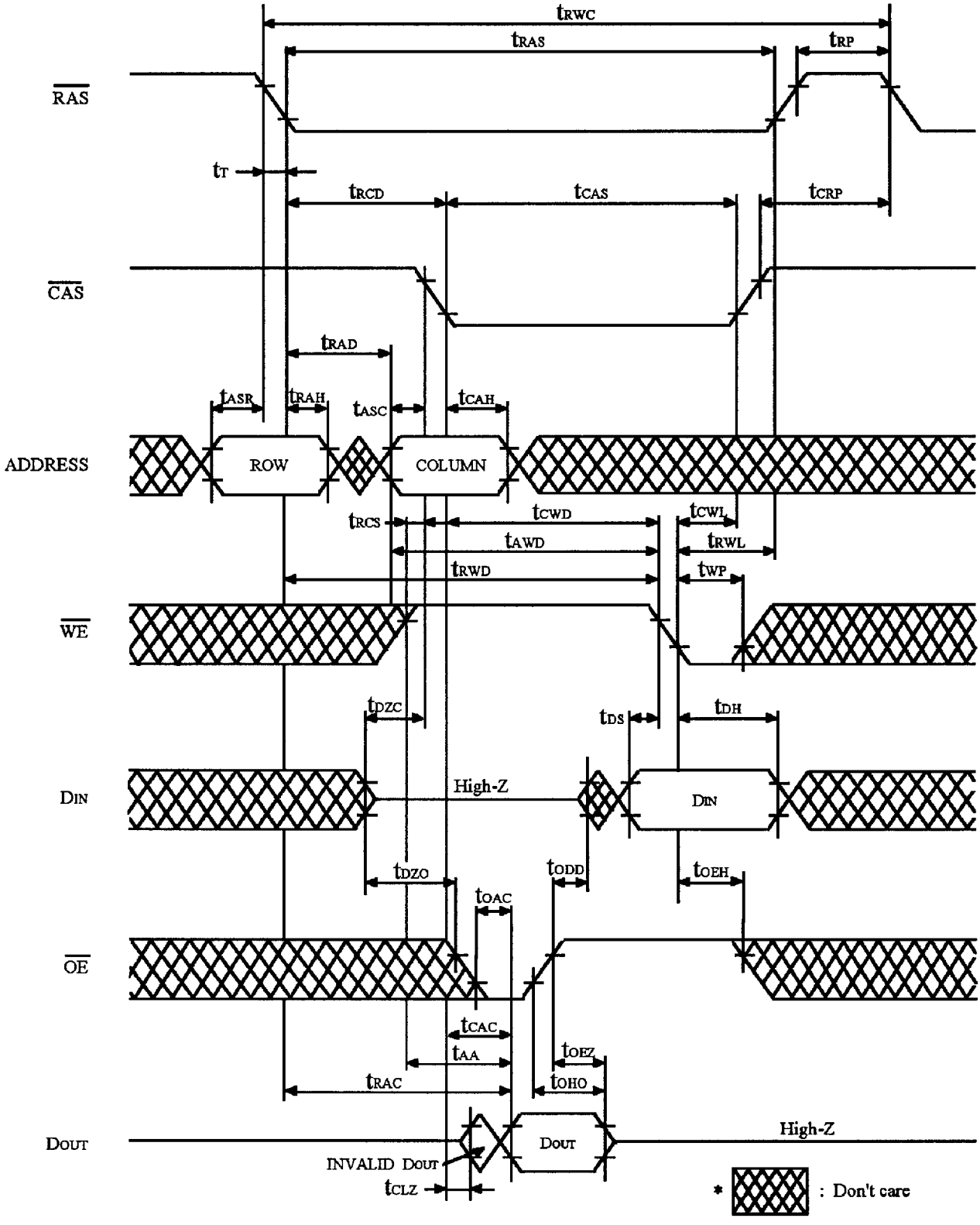
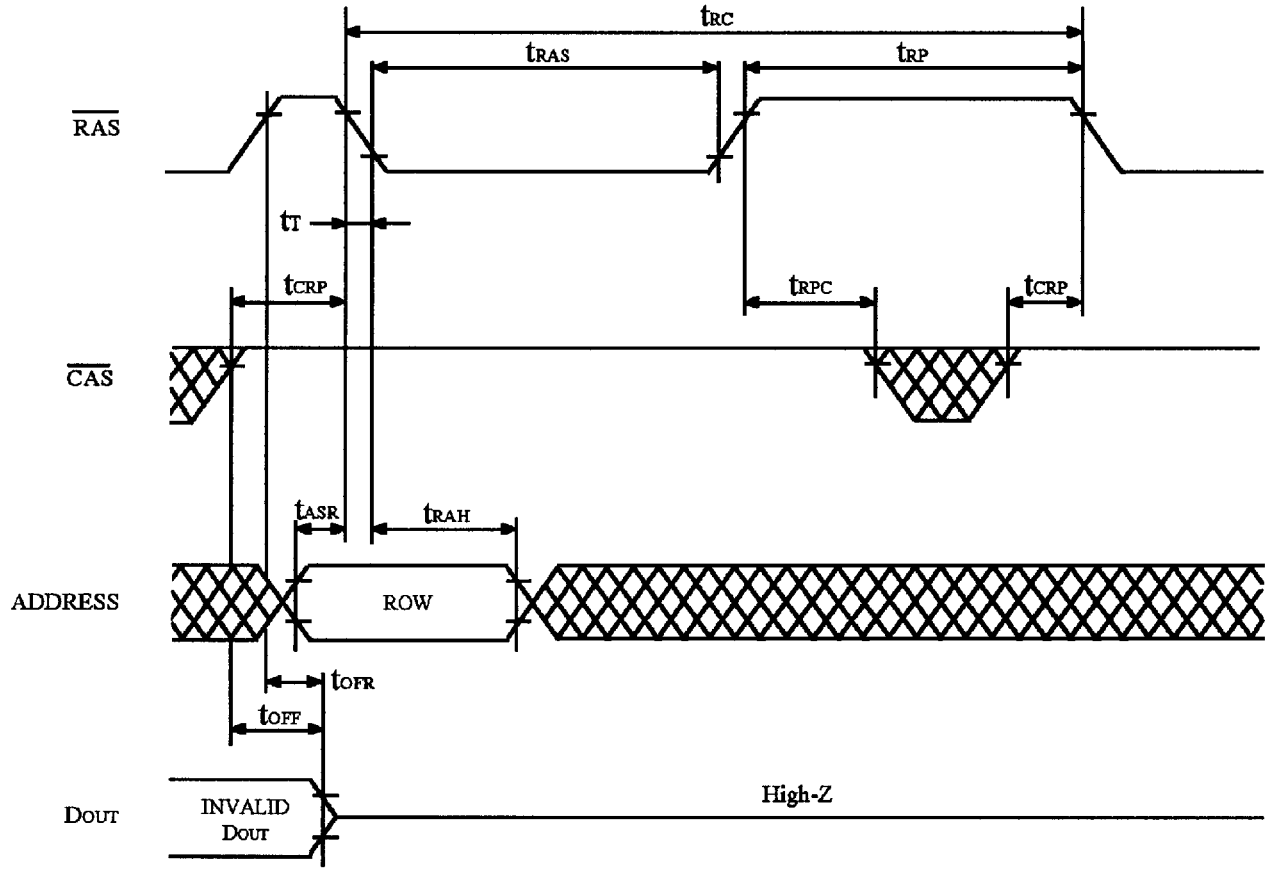


FIGURE 4. READ MODIFY WRITE CYCLE *18



* : Don't care

** $\overline{OE}$, $\overline{WE}$: Don't care

*** Refresh Address: A0-A10 (RA0-RA10)

FIGURE 5. $\overline{RAS}$ ONLY REFRESH CYCLE

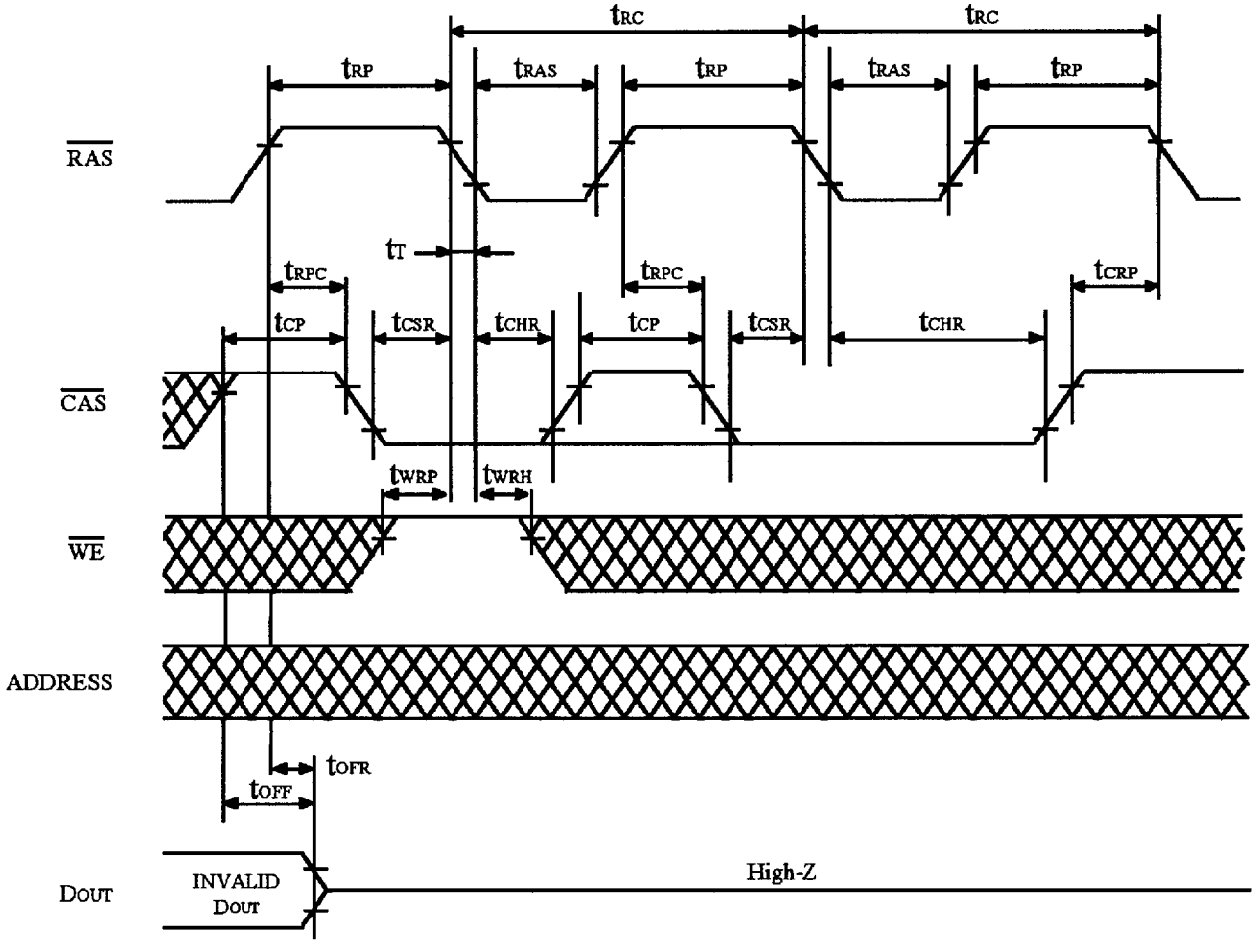


FIGURE 6. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

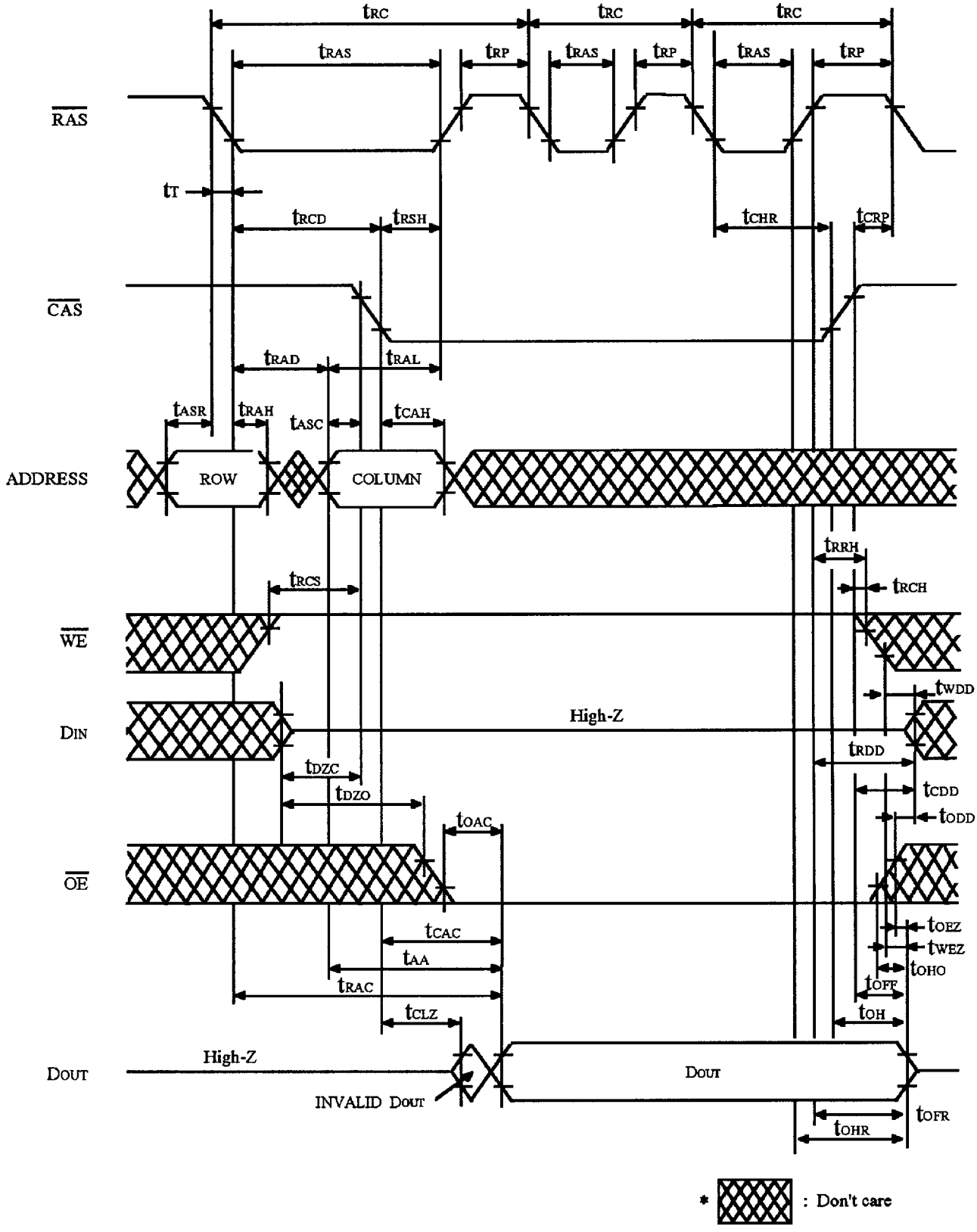


FIGURE 7. HIDDEN REFRESH CYCLE

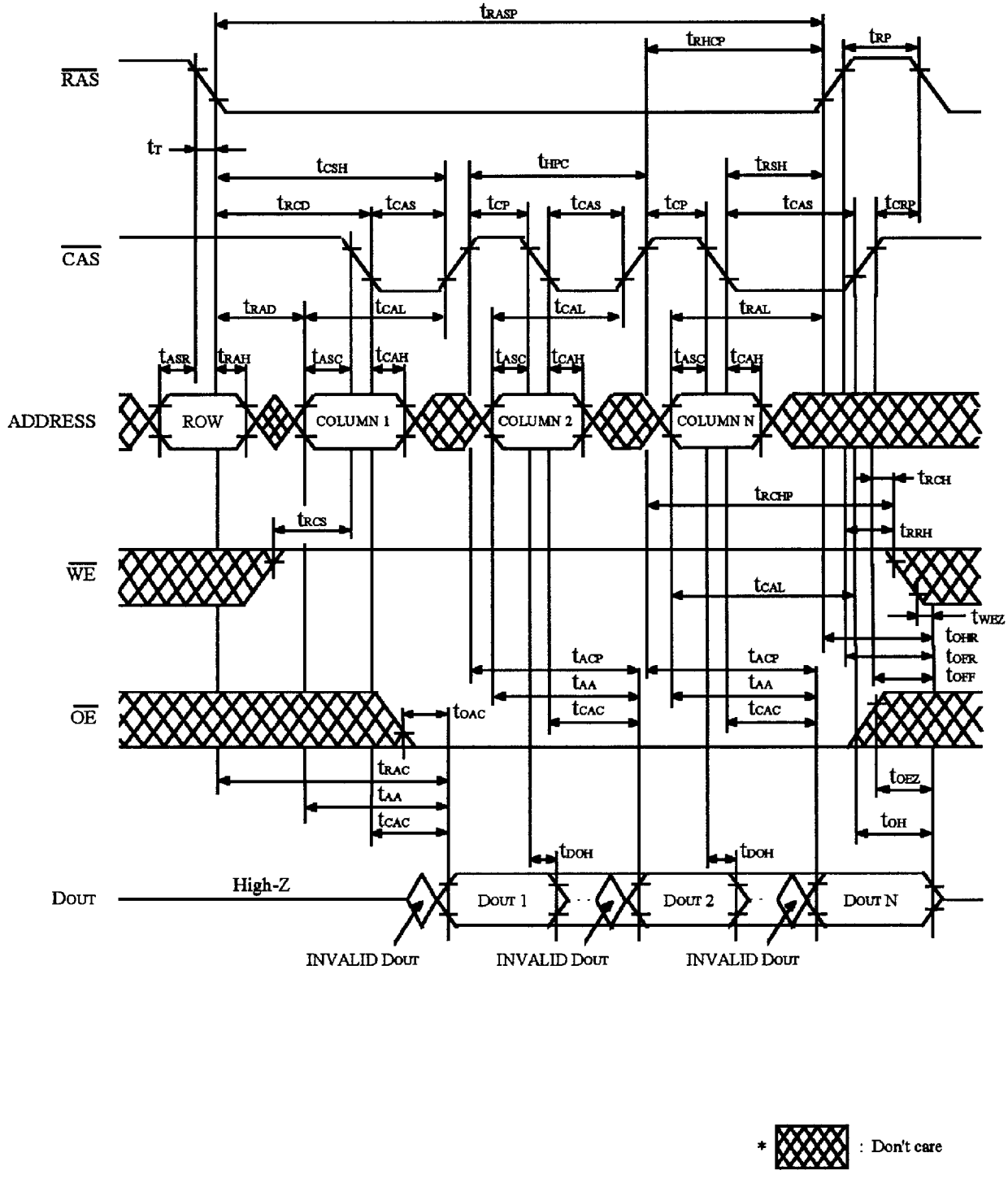


FIGURE 8. EXTENDED DATA OUT MODE READ CYCLE

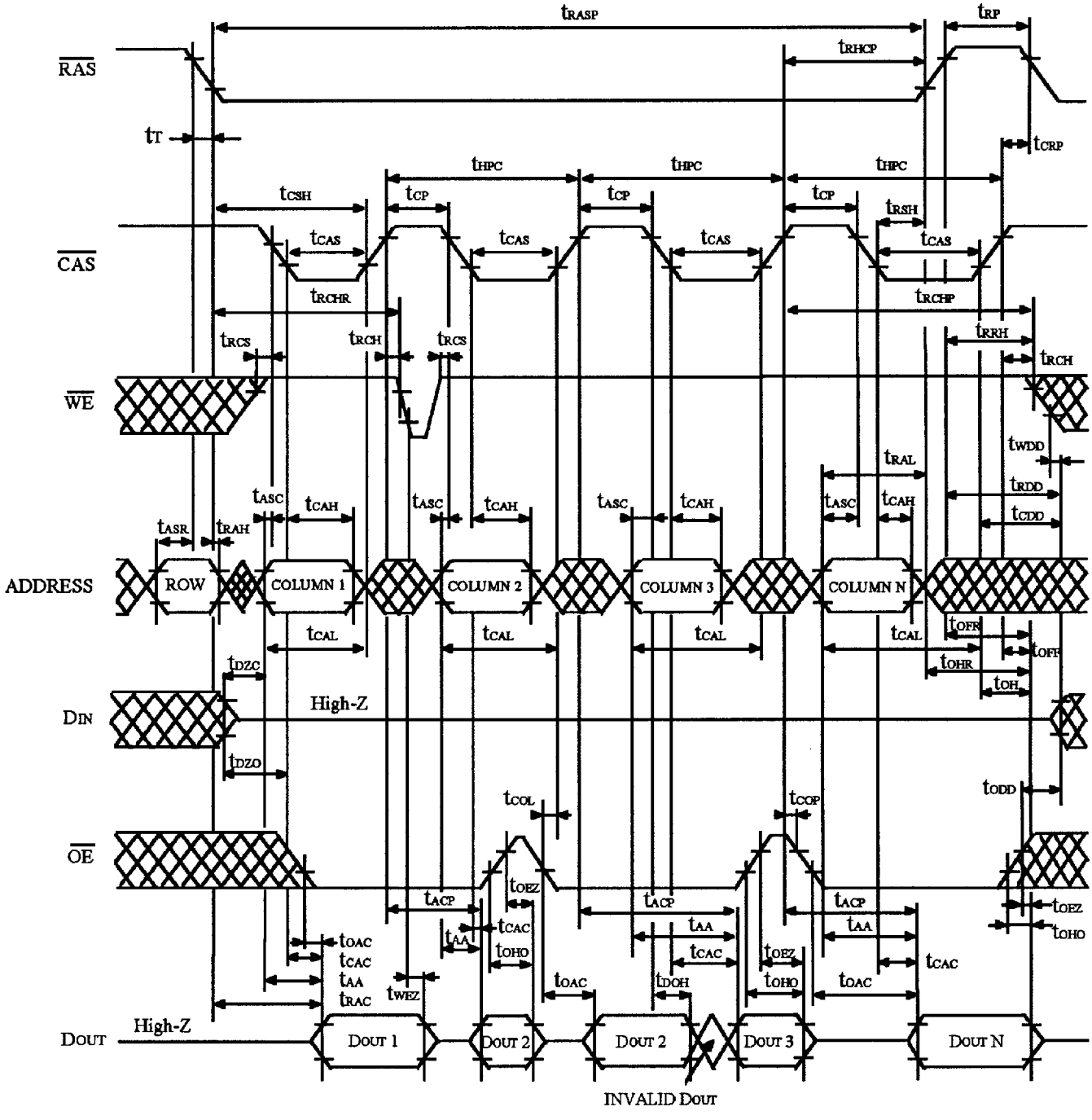


FIGURE 9. EXTENDED DATA OUT MODE READ CYCLE ($\overline{OE}$ CONTROL) *25

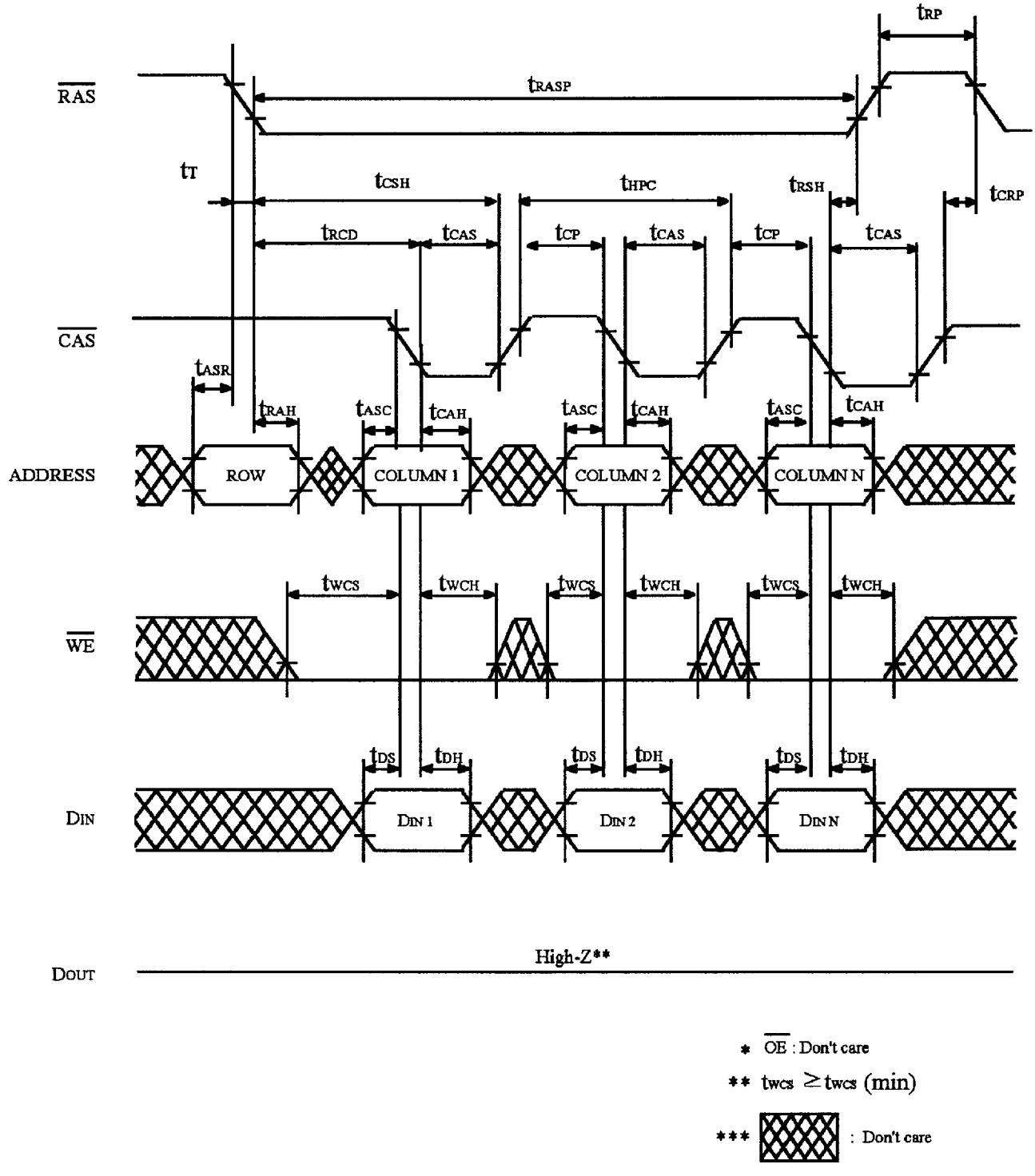


FIGURE 10. EXTENDED DATA OUT MODE EARLY WRITE CYCLE

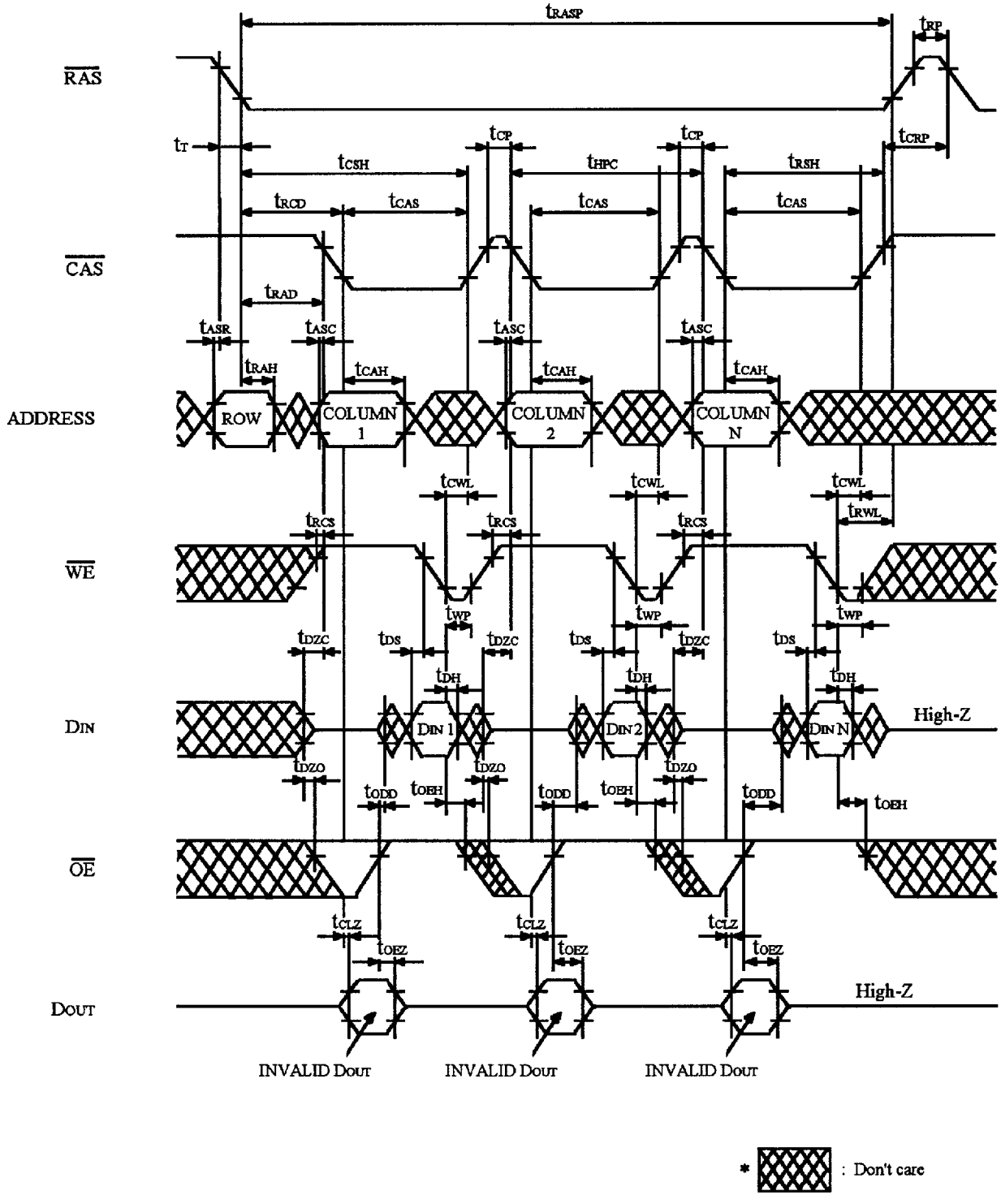


FIGURE 11. EXTENDED DATA OUT MODE DELAYED WRITE CYCLE *18

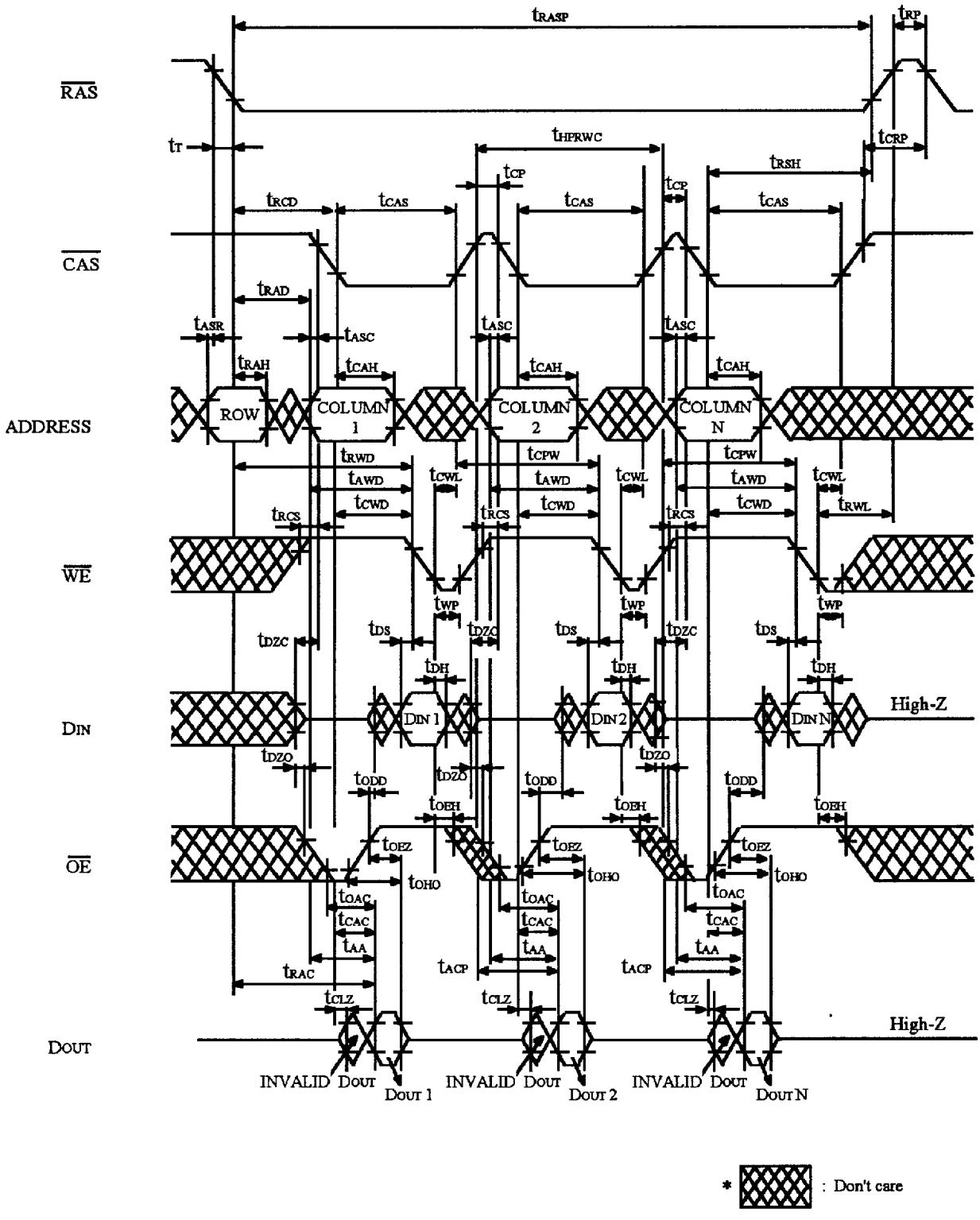


FIGURE 12. EXTENDED DATA OUT MODE READ MODIFY WRITE CYCLE [*18]

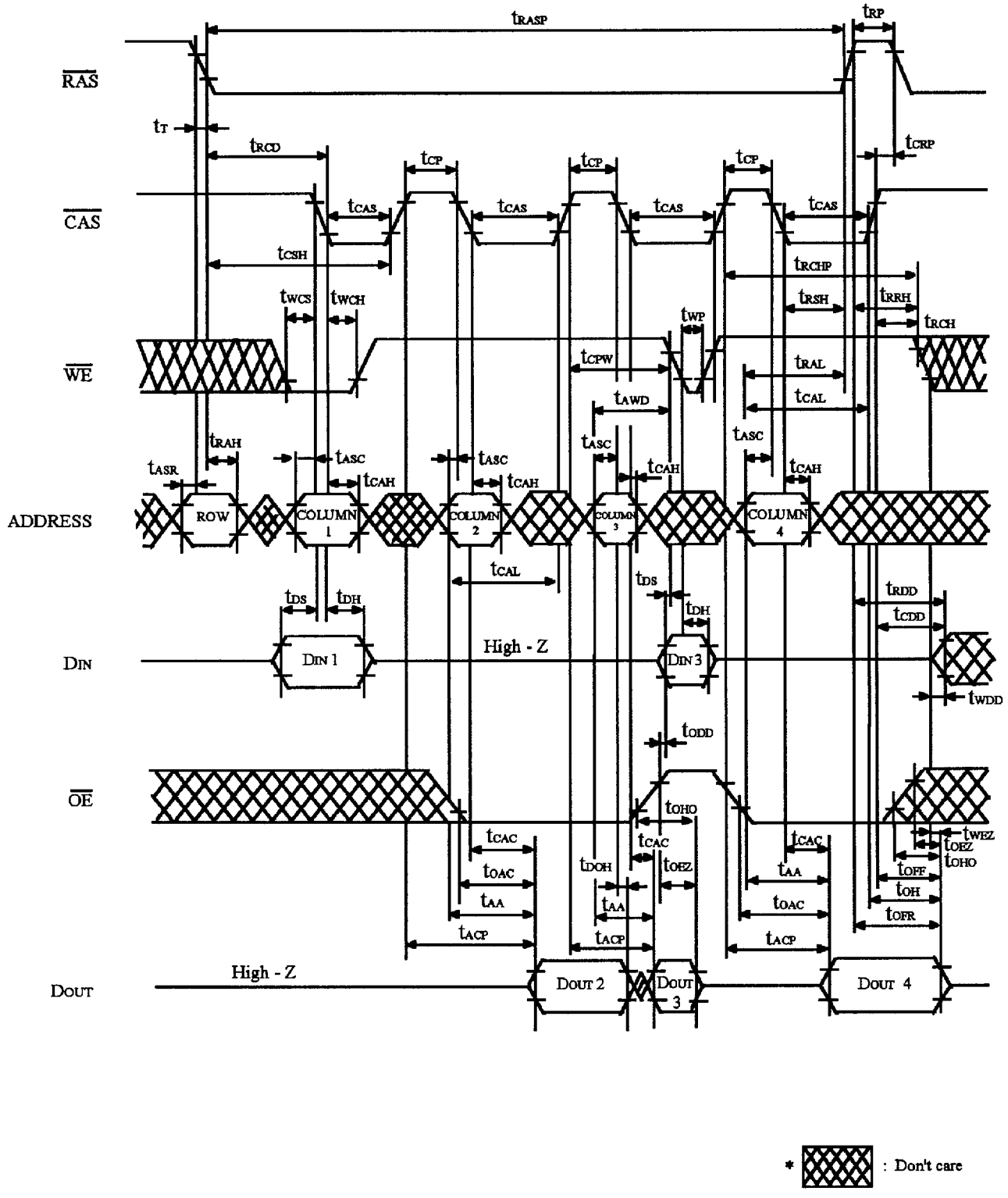


FIGURE 13. EXTENDED DATA OUT MODE MIX CYCLE (1) *26

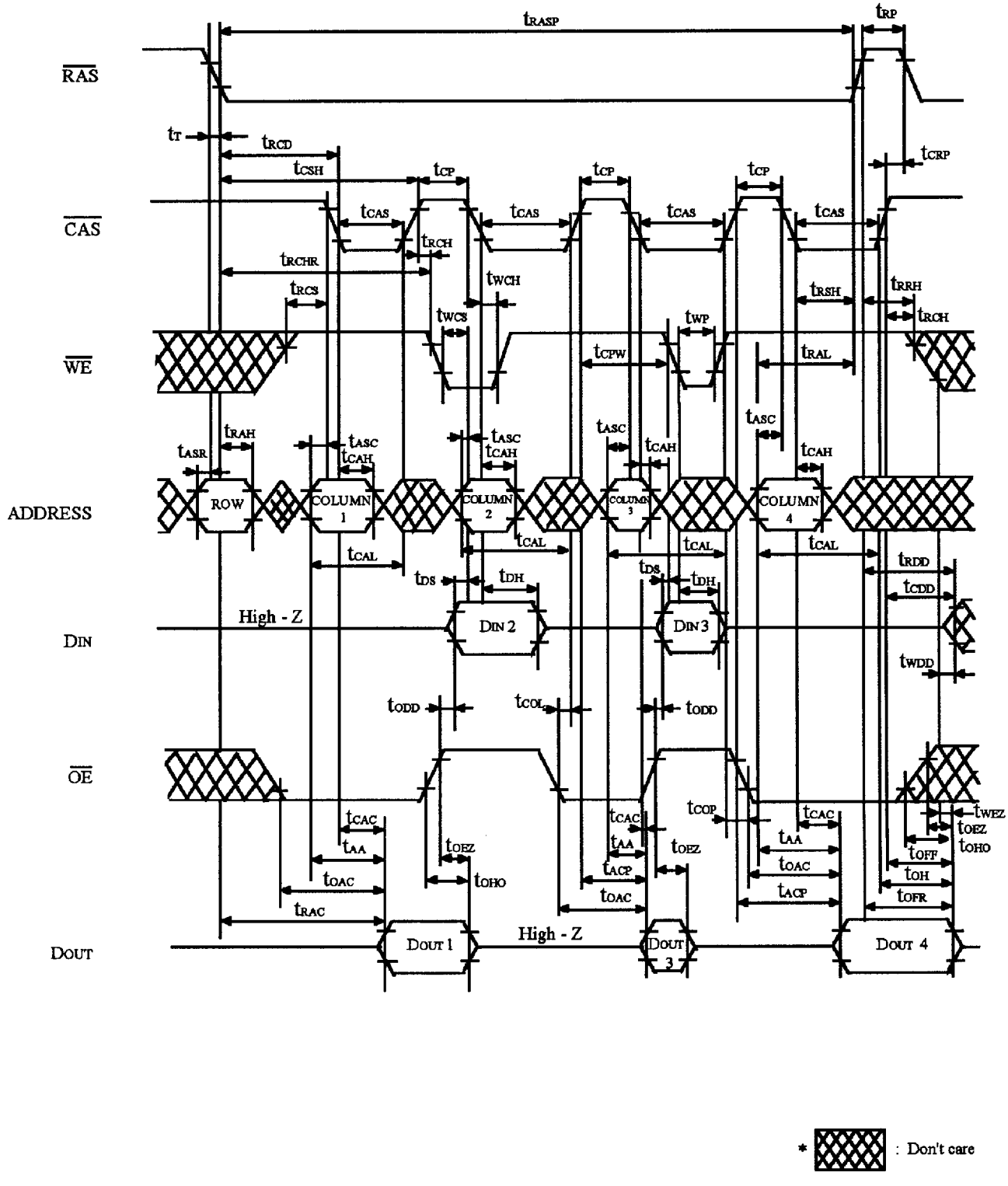


FIGURE 14. EXTENDED DATA OUT MODE MIX CYCLE (2) *26

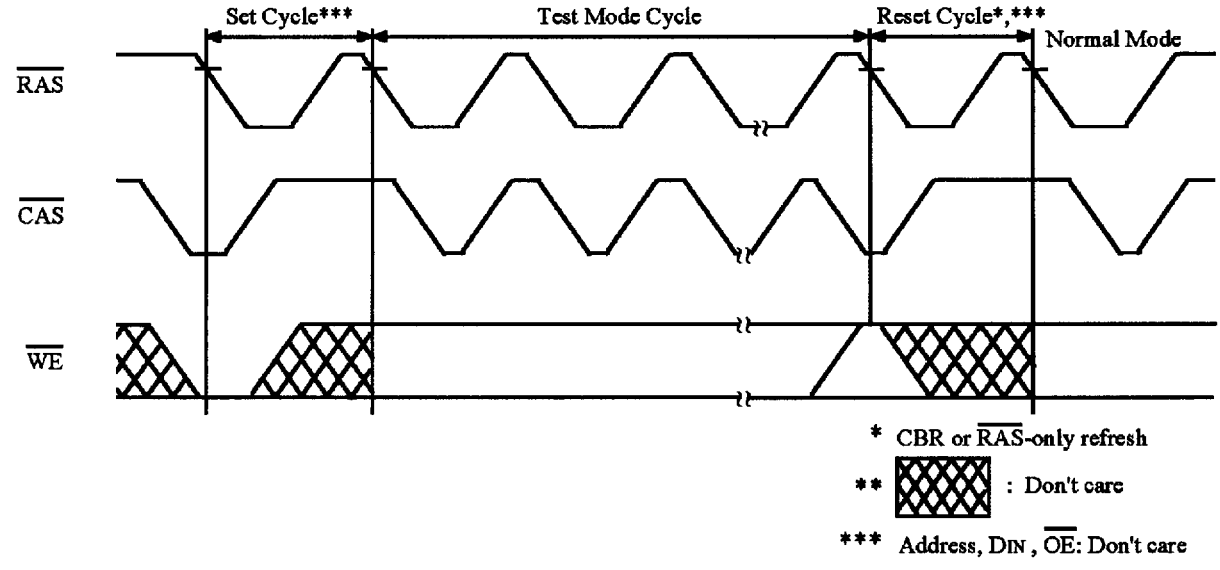


FIGURE 13. TEST MODE CYCLE *19

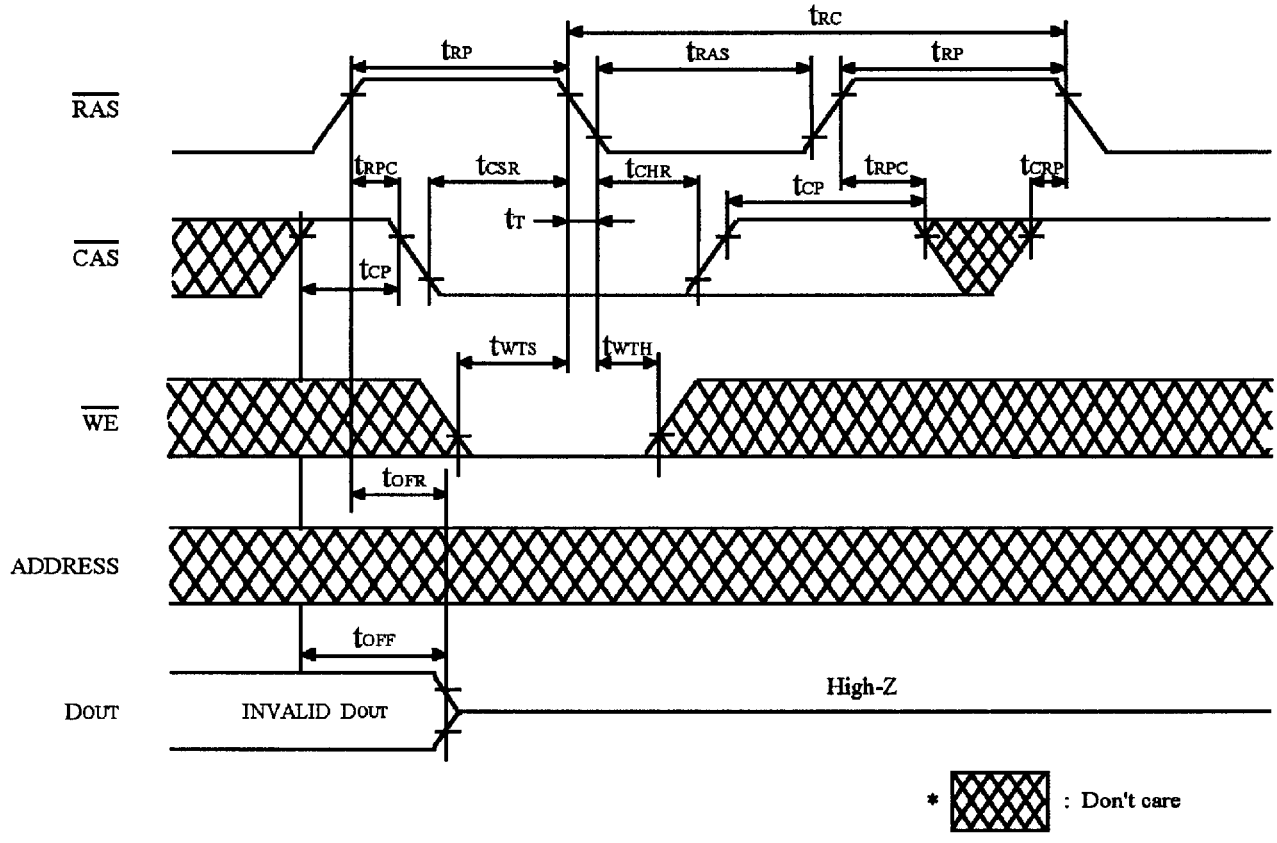


FIGURE 14. TEST MODE SET CYCLE

Test Mode Reset Cycle

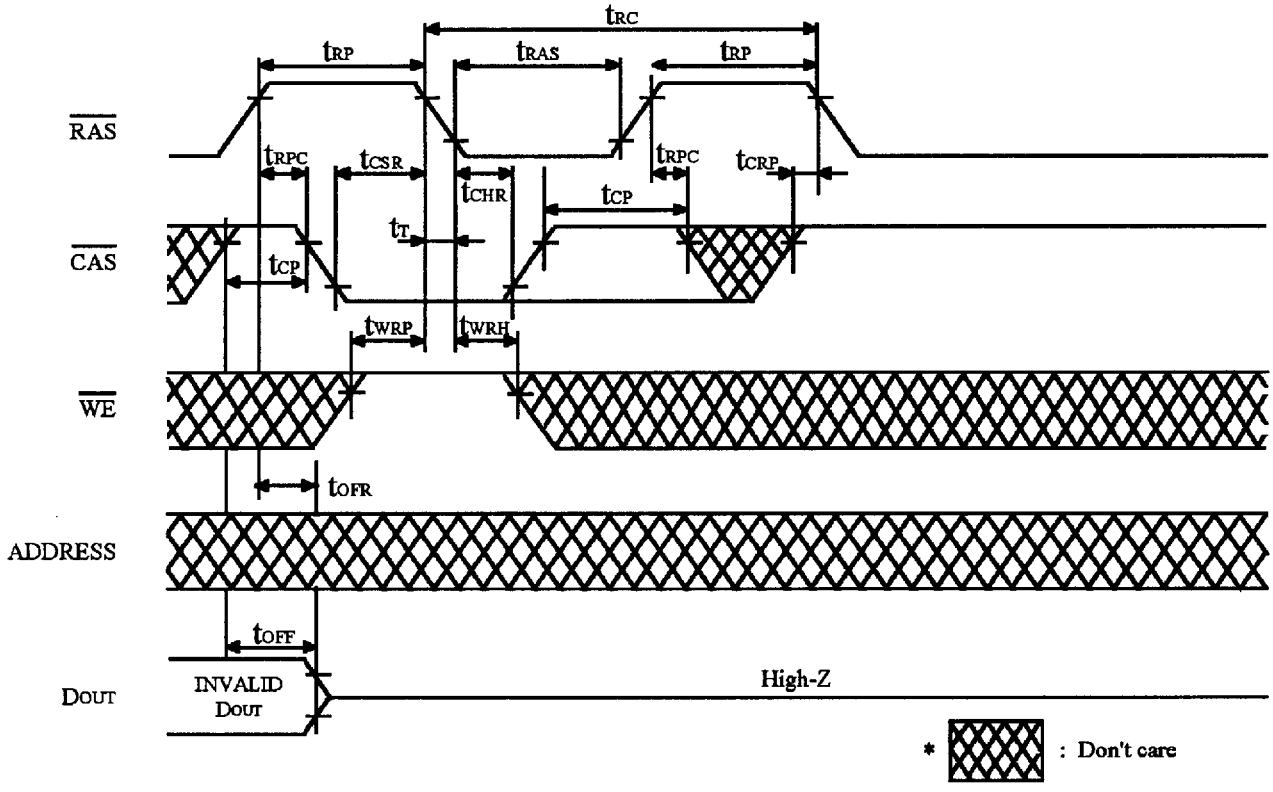


FIGURE 15. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

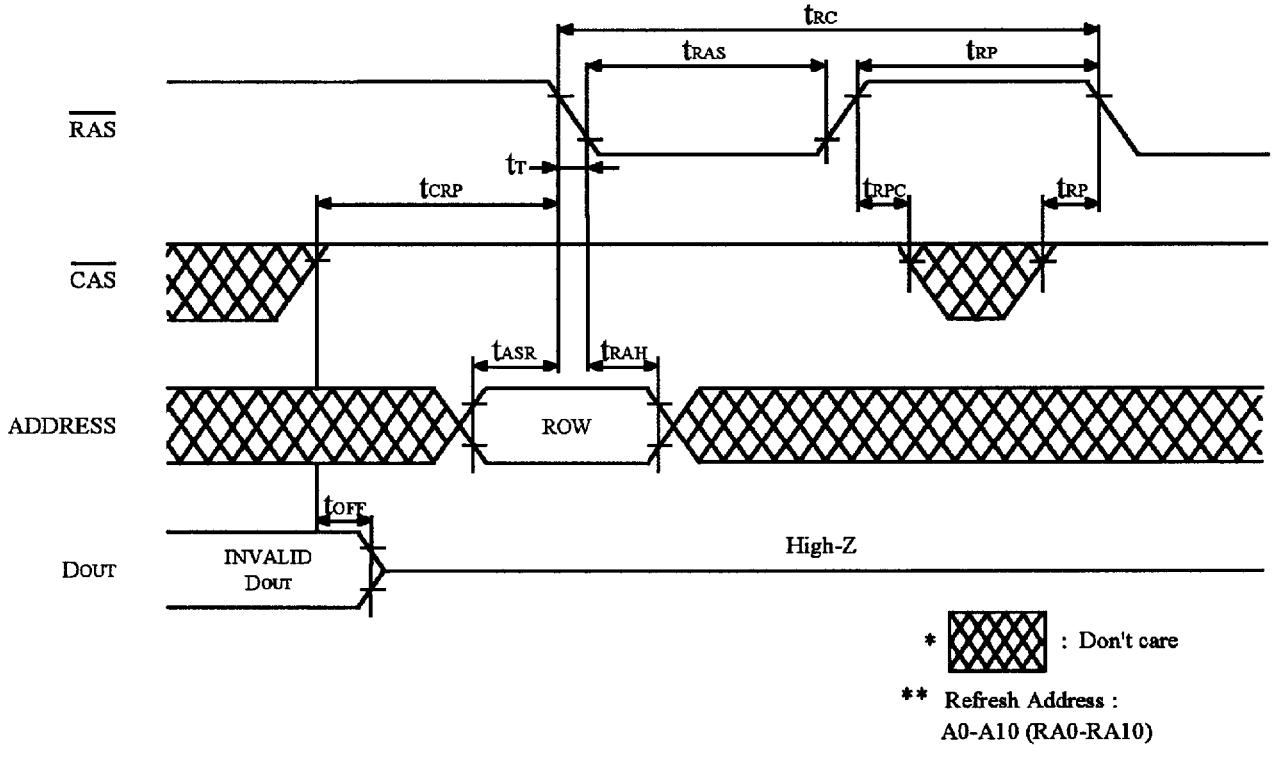


FIGURE 16. $\overline{RAS}$ ONLY REFRESH CYCLE

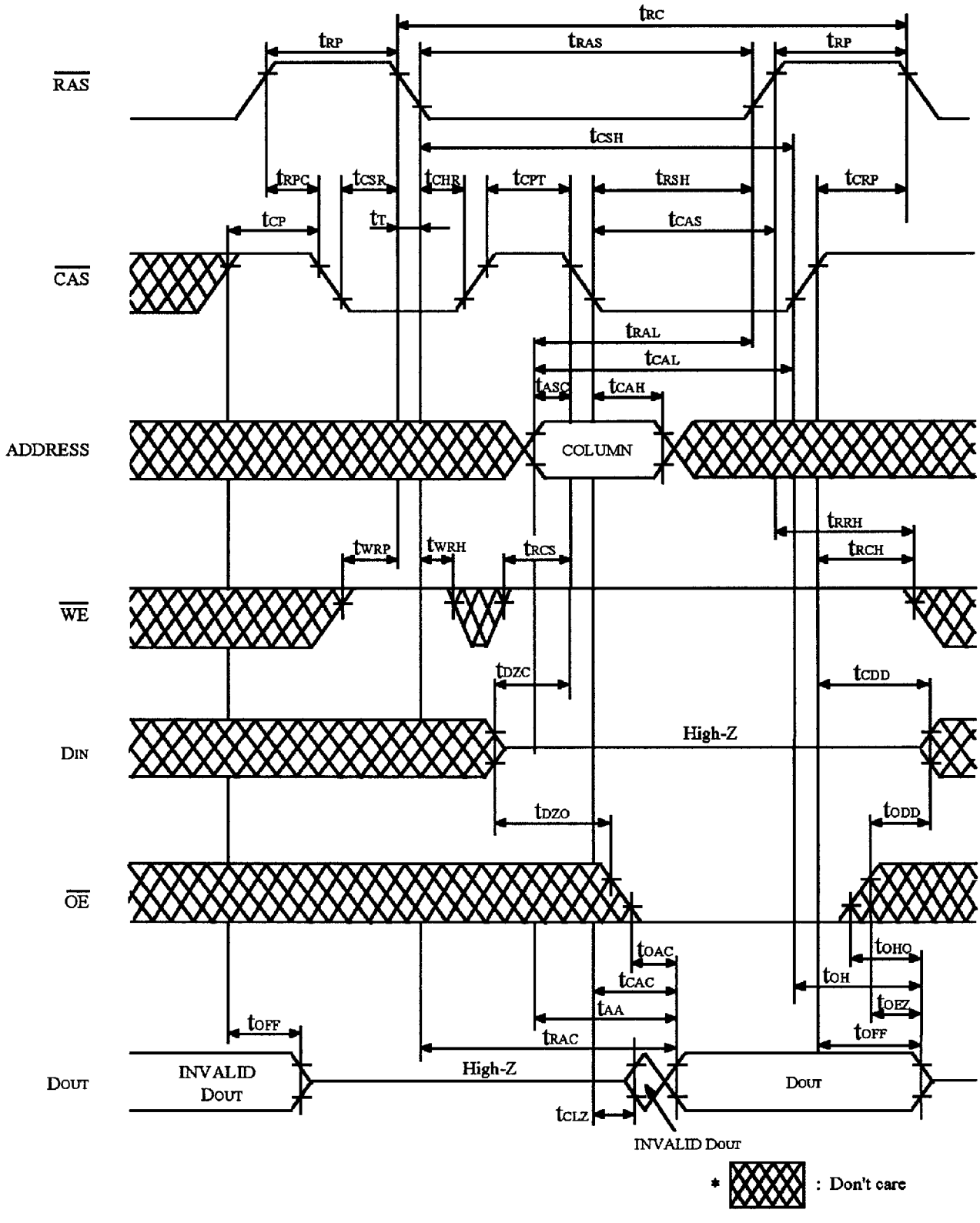


FIGURE 17. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

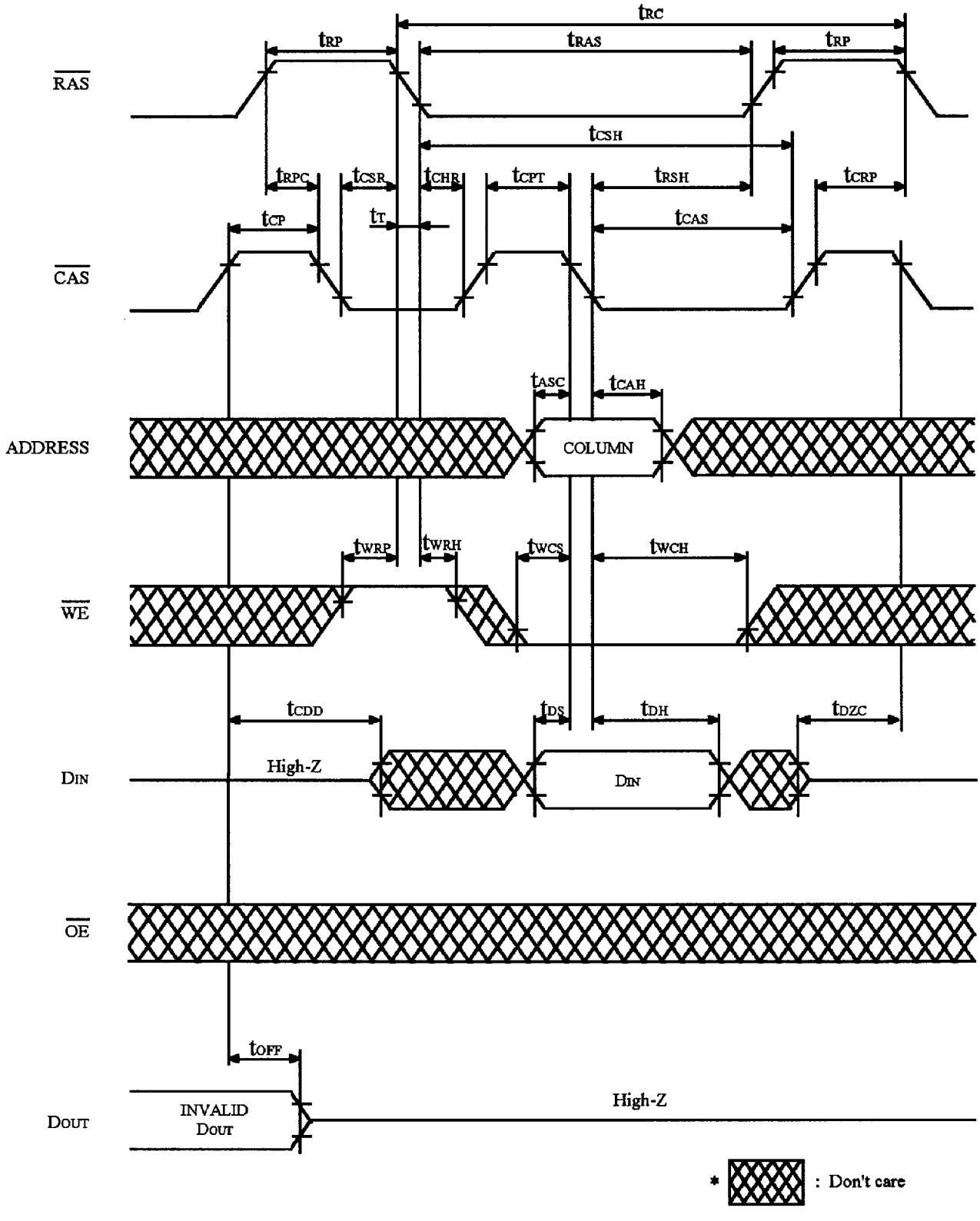
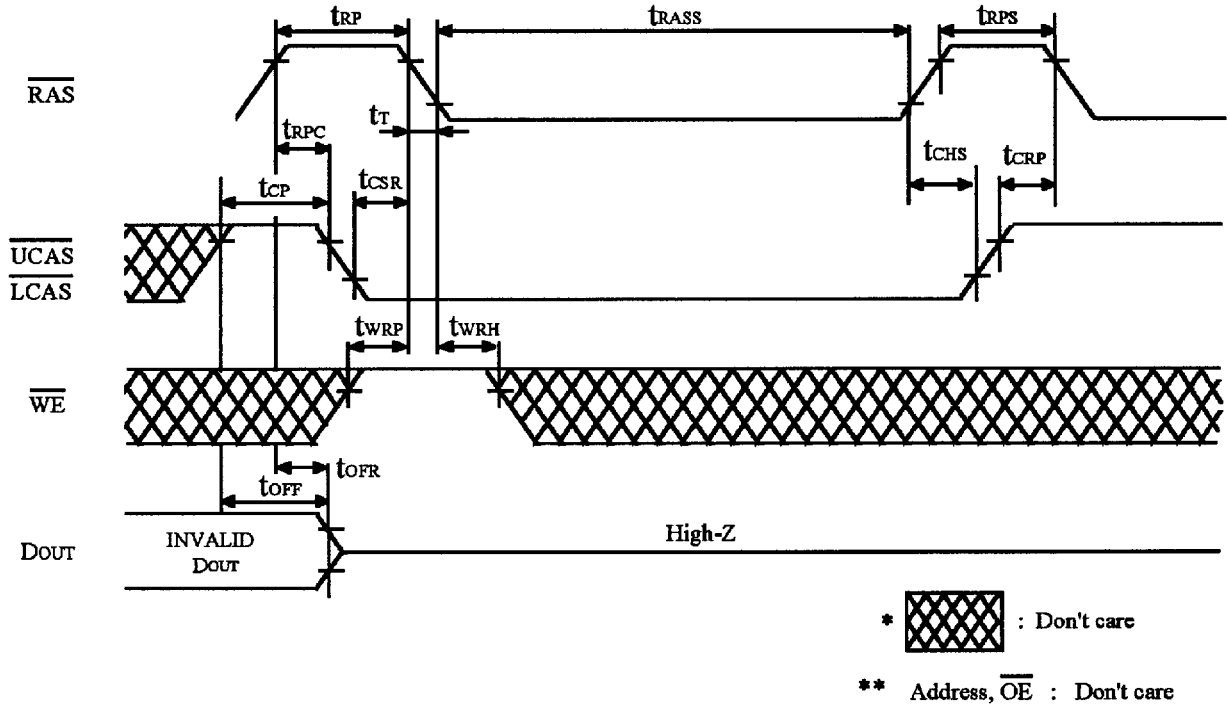


FIGURE 18. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (WRITE)



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

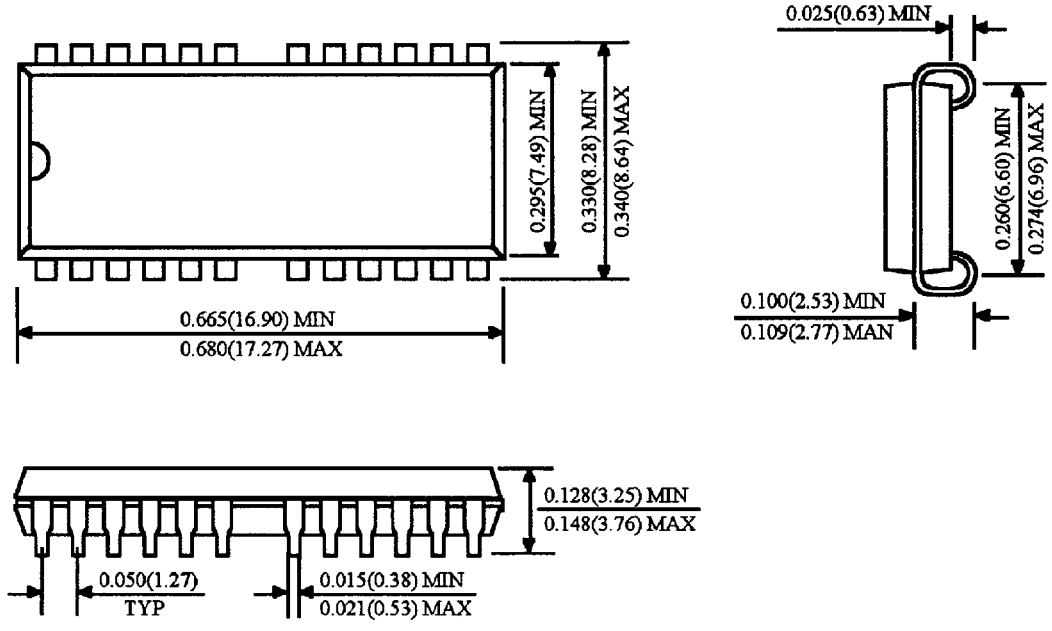
1. Please do not tRASS timing, $10\mu s \leq t_{RASS} \leq 100\mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu s$, then $\overline{RAS}$ precharge time should use tRPS instead of tRP.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 2048 cycles of distributed CBR refresh with 15.6μs interval should be executed within 32ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with 15.6μs interval in normal read/write cycle, CBR refresh should be executed within 15.6μs immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

FIGURE 19. SELF-REFRESH CYCLE

Package Dimension

Unit: Inches (mm)

24 (26) SOJ



24 (26) TSOP(TYPE II)