

CT 2542

Dual Redundant Remote Terminal

FOR MIL-STD-1553B

Features

- Replaces DDC BUS-65142 and BUS-65143
- Functions as a Complete Remote Terminal Unit
- Supports 13 Mode Codes, Illegalization of Codes Allowed
- Transfers Data with DMA Type Handshaking
- Latched Outputs for Command Word and Word Count
- 14 Bit Built-In-Test Word Register
- 4 Error Flag Outputs
- Advanced Low Power VLSI Technology
- DESC SMD# 5962-89798 Approved



General Description

The CT2542 contains 2 transceivers, 2 encoder/decoders, bit processors and complete Remote Terminal (RT) logic. The device is constructed using Aeroflex advanced VLSI custom chip and hybrid technology. It functions as a complete dual redundant MIL-STD-1553B RT Unit supporting all 13 mode codes for dual redundant operation. The CT2542 is a pin-for-pin functional equivalent of the DDC BUS-65142/143 and performs parallel data transfers with a DMA type handshake. Multiple error flag outputs and host access to many of the RT Status Word bits are just some of the features that make this part ideal for many RT applications. The unit has an operating range of -55°C to + 125°C. Aeroflex is a MIL-PRF-38534 Certified Manufacturer.

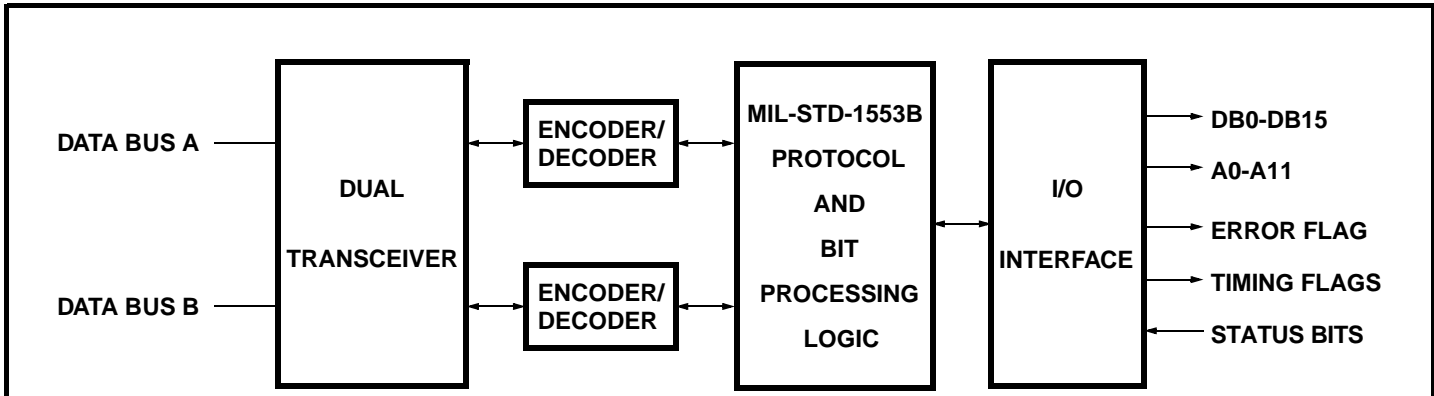


Figure 1 – Functional Block Diagram

Absolute Maximum Ratings

Parameter	Limits	Units
Power Supply Voltage (V _{EE})	+0.3 to -18.0	Volts
Power Supply Voltage (V _{CCL})	-0.3 to +7.0	Volts
Receiver Differential Input	±20 (40Vp-p)	Volts
Receiver Input Voltage	±15	Volts
Driver Output Current	+200	mA
Transmission Duty Cycle at T _C = 125°C	100	%
Operating Case Temperature Range (T _C)	-55 to +125	°C

Power and Thermal Data (Transceiver and Logic Section)

Parameter/Conditions	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V _{EE} V _{CCL}	-14.25 4.5	-15 5	-15.75 5.5	V V
Power Dissipation of most critical (hottest) device in hybrid during continuous transmission (100% Duty Cycle)	P _C		350		mW Note 1
Thermal Resistance, most critical device	∅ _{JC}		60		°C/W
Junction to case temperature rise of most critical device at 100% duty cycle	T _{JC}		60	80	°C
Total supply current standby mode, or transmitting at less than 1% duty cycle (e.g. 20us of transmission every 2ms or longer interval)	I _{CCL} I _{EE}		50	50 70	mA mA Note 2
Total supply current transmitting at 1Mhz into a 35-ohm load at point A in Figure 2	I _{EE} @ 50% I _{EE} @ 100%			175 270	mA Note 3 mA Note 3

Note 1: Decreases linearly to zero at zero duty cycle.

Note 2: I_{CCL} limit does not change with mode of operation or duty cycle.

Note 3: Decreases linearly to applicable "standby" values at zero duty cycle.

Electrical Characteristics (Receiver Section)

Parameter/Conditions	Symbol	Min	Typ	Max	Units
Differential input impedance DC to 1MHz, Point B, Figure 1	Z_{IN}	2K			Ω
Differential voltage range	V_{DIR}	$\pm 20V$			Vpeak
Input common mode voltage range	V_{ICR}	$\pm 10V$			Vpeak
Common mode rejection ratio (from point A, Figure 1)	CMMR	40			dB
Threshold characteristics (Sine wave at 1MHz) Note: Threshold voltages refer to point A, Figure 1.	V_{th}	0.6		1.2	Vp-p

Electrical Characteristics (Transmitter Section)

Parameter/Conditions	Symbol	Min	Typ	Max	Units
Differential output level at point B, Figure 1 (145 ohm load)	V_O	26		35	Vp-p
Rise and Fall times (10% to 90% of p-p output)	T_r	100		300	nS
Output offset at point A in Figure 2 (35-ohm load) 2.5us after mid-bit crossing of parity bit of last word of a 660us message	V_{OS}		± 20	± 90	mV Vpeak
Differential output noise	V_{NOI}			10	mV pp

Logic Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input "1"	2.4			VDC	
V_{IL}	Input "0"			0.7	VDC	
I_{IL}	Input I	-80		-400	μ A	Note 1A
I_{IH}	Input I	-40		-200	μ A	Note 1B
I_{IL}	Input I	-20		+20	μ A	Note 2A
I_{IH}	Input I	-20		+20	μ A	Note 1B
I_{IL}	Input I	-20		-200	μ A	Note 5
I_{IH}	Input I	-40		-400	μ A	
V_{OH}	Output "1"	2.7			VDC	Note 3A/4A
V_{OL}	Output "0"			0.4	VDC	Note 3B/4B

Note 1 For INPUT pins 12,13,14,15, 53, 54, 55.
VCC= 5.5V
A. @ V_{IL} = 0.4V
B. @ V_{IH} = 2.4V

Note 2 All remaining INPUTS other than in Note 1.
VCC= 5.5V
A. @ V_{IL} = 0.4V
B. @ V_{IH} = 2.4V

Note 3 For OUTPUT pins 4 through 11 and 43 through 50.
A. @ VCC = 4.5V and I_{OH} = 2mA
B. @ VCC = 4.5V and I_{OL} = 4mA

Note 4 All remaining OUTPUTS other than in Note 3.
A. @ VCC = 4.5V and I_{OH} = 1mA
B. @ VCC = 4.5V and I_{OL} = 2mA

Note 5 For INPUT pins 4-11, 43-50.
VCC= 5.5V
A. @ V_{IL} = 0.4V
B. @ V_{IH} = 2.4V

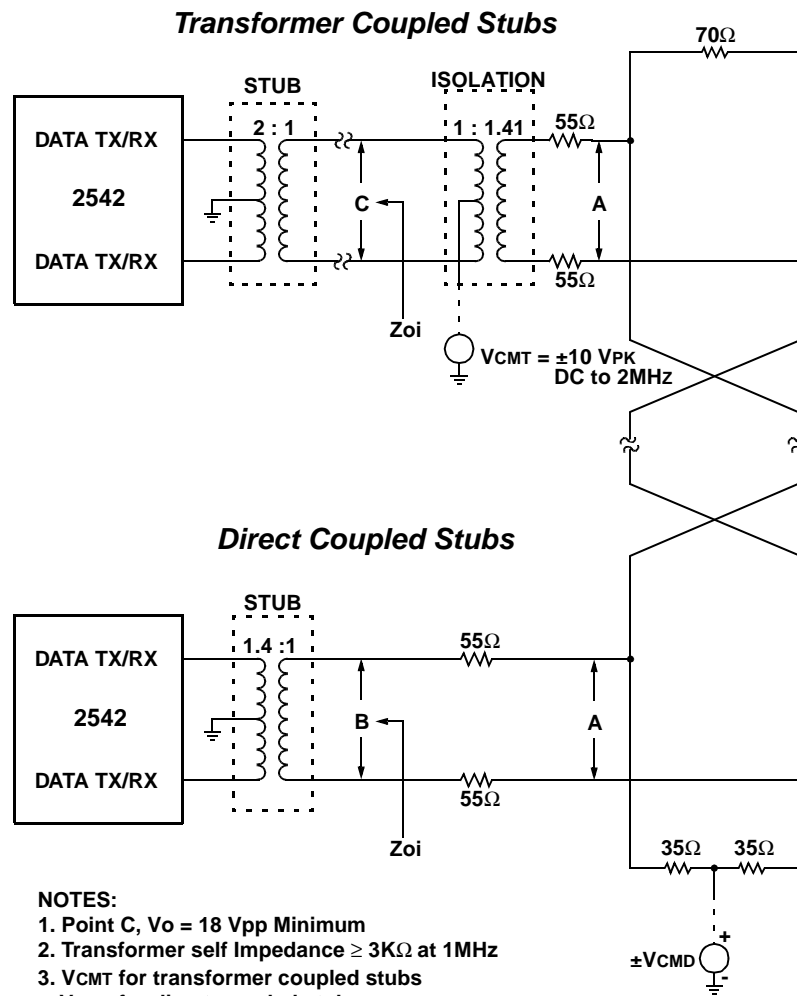


Figure 1 – Typical Bus Coupling

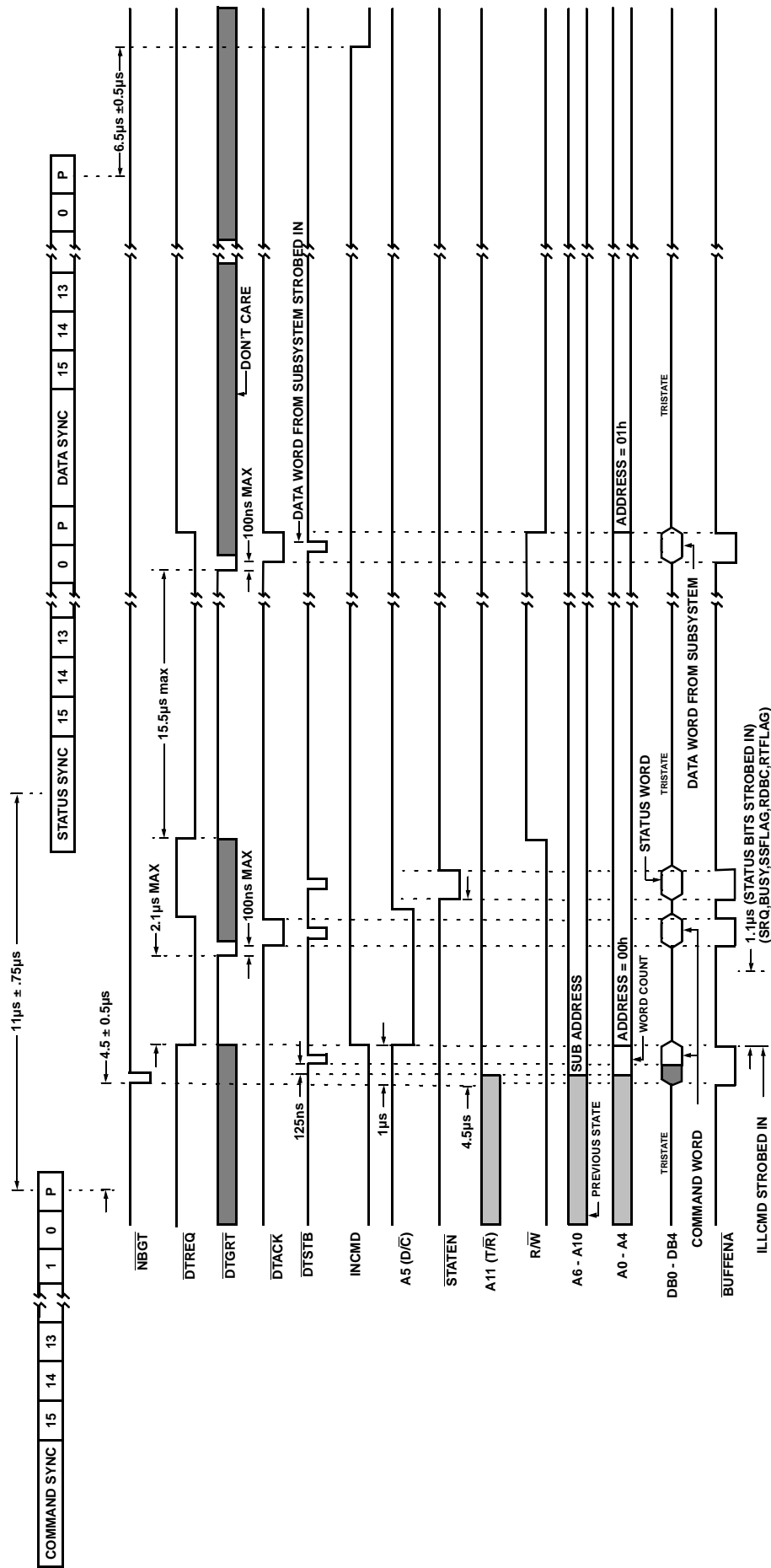


Figure 3 – Timing Diagram, Transmit One Word

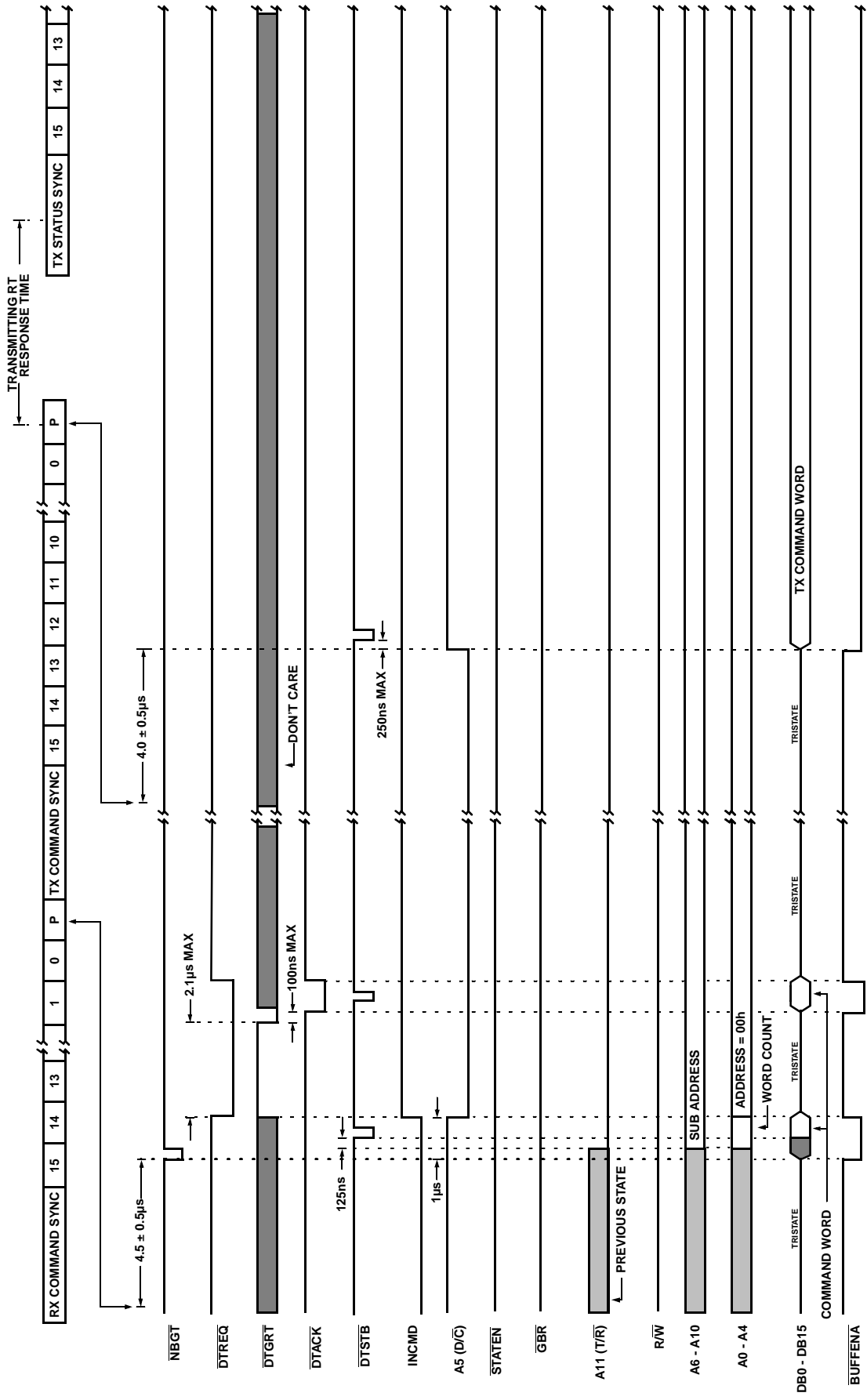


Figure 5 – Timing Diagram, RT to RT Receive One Word (Part A)

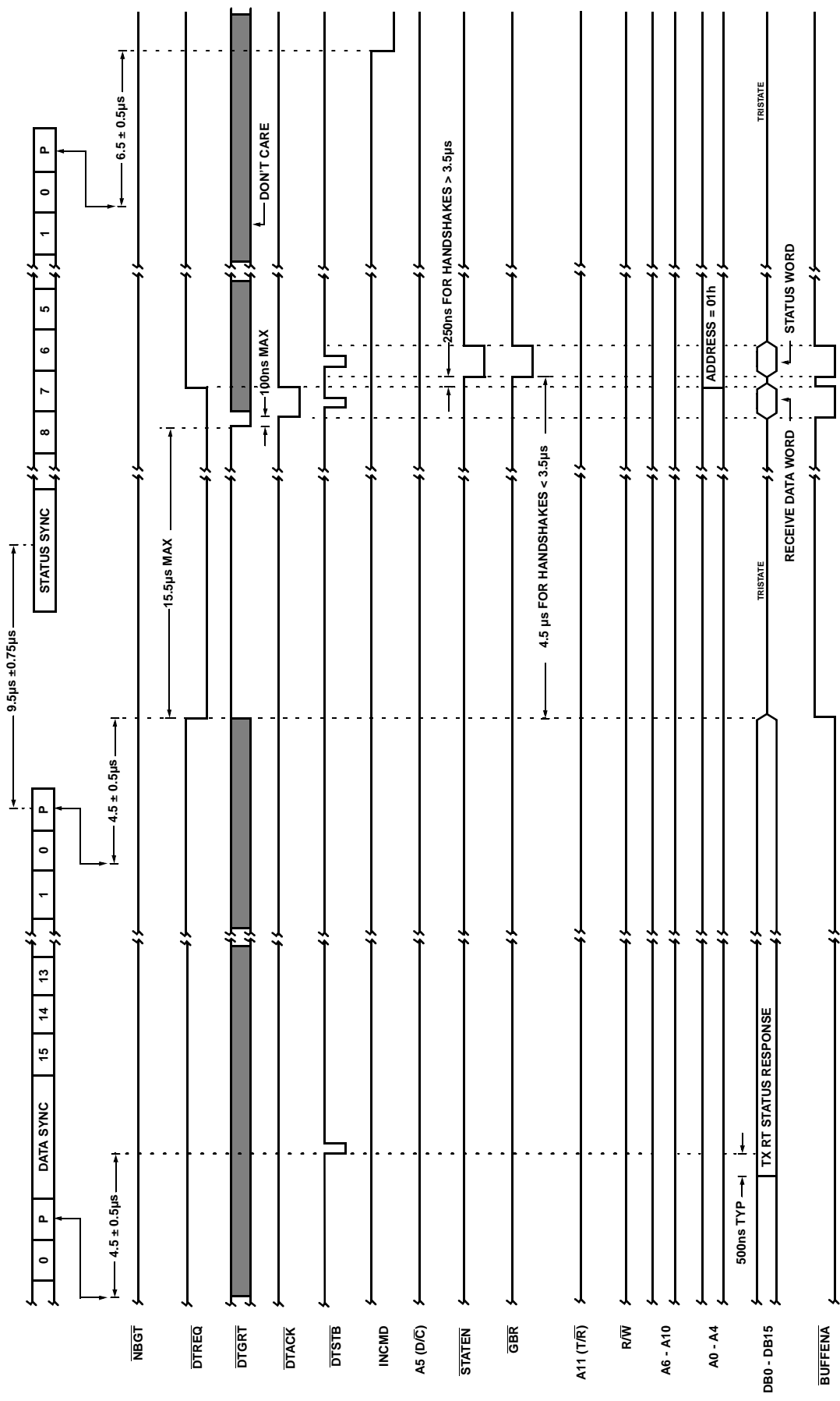
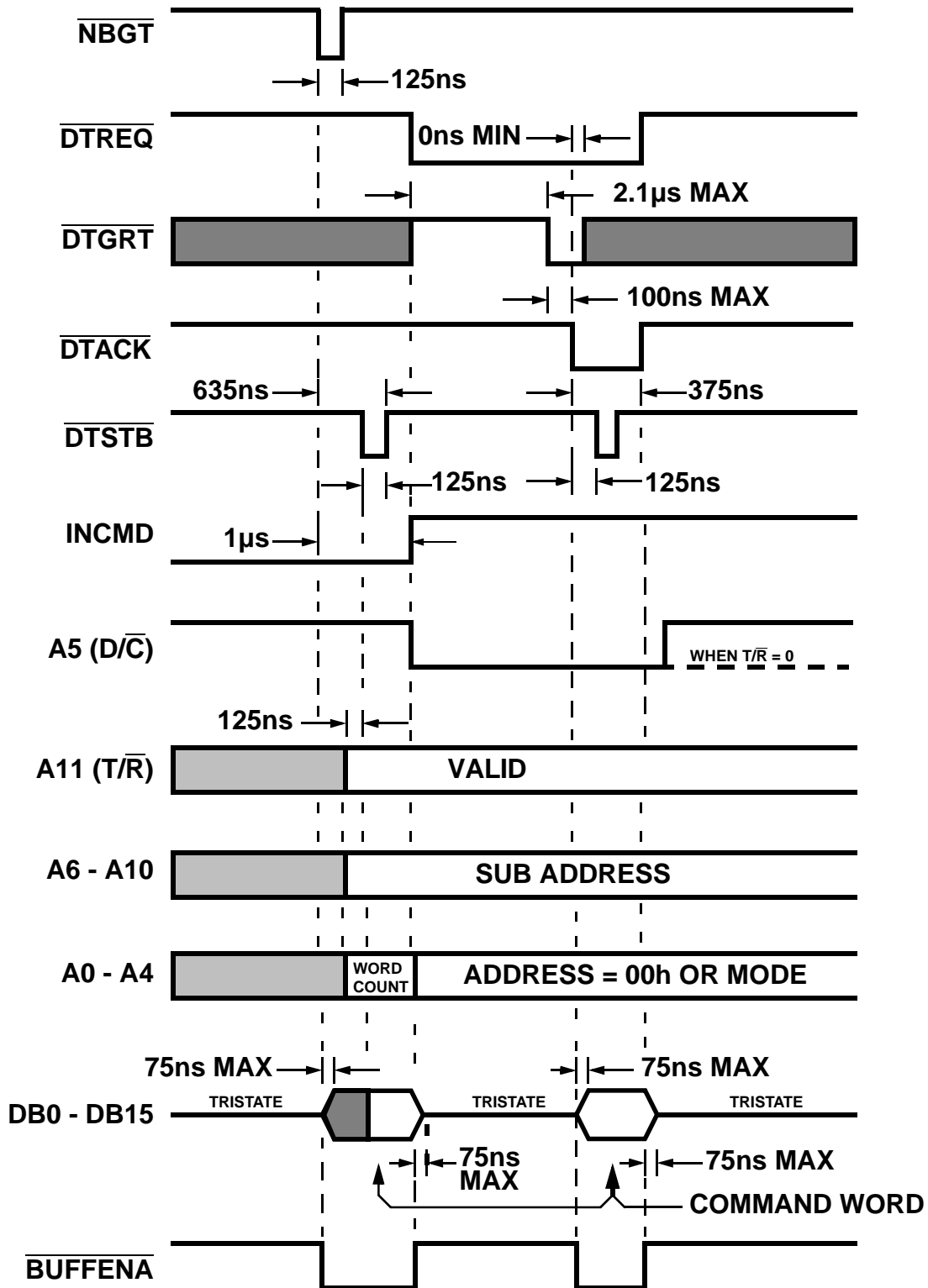
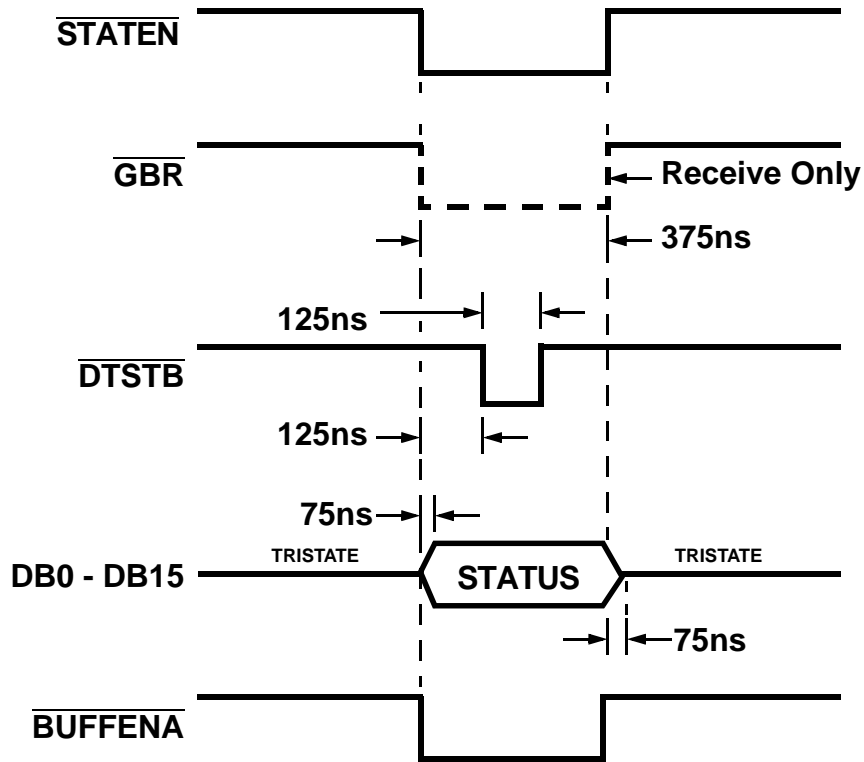


Figure 5 – Timing Diagram, RT to RT Receive One Word (Part B)



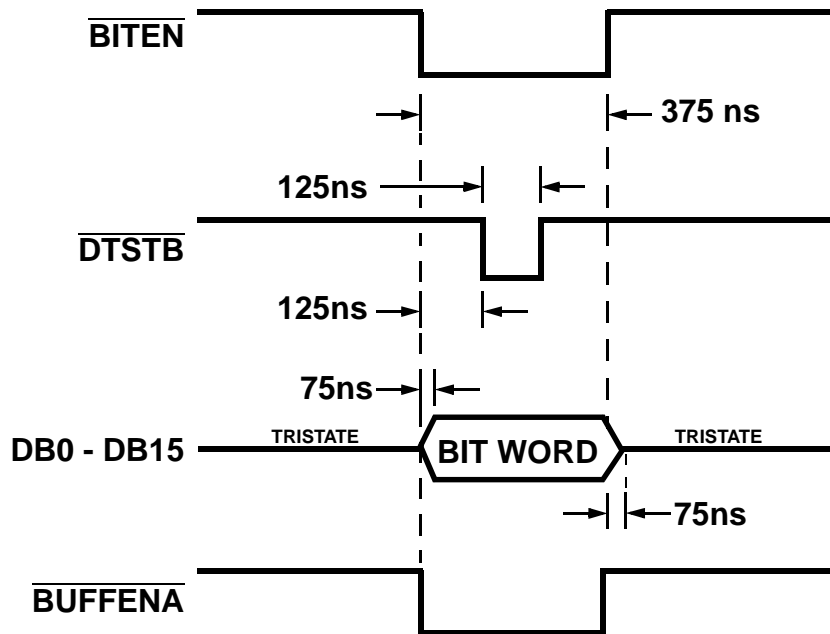
NOTE:
1. R/W = LOGIC 0

Figure 6 – TIMING DIAGRAM, COMMAND WORD TRANSFER



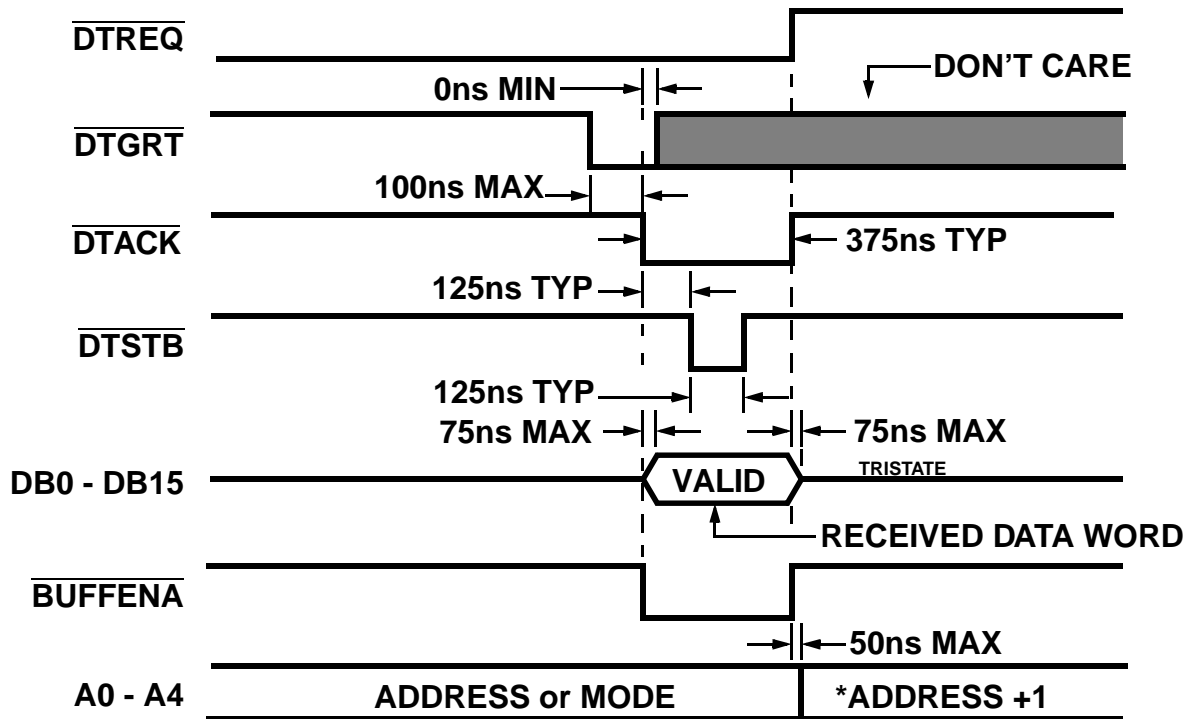
NOTE:
1. R/W = LOGIC 0

Figure 7 – Timing Diagram, Status Word Transfer



NOTE:
1. R/W = LOGIC 0

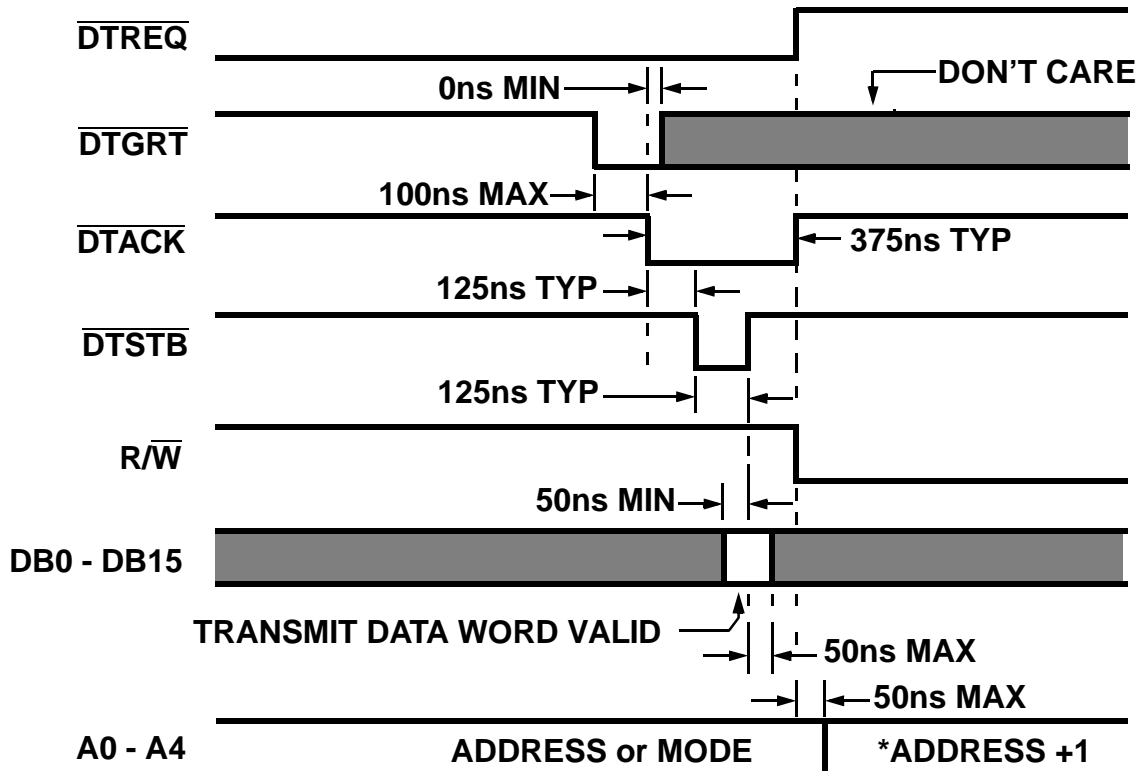
Figure 8 – Timing Diagram, Bit Word Transfer



NOTES: A0 - A4

1. R/W = Logic 0
2. (*) = Non-Mode Only
3. BUFFENA = DTACK

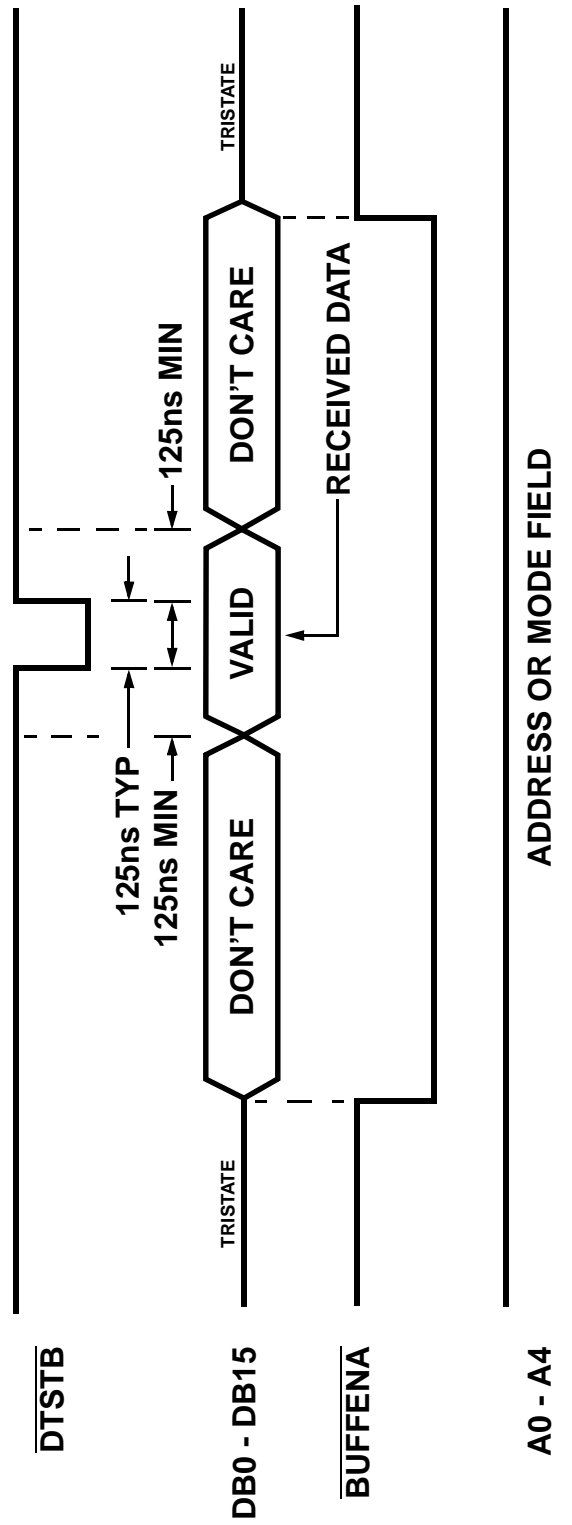
Figure 9 – Timing Diagram, Data to Subsystem



NOTES: A0 - A4

1. (*) = Non-Mode Only
2. Word Count for Mode Code
3. BUFFENA = Don't Care

Figure 10 – Timing Diagram, Data from Subsystem

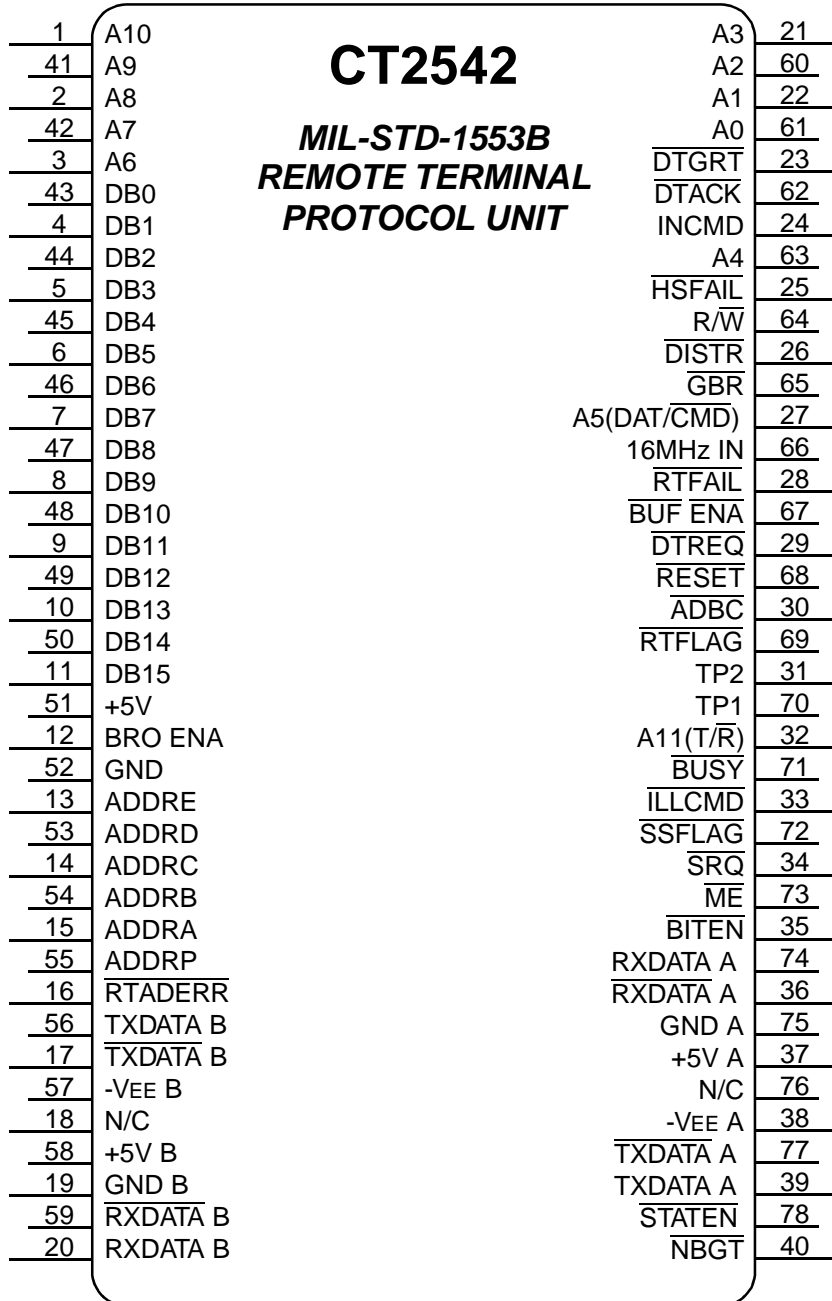


NOTES:

1. $\overline{R/W} = \text{LOGIC 0}$
2. $\text{DTGRT} = \text{DTREQ} = \text{LOGIC 1}$
3. $\text{INCMMD} = \text{DAT/CMD ARE LOGIC 1}$

Figure 11 – Timing Diagram, Data Transfers to Subsystem (No Handshake)

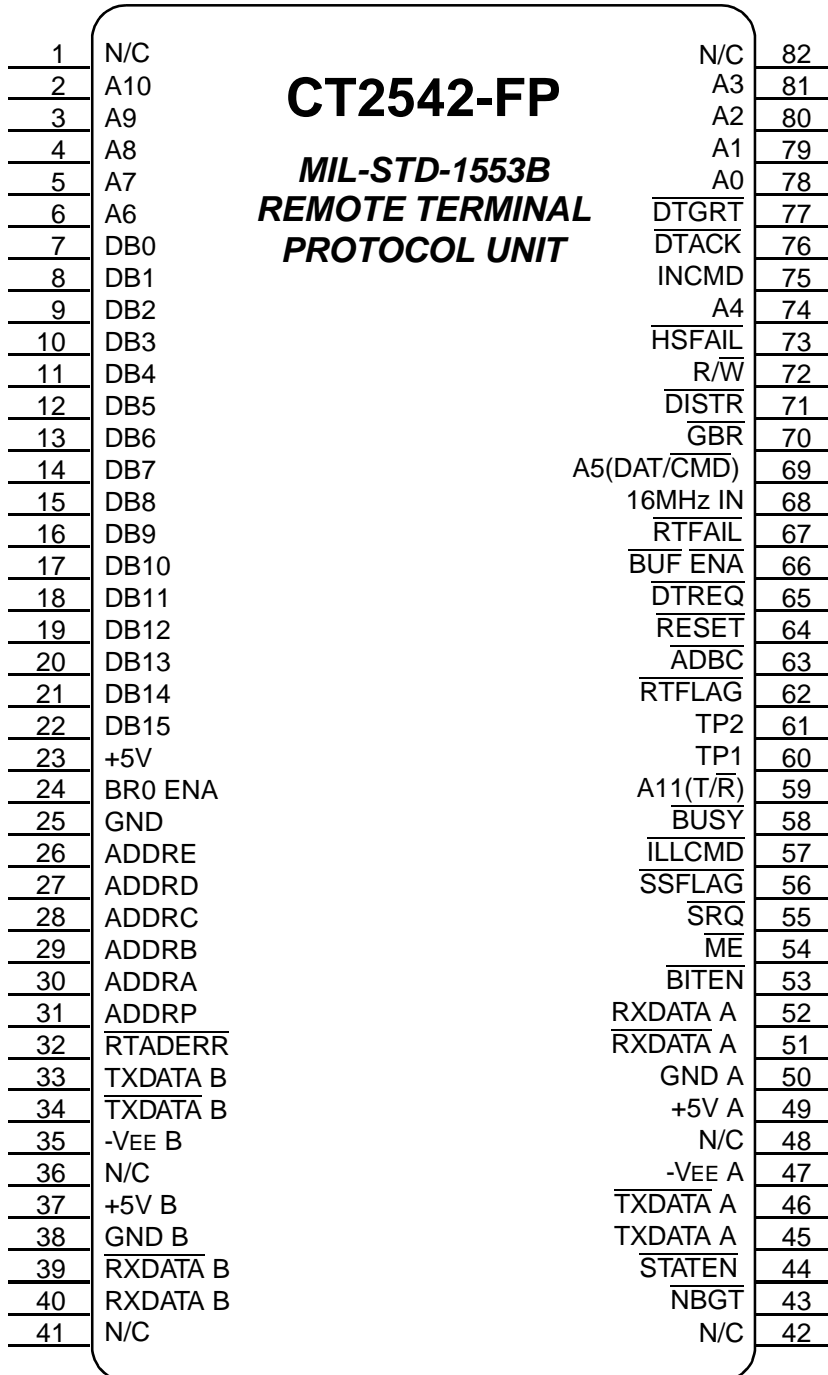
CT2542 Pin Out Description (DDIP)



Pin #	Function	Pin #	Function
1	A10	40	NBGT
2	A8	41	A9
3	A6	42	A7
4	DB1	43	DB0
5	DB3	44	DB2
6	DB5	45	DB4
7	DB7	46	DB6
8	DB9	47	DB8
9	DB11	48	DB10
10	DB13	49	DB12
11	DB15	50	DB14
12	BRO ENA	51	+5V
13	ADDRE	52	GND
14	ADDRC	53	ADDRD
15	ADDRA	54	ADDRB
16	RTADERR	55	ADDRP
17	TXDATA B	56	TXDATA B
18	N/C	57	-VEE B
19	GND B	58	+5V B
20	RXDATA B	59	RXDATA B
21	A3	60	A2
22	A1	61	A0
23	DTGRT	62	DTACK
24	INCMD	63	A4
25	HSFAIL	64	R/W
26	DTSTR	65	GBR
27	A5 (DAT/CMD)	66	16MHz IN
28	RTFAIL	67	BUF ENA
29	DTREQ	68	RESET
30	ADBC	69	RTFLAG
31	TP2 (NC)	70	TP1 (NC)
32	A11 (T/R)	71	BUSY
33	ILLCMD	72	SSFLAG
34	SRQ	73	ME
35	BITEN	74	RXDATA A
36	RXDATA A	75	GND A
37	+5V A	76	N/C
38	-VEE A	77	TXDATA A
39	TXDATA A	78	STATEN

Figure 12 – DDIP Pin Connection Diagram, CT2542 and Pinout Table

CT2542 Pin Out Description (FP)



Pin #	Function	Pin #	Function
1	NC	42	NC
2	A10	43	NBGT
3	A9	44	STATEN
4	A8	45	TXDATA A
5	A7	46	TXDATA A
6	A6	47	VEE A
7	DB0	48	N/C
8	DB1	49	+5V A
9	DB2	50	GND A
10	DB3	51	RXDATA A
11	DB4	52	RXDATA A
12	DB5	53	BITEN
13	DB6	54	ME
14	DB7	55	SRQ
15	DB8	56	SSFLAG
16	DB9	57	ILLCMD
17	DB10	58	BUSY
18	DB11	59	A11 (T/R)
19	DB12	60	TP1
20	DB13	61	TP2
21	DB14	62	RTFLAG
22	DB15	63	ADBC
23	+5V	64	RESET
24	BRO ENA	65	DTREQ
25	GND	66	BUF ENA
26	ADDRE	67	RTFAIL
27	ADDR D	68	16MHz IN
28	ADDR C	69	A5 (DAT/CMD)
29	ADDR B	70	GBR
30	ADDR A	71	DTSTR
31	ADDR P	72	R/W
32	RTADERR	73	HSFAIL
33	TXDATA B	74	A4
34	TXDATA B	75	INCMD
35	-VEE B	76	DTACK
36	+15V B	77	DTGRT
37	N/C	78	A0
38	GND B	79	A1
39	RXDATA B	80	A2
40	RXDATA B	81	A3
41	NC	82	NC

Figure 13 – Flat package Pin Connection Diagram, CT2542 and Pinout Table



Ordering Information

Model Number	Screening	DESC SMD #	Package
CT2542	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883	-	Plug in
CT2542-FP		-	Flat Package
CT2542-701	Industrial Temperature, -40°C to +85°C, No Burn-in	-	Plug in
CT2542-FP-701		-	Flat Package
CT2542	-	5962-8979803XA	Plug in
CT2542	-	5962-8979803XC	Plug in
CT2542-FP	-	5962-8979803YA	Flat Package
CT2542-FP	-	5962-8979803YC	Flat Package

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Specifications subject to change without notice.