

# TBB1010

## Twin Build in Biasing Circuit MOS FET IC VHF/VHF RF Amplifier

# RENESAS

ADE-208-1607B (Z)

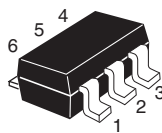
3rd. Edition  
Feb. 2003

### Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- High  $|y_{fs}|=29\text{mS} \times 2$
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at  $C = 200 \text{ pF}$ ,  $R_s = 0$  conditions.
- Provide mini mold packages; CMPAK-6

### Outline

CMPAK-6



1. Drain(1)
2. Source
3. Drain(2)
4. Gate-1(2)
5. Gate-2
6. Gate-1(1)

- Notes:
1. Marking is "KM".
  2. TBB1010 is individual type number of HITACHI TWIN BBFET.

**Absolute Maximum Ratings**

(Ta = 25°C)

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	V <sub>DS</sub>	6	V
Gate1 to source voltage	V <sub>G1S</sub>	+6 -0	V
Gate2 to source voltage	V <sub>G2S</sub>	+6 -0	V
Drain current	I <sub>D</sub>	30	mA
Channel power dissipation	P <sub>ch</sub> <sup>*3</sup>	250	mW
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 3. Value on the glass epoxy board (50mm × 40mm × 1mm).

## Electrical Characteristics

( $T_a = 25^\circ\text{C}$ )

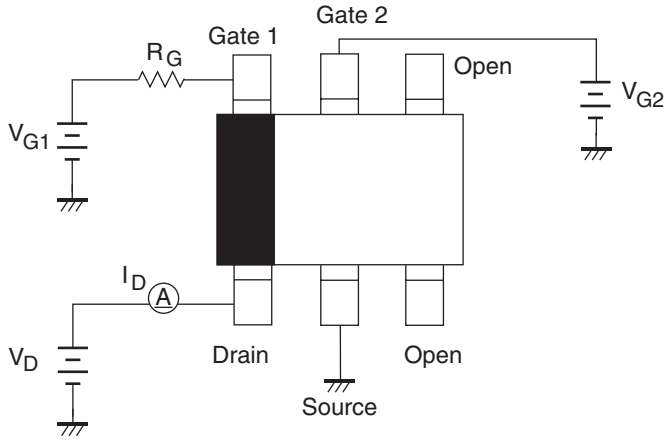
The below specification are applicable for FET1 and FET2 unit

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200\ \mu\text{A}$ , $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10\ \mu\text{A}$ , $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10\ \mu\text{A}$ , $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	$I_{G1SS}$	—	—	+100	nA	$V_{G1S} = +5\ \text{V}$ , $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	$I_{G2SS}$	—	—	+100	nA	$V_{G2S} = +5\ \text{V}$ , $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.6	—	1.1	V	$V_{DS} = 5\ \text{V}$ , $V_{G2S} = 4\ \text{V}$ , $I_D = 100\ \mu\text{A}$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.6	—	1.1	V	$V_{DS} = 5\ \text{V}$ , $V_{G1S} = 5\ \text{V}$ , $I_D = 100\ \mu\text{A}$
Drain current	$I_{D(op)}$	12	16	20	mA	$V_{DS} = 5\ \text{V}$ , $V_{G1} = 5\ \text{V}$ $V_{G2S} = 4\ \text{V}$ , $R_G = 120\ \text{k}\Omega$
Forward transfer admittance	$ y_{fs} $	24	29	—	mS	$V_{DS} = 5\ \text{V}$ , $V_{G1} = 5\ \text{V}$ , $V_{G2S} = 4\ \text{V}$ $R_G = 120\ \text{k}\Omega$ , $f = 1\ \text{kHz}$
Input capacitance	$C_{iss}$	1.7	2.1	2.5	pF	$V_{DS} = 5\ \text{V}$ , $V_{G1} = 5\ \text{V}$
Output capacitance	$C_{oss}$	1.0	1.4	1.8	pF	$V_{G2S} = 4\ \text{V}$ , $R_G = 120\ \text{k}\Omega$
Reverse transfer capacitance	$C_{rss}$	—	0.03	0.05	pF	$f = 1\ \text{MHz}$
Power gain	PG	25	30	—	dB	$V_{DS} = V_{G1} = 5\ \text{V}$ , $V_{G2S} = 4\ \text{V}$
Noise figure	NF	—	1.1	1.8	dB	$R_G = 120\ \text{k}\Omega$ , $f = 200\ \text{MHz}$

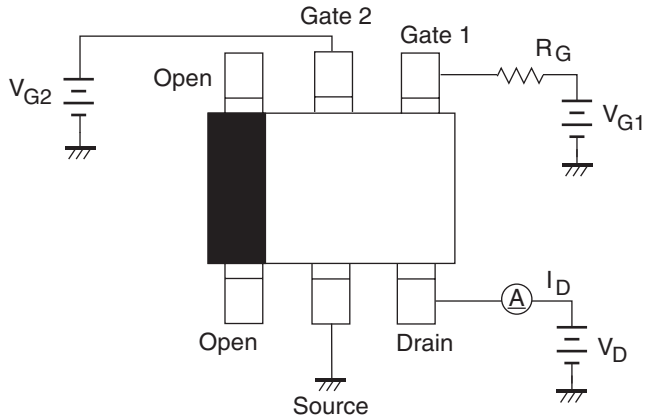
## Test Circuits

- DC Biasing Circuit for Operating Characteristic Items ( $I_{D(op)}$ ,  $|y_{fs}|$ ,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ , NF, PG)

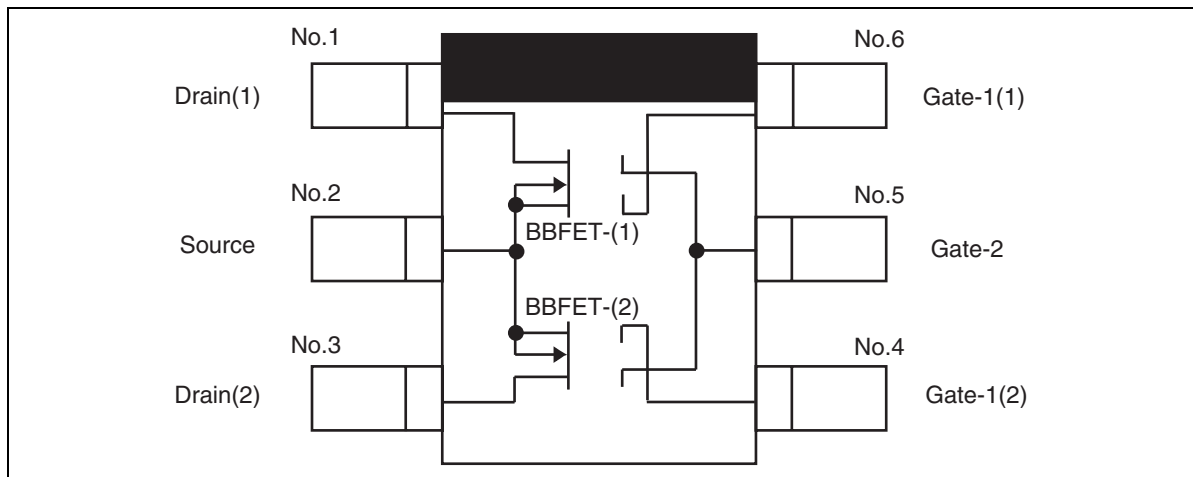
Measurement of FET1



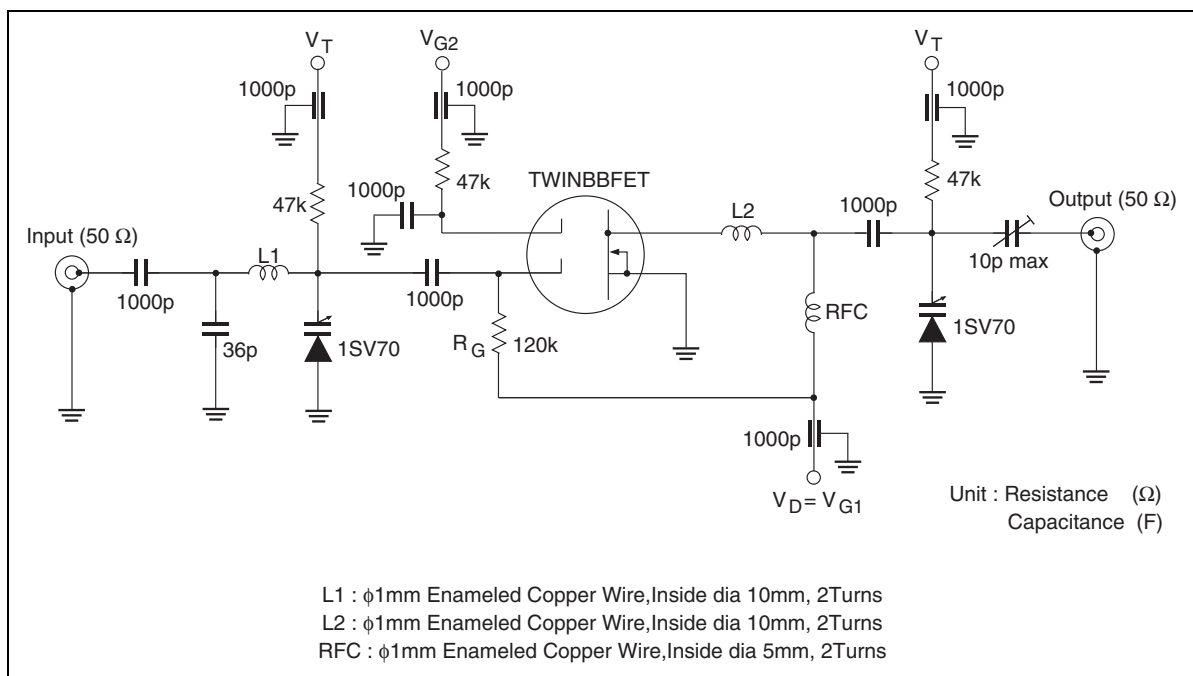
Measurement of FET2



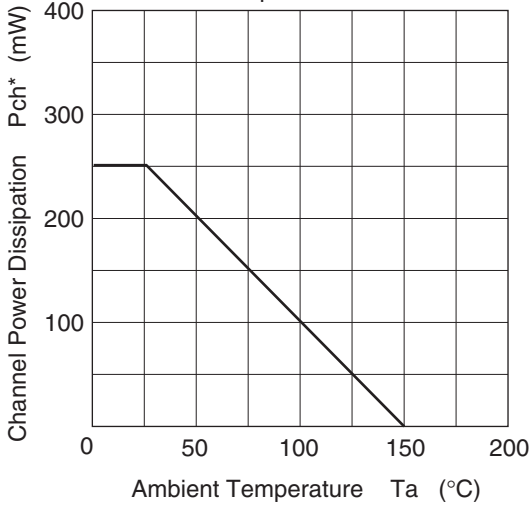
• Equivalent Circuit



• 200 MHz Power Gain, Noise Figure Test Circuit

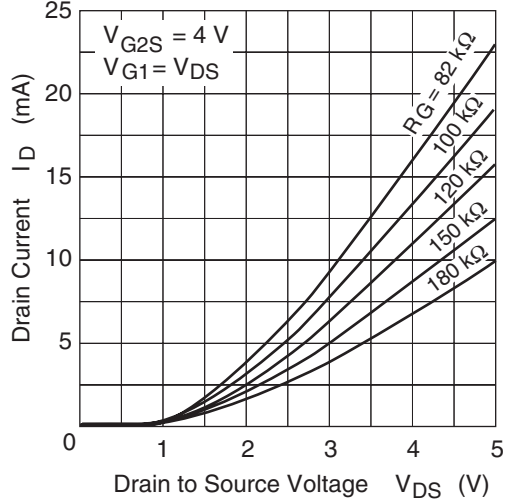


Maximum Channel Power Dissipation Curve

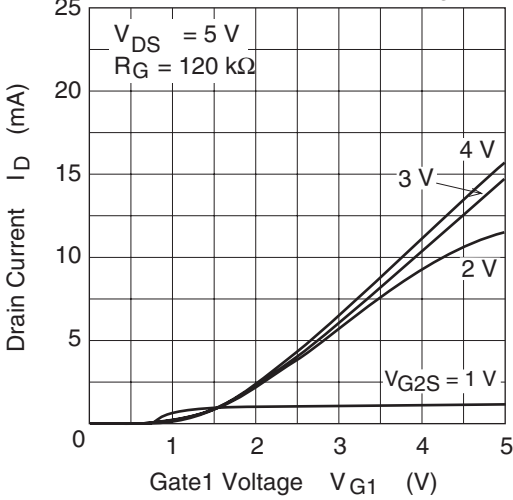


\* Value on the glass epoxy board (50mm × 40mm × 1mm)

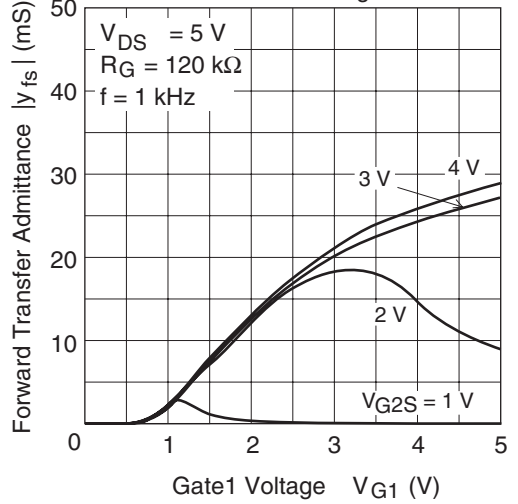
Typical Output Characteristics

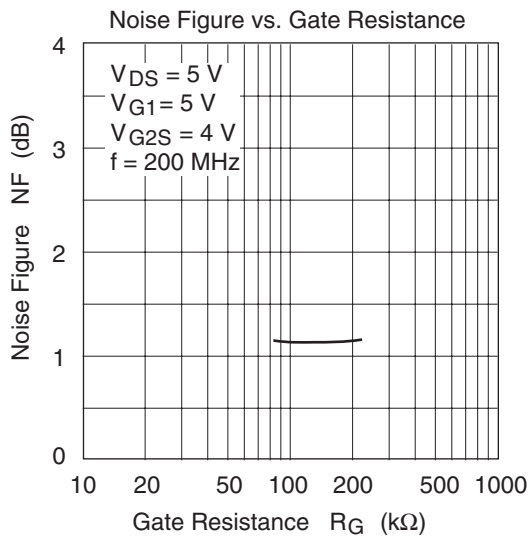
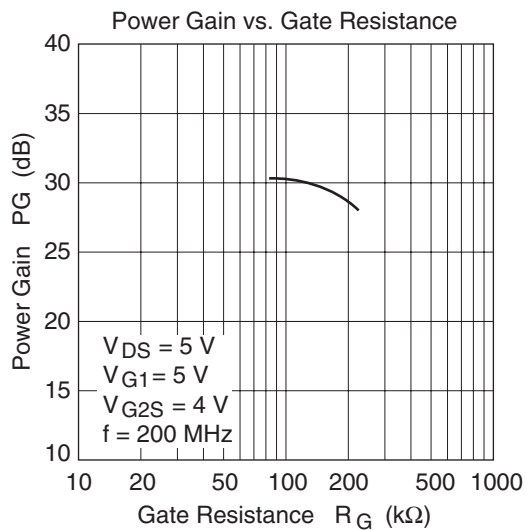
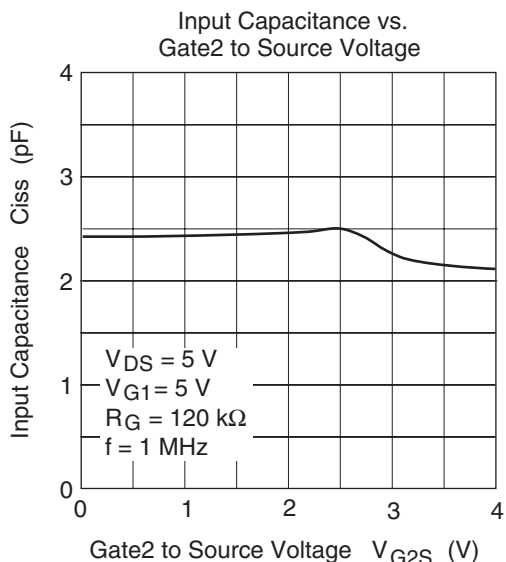
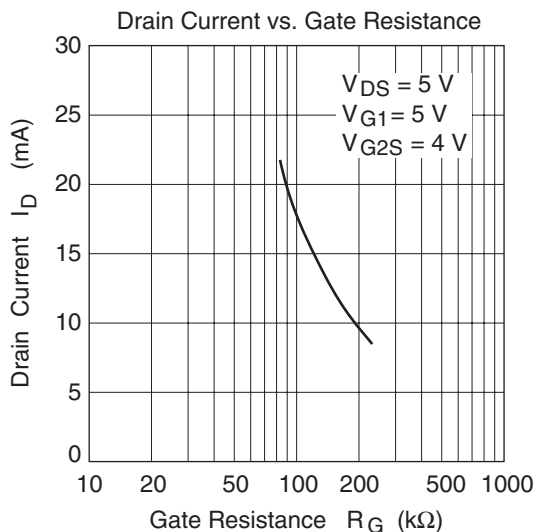


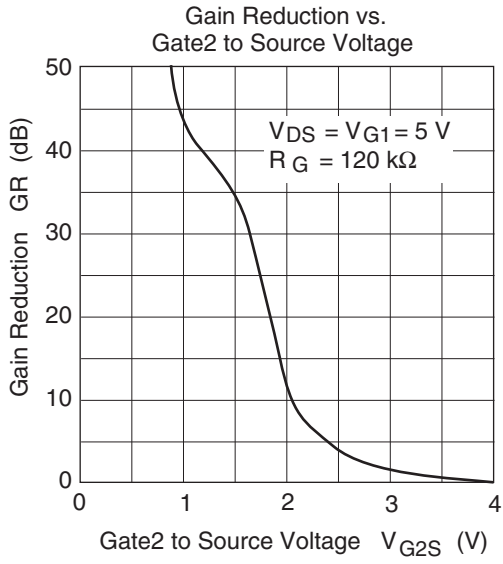
Drain Current vs. Gate1 Voltage



Forward Transfer Admittance vs. Gate1 Voltage





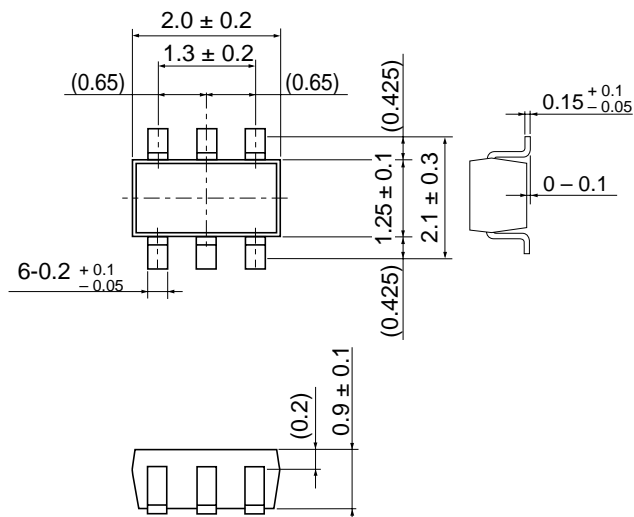




## Package Dimensions

As of July, 2002

Unit: mm



Hitachi Code	CMPAK-6
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

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