

# DATA SHEET

## **74LVC623A**

Octal transceiver with dual enable  
(3-State)

Product specification

1998 Jul 29

## Octal transceiver with dual enable (3-State)

## 74LVC623A

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- Flow-through pin-out architecture
- CMOS low power consumption
- Inputs accept voltages up to 5.5V
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

## DESCRIPTION

The 74LVC623A is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC623A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses.

The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels at the enable inputs (OEAB,  $\overline{\text{OEBA}}$ ). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OEAB and  $\overline{\text{OEBA}}$ . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The '623A' is identical to the '620A' but has true (non-inverting) outputs.

## QUICK REFERENCE DATA

GND = 0V;  $T_{\text{amb}} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{\text{PHL}}/t_{\text{PLH}}$	Propagation delay An to Bn; Bn to An	$C_L = 50\text{pF}$ $V_{\text{CC}} = 3.3\text{V}$	3.3	ns
$C_I$	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
$C_{\text{PD}}$	Power dissipation capacitance per latch	Notes 1, 2	32	pF

## NOTES:

- $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i + \sum (C_L \times V_{\text{CC}}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{\text{CC}}$  = supply voltage in V;  
 $\sum (C_L \times V_{\text{CC}}^2 \times f_o)$  = sum of the outputs.
- The condition is  $V_I = \text{GND}$  to  $V_{\text{CC}}$ .

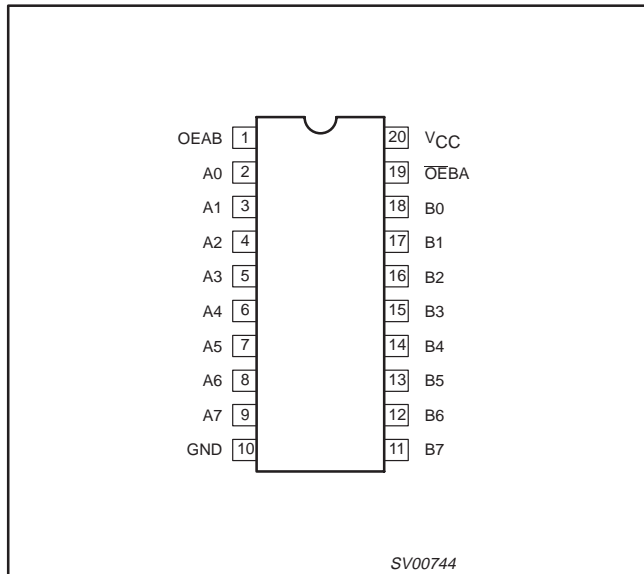
## ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	-40°C to +85°C	74LVC623A D	74LVC623A D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC623A DB	74LVC623A DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC623A PW	7LVC623APW DH	SOT360-1

# Octal transceiver with dual enable (3-State)

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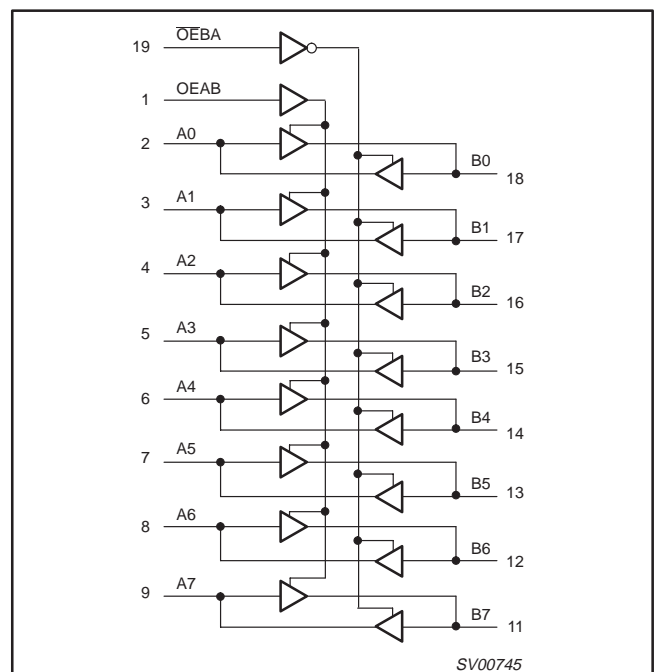
## PIN CONFIGURATION



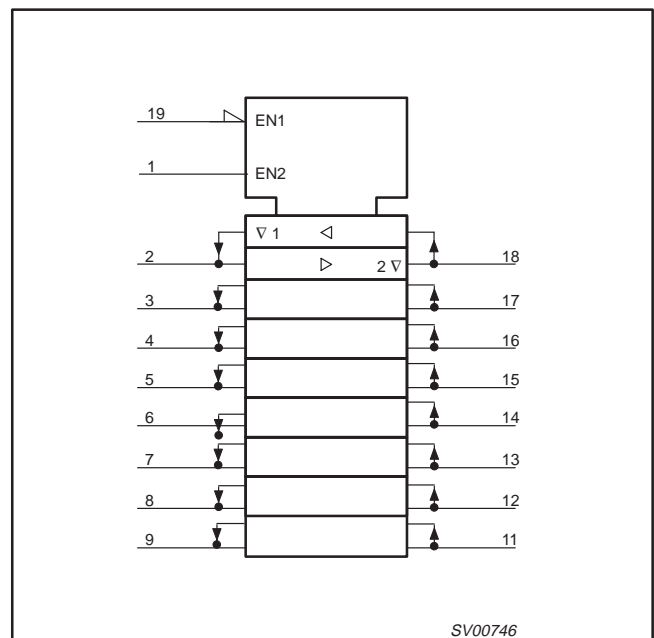
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs
10	GND	Ground (0V)
11, 12, 13, 14, 15, 16, 17, 18	B0 – B7	Data inputs/outputs
19	$\overline{OEBA}$	Output enable input (active LOW)
20	V <sub>CC</sub>	Positive supply voltage

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## Octal transceiver with dual enable (3-State)

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## FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
OEAB	OEBA	An	Bn
L	L	A=B	Inputs
H	H	Inputs	B=A
L	H	Z	Z
H	L	A=B Inputs	Inputs B=A

H = High voltage level

L = Low voltage level

Z = High impedance

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
V <sub>CC</sub>	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V <sub>I</sub>	DC input voltage range		0	5.5	V
V <sub>O</sub>	DC output voltage range; output HIGH or LOW state		0	V <sub>CC</sub>	V
	DC output voltage range; output 3-State		0	5.5	
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7V V <sub>CC</sub> = 2.7 to 3.6V	0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +6.5	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage	Note 2	-0.5 to +6.5	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	± 50	mA
V <sub>O</sub>	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to V <sub>CC</sub> + 0.5	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
I <sub>O</sub>	DC output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	± 50	mA
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		± 100	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C
P <sub>TOT</sub>	Power dissipation per package			
	- plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Octal transceiver with dual enable (3-State)

# 74LVC623A

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100µA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		GND	0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		± 0.1	± 5	µA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	± 5	µA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	± 10	µA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	µA

**NOTES:**

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

## AC CHARACTERISTICS

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V <sub>CC</sub> = 3.3V ± 0.3V			V <sub>CC</sub> = 2.7V		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay An to Bn, Bn to An	Figures 1, 4	1.5	2.3	6	1.5	7	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time OEAB to Bn	Figures 3, 4	1.5	4.6	7.6	1.5	8.6	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time OEAB to Bn	Figures 3, 4	1.5	4.0	6.5	1.5	7.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time OEBA to An	Figures 2, 4	1.5	4.4	7.9	1.5	8.9	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time OEBA to An	Figures 2, 4	1.5	3.7	6.5	1.5	7.5	ns

**NOTE:**

1. These typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

# Octal transceiver with dual enable (3-State)

74LVC623A

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$   
 $V_M = 0.5V \cdot V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL}$  at  $0.3V \geq 2.7V$   
 $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

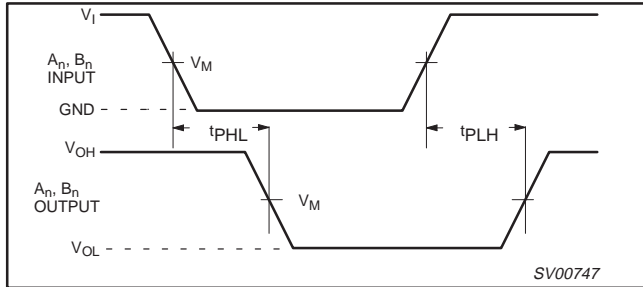


Figure 1. Input (An, Bn) to output (Bn, An) propagation delays.

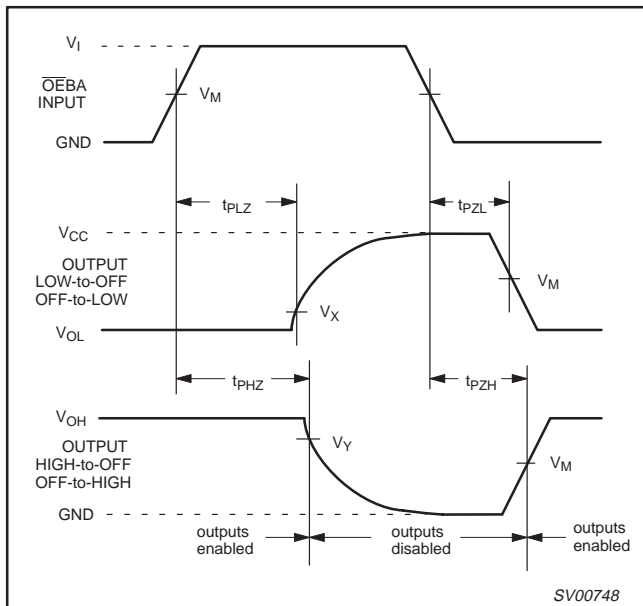


Figure 2. 3-State enable and disable times for OEBA input

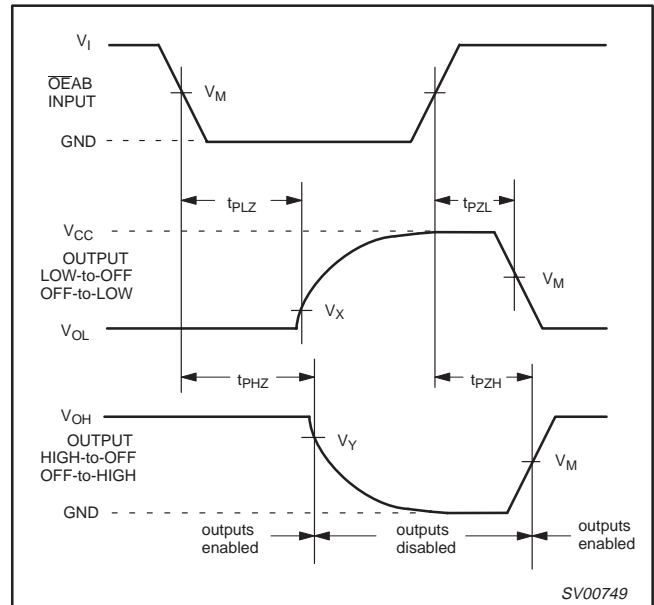


Figure 3. 3-State enable and disable times for OEAB input

## TEST CIRCUIT

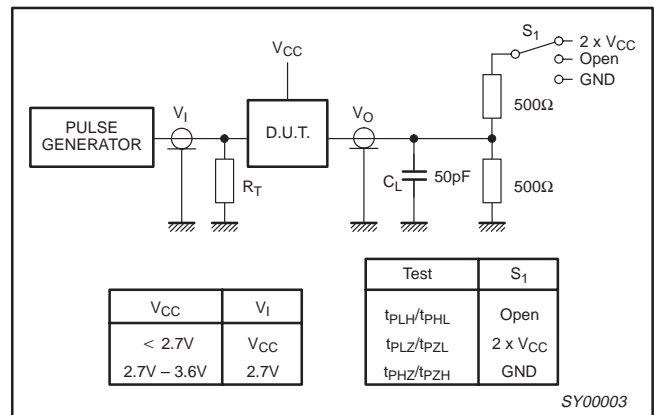


Figure 4. Load circuitry for switching times

# Octal transceiver with dual enable (3-State)

# 74LVC623A

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

# Octal transceiver with dual enable (3-State)

# 74LVC623A

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

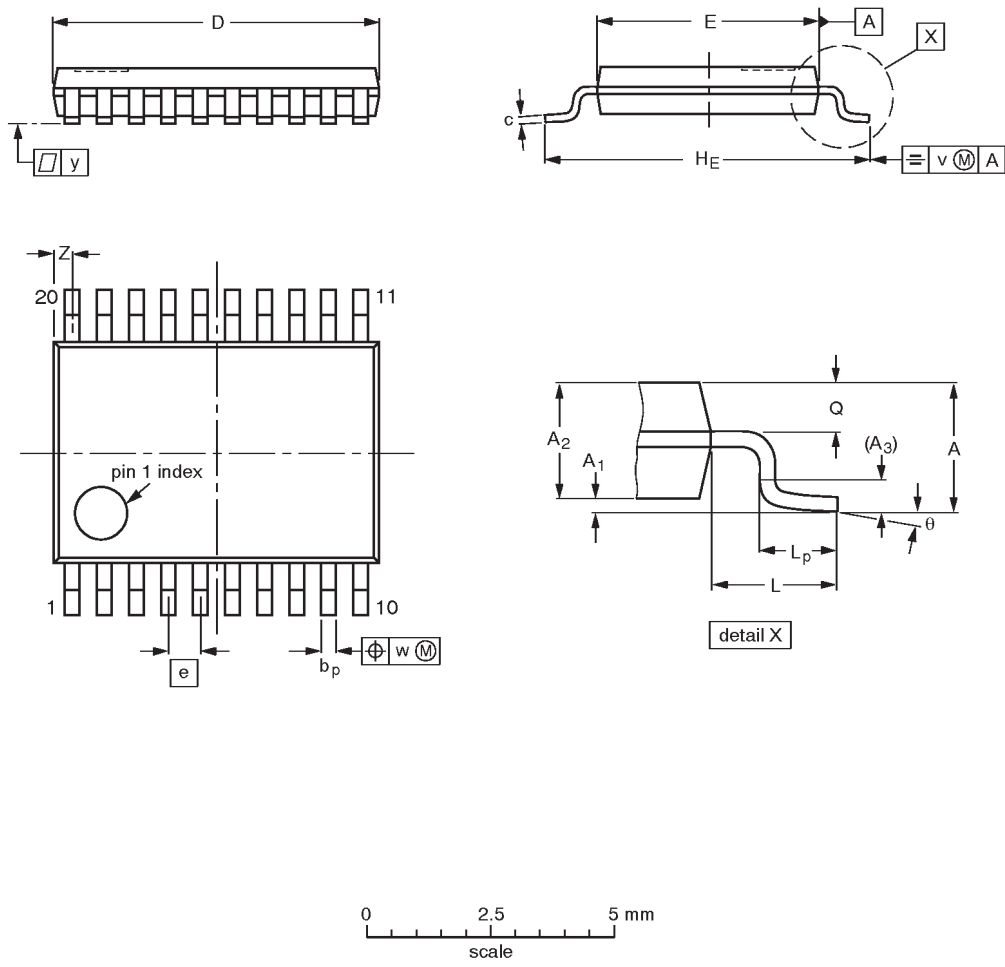


# Octal transceiver with dual enable (3-State)

# 74LVC623A

**TSSOP20:** plastic thin shrink small outline package; 20 leads; body width 4.4 mm

**SOT360-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16 95-02-04

## Octal transceiver with dual enable (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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