FUJITSU

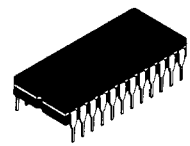
MOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB 8128-10
MB 8128-15

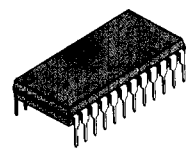
16384-BIT STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 8128 is a 16384 bit static random access memory organized as 2048 words by 8 bits. The MB 8128 is fabricated using N-channel silicon gate MOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

MB 8128 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. The MB 8128 is compatible with TTL logic families in all respects; inputs, outputs and a single +5V supply.



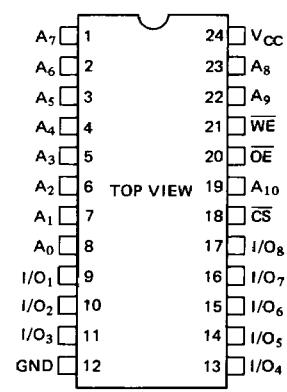
CERAMIC PACKAGE
(CERDIP)
DIP-24C-C01



PLASTIC PACKAGE
DIP-24P-M01

- 2048 words x 8 bits organization
- Static operation: no clocks or refresh required
- Fast access time : 100ns max. (MB 8128-10)
  : 150ns max. (MB 8128-15)
- Single +5V supply, ±10% tolerance
- Common data input/output
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 24 pin DIP package

PIN ASSIGNMENT



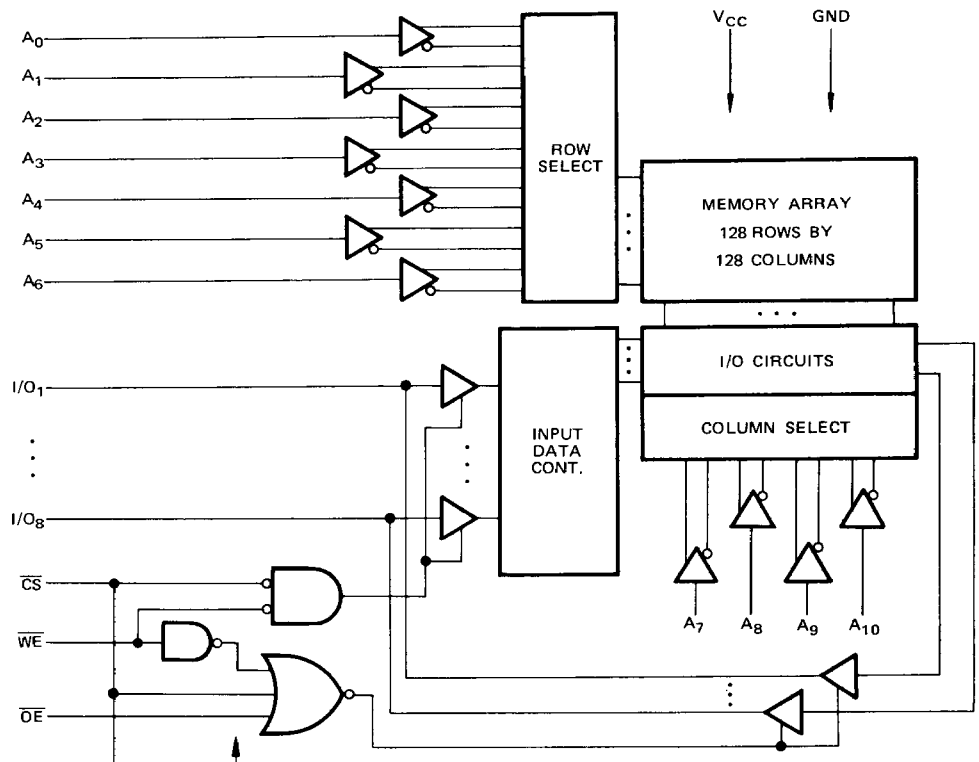
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin with respect to GND		V_{IN}, V_{OUT}, V_{CC}	-3.5 to +7	V
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-40 to +125	
Power Dissipation		P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 8128 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)*	C_{IN}	–	5	pF
Input/Output Capacitance ($V_{I/O}$ = 0V)*	$C_{I/O}$	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0[2]	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	6.0	V	

Note: 1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.
2) −3.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = −0.5 V at DC level).

DC CHARACTERISTICS

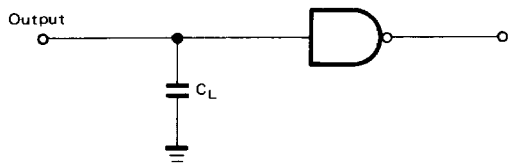
(Recommended operating conditions unless otherwise noted.)

Parameter			Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = GND to V_{CC}, V_{CC} = Max.)			$\|I_{LI}\|$			10	μA
Input/Output Leakage Current ($\overline{CS}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}, V_{CC} = Max.)			$\|I_{LO}\|$			10	μA
Power Supply Current (V_{CC} = Max., $\overline{CS}$ = V_{IL}, $I_{I/O}$ = Open)	T_A = 25°C	MB 8128-10	I_{CC}		70		mA
		MB 8128-15			50		
	T_A = 0°C	MB 8128-10				100	
		MB 8128-15				70	
Output Low Voltage (I_{OL} = 2.1 mA)			V_{OL}			0.4	V
Output High Voltage (I_{OH} = -1.0 mA)			V_{OH}	2.4			V
Standby Current (V_{CC} = Min. to Max., $\overline{CS}$ = V_{IH})		MB 8128-10	I_{SB}		8	20	mA
		MB 8128-15			6	15	
Peak Power-On Current (V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.)		MB 8128-10	I_{PO}			20	mA
		MB 8128-15				15	

Note: A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselacted. Otherwise, power-on current approaches I_{CC} active.

Fig. 2 – AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.4V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V
Output Load :	1 TTL Gate and C_L = 100 pF



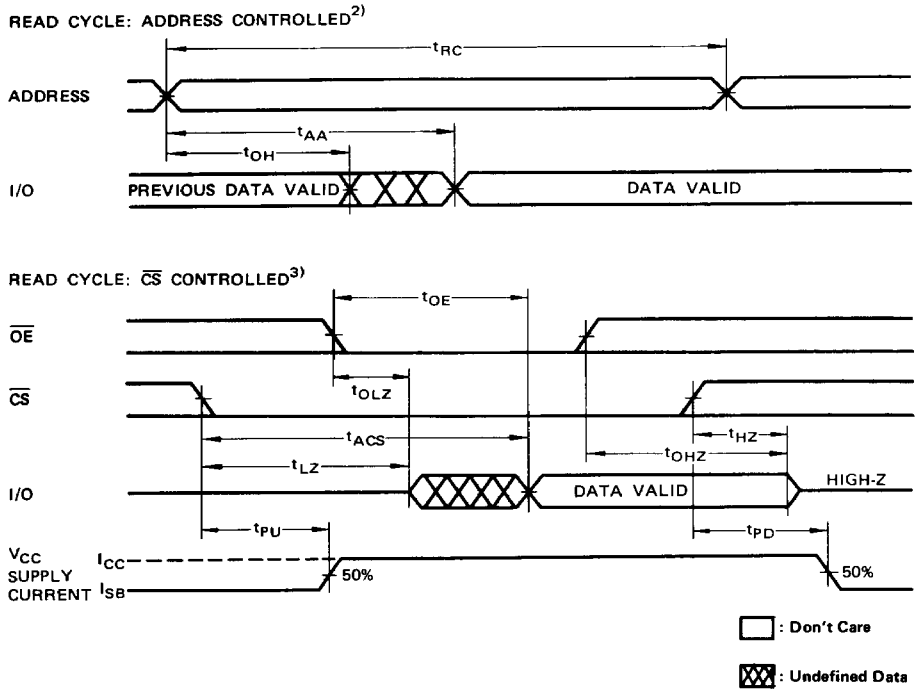
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB 8128-10			MB 8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle Time	t_{RC}	100			150			ns
Address Access Time	t_{AA}			100			150	ns
Chip Select Access Time	t_{ACS}			100			150	ns
Output Hold from Address Change	t_{OH}	15			20			ns
Chip Select to Output Active	t_{LZ}	0			0			ns
Chip Select to Output in High Z	t_{HZ}			40			60	ns
Output Enable to Output Valid	t_{OE}			50			60	ns
Output Enable to Output Active	t_{OLZ}	10			10			ns
Output Enable to Output in High Z	t_{OHZ}			40			60	ns
Chip Select to Power Up Time	t_{PU}	0			0			ns
Chip Select to Power Down Time	t_{PD}			40			60	ns

READ CYCLE TIMING DIAGRAM[1]

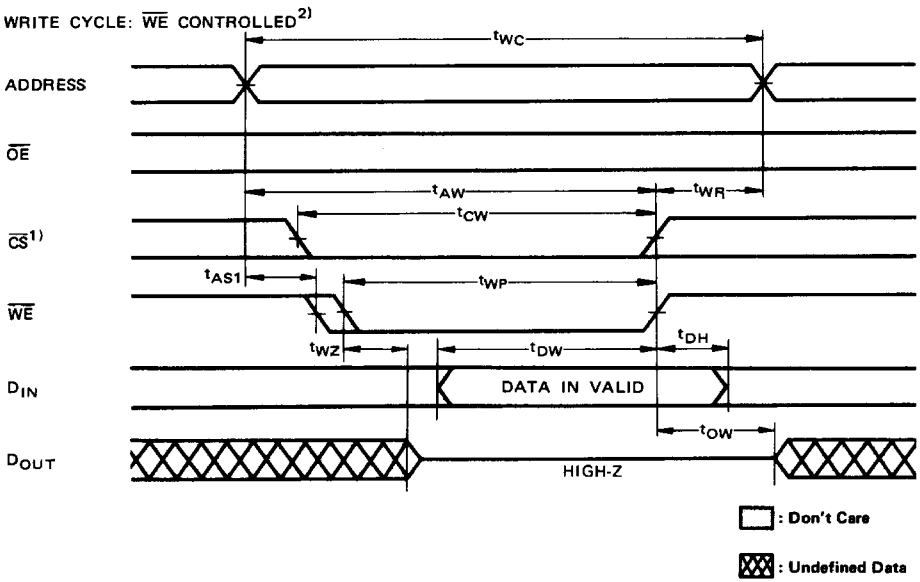


Note: 1) $\overline{WE}$ is high for Read Cycle.
2) Device is continuously selected, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$.
3) Addresses valid prior to or coincident with $\overline{CS}$ transition low.

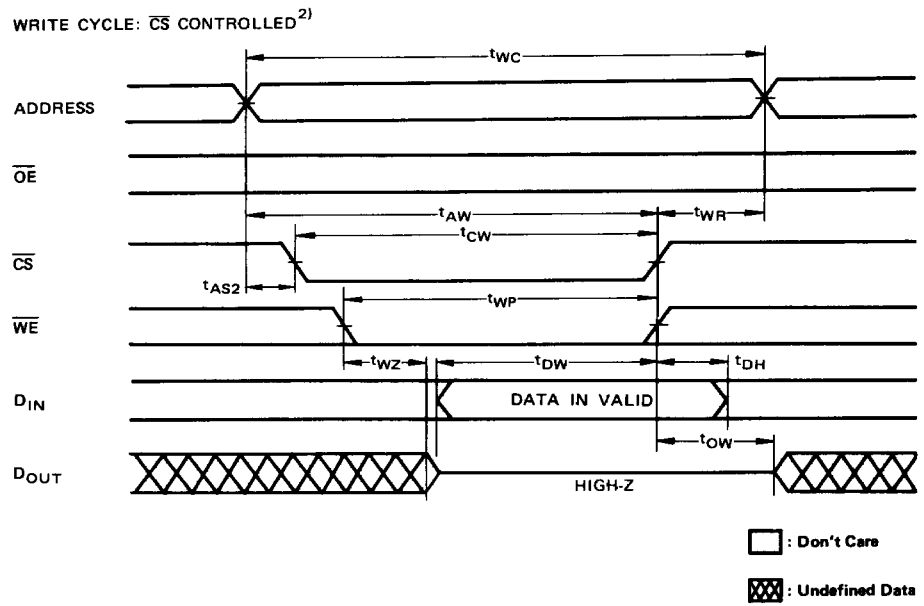
WRITE CYCLE

Parameter	Symbol	MB 8128-10			MB 8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	t_{WC}	100			150			ns
Address Valid to End of Write	t_{AW}	95			140			ns
Chip Select to End of Write	t_{CW}	95			140			ns
Data Valid to End of Write	t_{DW}	40			60			ns
Data Hold Time	t_{DH}	5			5			ns
Write Pulse Width	t_{WP}	85			130			ns
Write Recovery Time	t_{WR}	5			10			ns
Address Setup Time	t_{AS1}	0			0			ns
	t_{AS2}	0			0			ns
Output Active From End of Write	t_{OW}	10			10			ns
Write Enabled to Output in High Z	t_{WZ}			40			60	ns

WRITE CYCLE TIMING DIAGRAM



WRITE CYCLE TIMING DIAGRAM (Cont'd)



Note: 1) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ low, the outputs remain in a high impedance state.
2) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

DESCRIPTION

The MB 8128 from Fujitsu is high performance part. This is designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MB 8128 chip select (active low). The MB 8128 automatically enters standby drawing only I_{SB} whenever the chip select is high. Upon activation of chip select ($\overline{CS}$ = LOW) the MB 8128 automatically powers up and draws I_{CC}.

This automatic power up/down is an extremely useful feature. However, care must be used as proper decoupling and PC board layout is required to minimize power line glitches.

PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

PACKAGE DIMENSIONS