

Low Power Quad Operational Amplifier

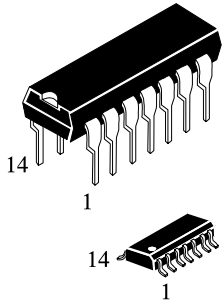
IL2902

The IL2902 contains four independent high gain operational amplifiers with internal frequency compensation. The four op-amps operate over a wide voltage range from a single power supply. Also use a split power supply. The device has low power supply current drain, regardless of the power supply voltage. The low power drain also makes the IL2902 a good choice for battery operation.

When your project calls for a traditional op-amp function, now you can streamline your design with a simple single power supply. Use ordinary +5VDC common to practically any digital system or personal computer application, without requiring an extra 15V power supply just to have the interface electronics you need.

The IL2902 is a versatile, rugged workhorse with a thousand-and-one uses, from amplifying signals from a variety of transducers to dc gain blocks, or any op-amp function. The attached pages offer some recipes that will have your project cooking in no time.

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range:
3V ~ 32V (or $\pm 1.5V \sim \pm 16V$)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to $V_{CC}-1.5V$ DC
- Power drain suitable for battery operation
- Low input offset voltage and offset current
- Differential input voltage range equal to the power supply voltage

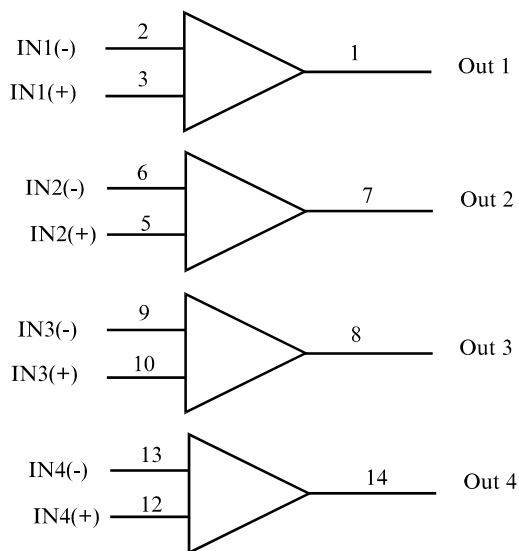


N SUFFIX
PLASTIC

D SUFFIX
SOIC

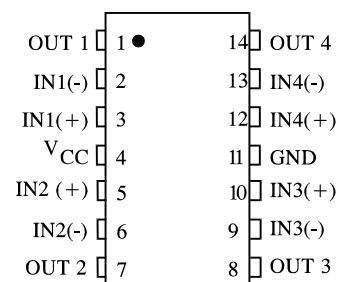
ORDERING INFORMATION
 IL2902N Plastic
 IL2902D SOIC
 $T_A = -40^\circ$ to $+85^\circ$ C
 for all packages.

LOGIC DIAGRAM



PIN 4 = V_{CC}
 PIN 11 = GND

PIN ASSIGNMENT



MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|-------------|------|
| V _{CC} | Power Supply Voltages Single Supply Split Supplies | 32 ±16 | V |
| V _{IDR} | Input Differential Voltage Range (1) | ±32 | V |
| V _{ICR} | Input Common Mode Voltage Range | -0.3 to 32 | V |
| I _{SC} | Output Short Circuit Duration | Continuous | |
| T _J | Junction Temperature Plastic Packages | 150 | °C |
| T _{stg} | Storage Temperature Plastic Packages | -55 to +125 | °C |
| I _{IN} | Input Current, per pin (2) | 50 | mA |
| T _L | Lead Temperature, 1mm from Case for 10 Seconds | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

Notes:

1. Split Power Supplies.
2. V_{IN}<-0.3V. This input current will only exist when voltage at any of the input leads is driven negative.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-----------------|--|----------------|--------------|------|
| V _{CC} | DC Supply Voltage | ±2.5 or 5.0 | ±15 or 30 | V |
| T _A | Operating Temperature, All Package Types | -40 | +85 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS ($T_A=-40$ to $+85^\circ\text{C}$)

| Symbol | Parameter | Test Conditions | Guaranteed Limit | | | Unit |
|--------------------------|---|---|------------------|-----|-------------|------------------------------|
| | | | Min | Typ | Max | |
| V_{IO} | Maximum Input Offset Voltage | $V_O=1.4V$ $V_{CC}=5.0-30V$; $R_S=0\Omega$ $V_{ICM}=0V$ to $V_{CC}-1.7V$ | | | 9.0 5.0* | mV |
| $\Delta V_{IO}/\Delta T$ | Input Offset Voltage Drift | $R_S=0\Omega$, $V_{CC}=30V$ | | 7.0 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IO} | Maximum Input Offset Current | $V_{CC}=5.0V$ | | | 150 50* | nA |
| $\Delta I_{IO}/\Delta T$ | Input Offset Current Drift | $R_S=0\Omega$, $V_{CC}=30V$ | | 10 | | $\text{pA}/^\circ\text{C}$ |
| I_{IB} | Maximum Input Bias Current | $V_{CC}=5.0V$ | | | 500 250* | nA |
| V_{ICR} | Input Common Mode Voltage Range | $V_{CC}=30V$ | 0 | | 28 | V |
| I_{CC} | Maximum Power Supply Current | $R_L=\infty$, $V_{CC}=30V$, $V_0=0V$ $R_L=\infty$, $V_{CC}=5V$, $V_0=0V$ | | | 3 1.2 | mA |
| A_{VOL} | Minimum Large Signal Open-Loop Voltage Gain | $V_{CC}=15V$, $R_L \geq 2K\Omega$ | 15 25* | | | V/mV |
| V_{OH} | Minimum Output High-Level Voltage Swing | $V_{CC}=30V$, $R_L=2K\Omega$ $V_{CC}=30V$, $R_L=10K\Omega$ | 26 27 | | | V |
| V_{OL} | Maximum Output Low-Level Voltage Swing | $V_{CC}=5V$, $R_L=10K\Omega$ | | | 20 | mV |
| CMR | Common Mode Rejection | $V_{CC}=30V$, $R_S=10K\Omega$ | 65* | | | dB |
| PSR | Power Supply Rejection | $V_{CC}=30V$ | 65* | | | dB |
| CS | Channel Separation | $f=1\text{KHz}$ to 20KHz , $V_{CC}=30V$ | -120* | | | dB |
| I_{SC} | Maximum Output Short Circuit to GND | $V_{CC}=5.0V$ | | | 60* | mA |
| I_{source} | Minimum Output Source Current | $V_{IN+}=1V$, $V_{IN-}=0V$, $V_{CC}=15V$, $V_0=0V$ | 10 | | | mA |
| I_{sink} | Minimum Output Sink Current | $V_{IN+}=0V$, $V_{IN-}=1V$, $V_{CC}=15V$, $V_0=15V$ $V_{IN+}=0V$, $V_{IN-}=1V$, $V_{CC}=15V$, $V_0=0.2V$ | 5 10* 12* | | | mA μA |
| V_{IDR} | Differential Input Voltage Range | All $V_{IN} \geq \text{GND}$ or V-Supply (if used) | | | V_{CC}^* | V |

*= $@25^\circ\text{C}$

TYPICAL PERFORMANCE CHARACTERISTICS

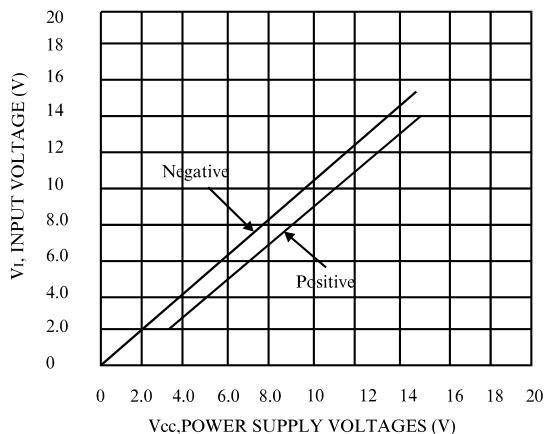


Figure 1. Input Voltage Range

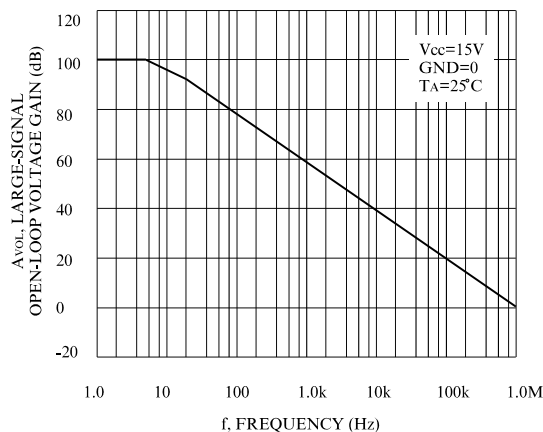


Figure 2. Open-Loop Frequency

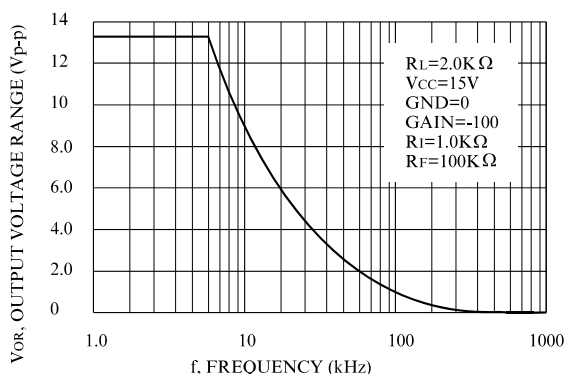


Figure 3. Large-Signal Frequency Response

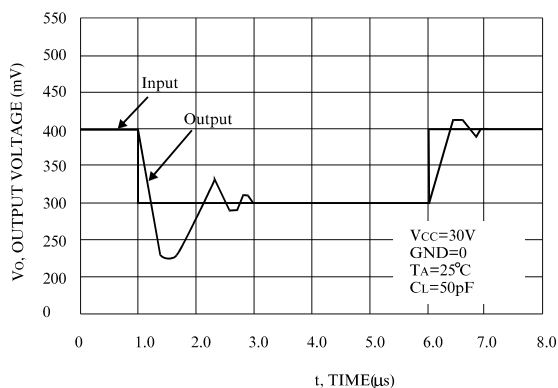


Figure 4. Small-Signal Voltage Follower Pulse Response (Noninverting)

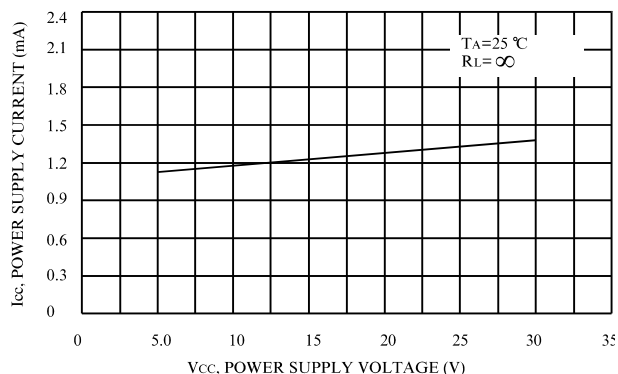


Figure 5. Power Supply Current versus Power Supply Voltage

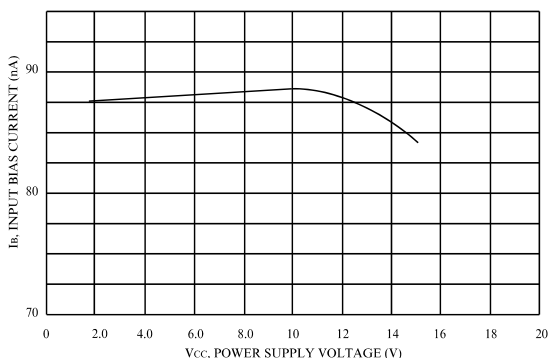
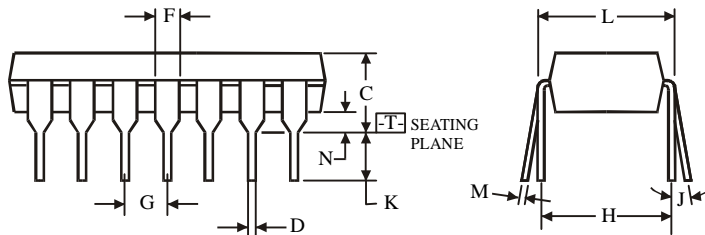
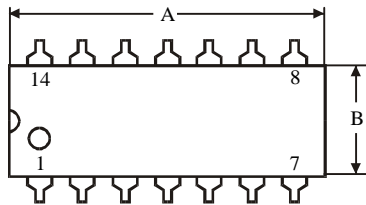
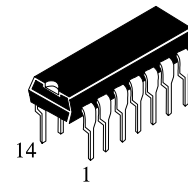


Figure 6. Input Bias Current versus Power Supply Voltage

**N SUFFIX PLASTIC DIP
(MS - 001AA)**



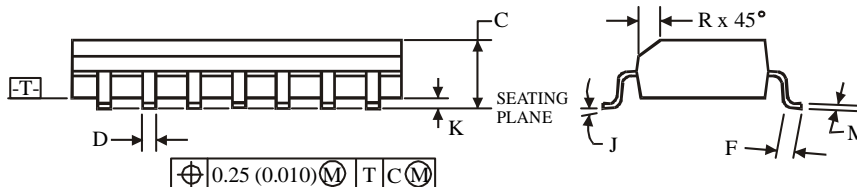
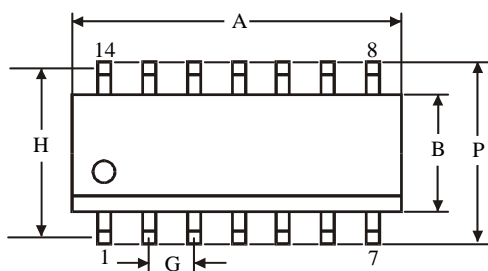
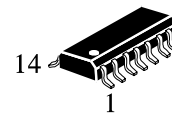
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|-------|
| | MIN | MAX |
| A | 18.67 | 19.69 |
| B | 6.1 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.2 | 0.36 |
| N | 0.38 | |

**D SUFFIX SOIC
(MS - 012AB)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side
for A; for B - 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|------|
| | MIN | MAX |
| A | 8.55 | 8.75 |
| B | 3.8 | 4 |
| C | 1.35 | 1.75 |
| D | 0.33 | 0.51 |
| F | 0.4 | 1.27 |
| G | 1.27 | |
| H | 5.27 | |
| J | 0° | 8° |
| K | 0.1 | 0.25 |
| M | 0.19 | 0.25 |
| P | 5.8 | 6.2 |
| R | 0.25 | 0.5 |