

Data Sheet March 1999 File Number 1827.3

13A, 500V, 0.400 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17435.

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF450	TO-204AA	IRF450

NOTE: When ordering, include the entire part number.

Features

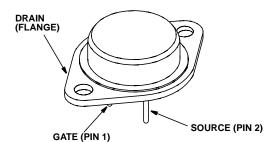
- 13A, 500V
- $r_{DS(ON)} = 0.400\Omega$
- Single Pulse Avalanche Energy Rated
- · SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- · Linear Transfer Characteristics
- · High Input Impedance
- · Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-204AA



Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	IRF450	UNITS
Drain to Source Voltage (Note 1)V _{DS}	500	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	500	V
Continuous Drain Current	13	Α
$T_C = 100^{\circ}C$	8.1	Α
Pulsed Drain Current (Note 3)	52	Α
Gate to Source Voltage	±20	V
Maximum Power Dissipation	125	W
Linear Derating Factor	1.2	W/oC
Single Pulse Avalanche Energy Rating (Note 4)	860	mJ
Operating and Storage Temperature	-55 to 150	оС
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10sT _L	300	°C
Package Body for 10s, See Techbrief 334	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}C$ to $125^{\circ}C$.

Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0V, I_D = 250\mu A \text{ (Figure 10)}$	500	-	-	V
Gate to Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.0	-	4.0	V
Gate to Source Leakage	I _{GSS}	$V_{GS} = \pm 20V$	-	-	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = Rated BV _{DSS} , V_{GS} = 0V V_{DS} = 0.8 x Rated BV _{DSS} , V_{GS} = 0V, T_{J} = 125°C		-	25	μΑ
				-	250	μΑ
On-State Drain Current (Note 2)	I _{D(ON)}	$V_{DS} > I_{D(ON) \times r_{DS(ON)MAX}}, V_{GS} = 10V \text{ (Figure 7)}$	13	-	-	Α
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	V _{GS} = 10V, I _D = 7.2A (Figures 8, 9)	-	0.3	0.400	Ω
Forward Transconductance (Note 2)	9 _{fs}	$V_{DS} \ge 50V$, $I_D = 7.2A$ (Figure 12)	6.0	11	-	S
Turn-On Delay Time	t _{d(ON)}	$V_{DD} = 250 \text{V}, \text{ I}_{D} \approx 13 \text{A}, \text{ R}_{G} = 6.2 \Omega, \text{ R}_{L} = 19 \Omega$ (Figures 17, 18) MOSFET SwitchingTimes are Essentially Independent of Operating Temperature		20	27	ns
Rise Time	t _r			40	66	ns
Turn-Off Delay Time	t _{d(OFF)}			72	100	ns
Fall Time	t _f			35	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{g(TOT)}	$\begin{split} &V_{GS} = 10\text{V, I}_D = 13\text{A, V}_{DS} = 0.8 \text{ x Rated BV}_{DSS}, \\ &I_{g(REF)} = 1.5\text{mA (Figures 14, 19, 20) Gate Charge} \\ &\text{is Essentially Independent of Operating} \\ &-\text{Temperature} \end{split}$		85	130	nC
Gate to Source Charge	Q _{gs}			12	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			42	-	nC
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz (Figure 11)		1800	-	pF
Output Capacitance	Coss			400	-	pF
Reverse Transfer Capacitance	C _{RSS}			100	-	pF
Internal Drain Inductance	L _D	Measured between the Contact Screw on the Flange that is Closer to Source and Gate Pins and the Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances	-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the Source Lead, 6mm (0.25in) from the Flange to Source Bonding Pad	-	12.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$,	-	-	0.83	°C/W
Thermal Resistance Junction to Ambient	R _{0JA}	Free Air Operation		-	30	°C/W

2

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I _{SD}	Modified MOSFET	Q D	-	-	13	Α
Pulse Source to Drain Current (Note 3)	^I SDM	Symbol Showing the Integral Reverse P-N Junction Diode	G S S	-	-	52	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}C$, $I_{SD} = 13A$, $V_{GS} = 0V$ (Figure 13)		-	-	1.4	V
Reverse Recovery Time	t _{rr}	$T_J = 25^{\circ}C$, $I_{SD} = 13A$, $dI_{SD}/dt = 100A/\mu s$		280	600	1200	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^{o}C$, $I_{SD} = 13A$, $dI_{SD}/dt = 100A/\mu s$		3.2	7.5	14	μС

NOTES:

- 2. Pulse test: pulse width $\leq 300 \mu s,$ duty cycle $\leq 2\%.$
- 3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
- 4. V_{DD} = 25V, starting T_J = 25°C, L = 9.2mH, R_G = 25 Ω , peak I_{AS} = 13A. See Figures 14, 15.

Typical Performance Curves Unless Otherwise Specified

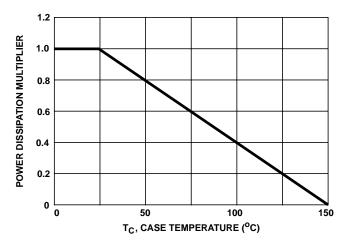


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

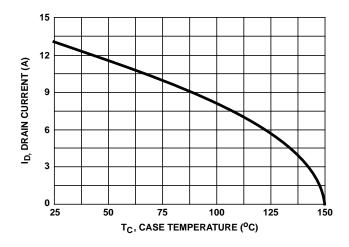


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

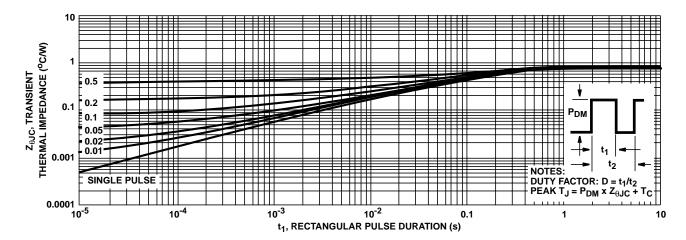


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

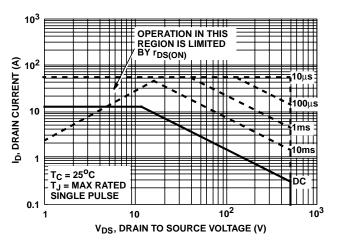


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

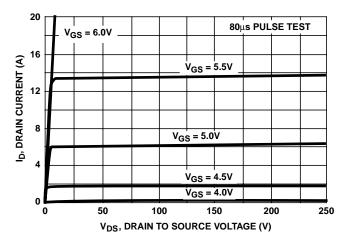


FIGURE 5. OUTPUT CHARACTERISTICS

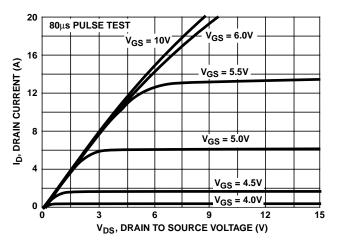


FIGURE 6. SATURATION CHARACTERISTICS

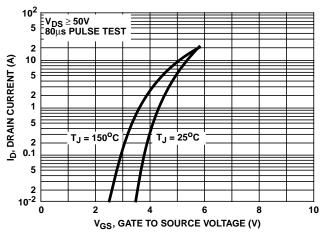


FIGURE 7. TRANSFER CHARACTERISTICS

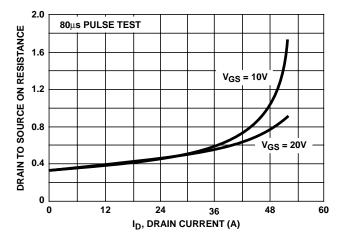


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

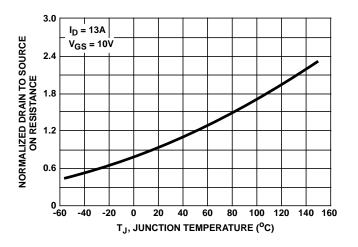


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

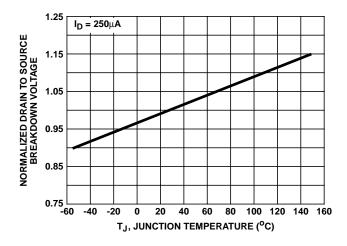


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

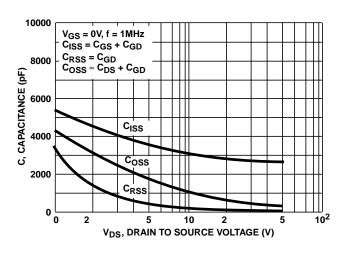


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

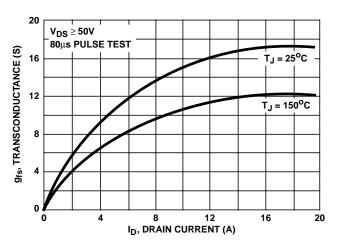


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

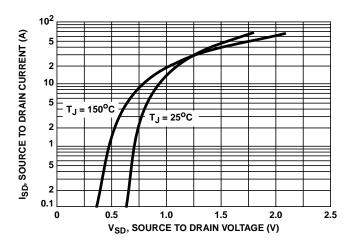


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

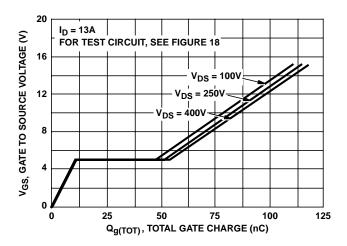


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

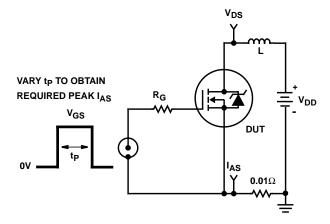


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

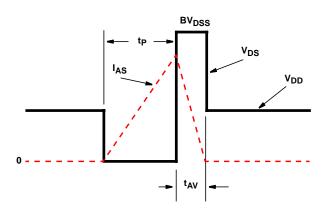


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

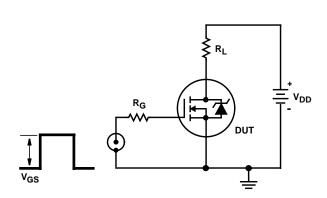


FIGURE 17. SWITCHING TIME TEST CIRCUIT

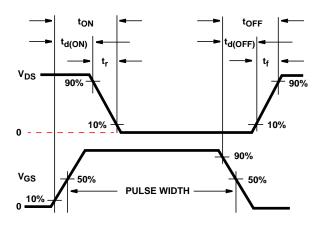


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

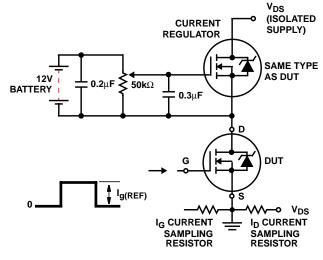


FIGURE 19. GATE CHARGE TEST CIRCUIT

6

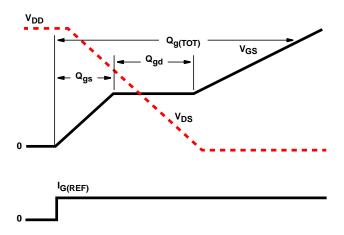


FIGURE 20. GATE CHARGE WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation P. O. Box 883, Mail Stop 53-204 Melbourne, FL 32902 TEL: (407) 724-7000

FAX: (407) 724-7240

EUROPE

Intersil SA Mercure Center 100, Rue de la Fusee 1130 Brussels, Belgium TEL: (32) 2.724.2111 FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd. 7F-6, No. 101 Fu Hsing North Road Taipei, Taiwan Republic of China TEL: (886) 2 2716 9310 FAX: (886) 2 2715 3029