GLT41016

64K X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Feb 2004 (Rev 2.2)

Features :

* 65,536 words by 16 bits organization.
* Fast access time and cycle time.
* Dual $\overline{CAS}$ Input.
* Low power dissipation.
* Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
* 256 refresh cycles per 4ms.
* Available in 40-pin 400 mil SOJ and 40/44 pin TSOP (II).
* Single 5.0V±10% Power Supply.
* All inputs and Outputs are TTL compatible.
* Extended Data-Out(EDO) Page Mode operation.

Description :

The GLT41016 is a 65,536 x 16 bit high-performance CMOS dynamic random access memory. The GLT41016 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The GLT41016 accepts 256-cycle refresh in 4ms interval.

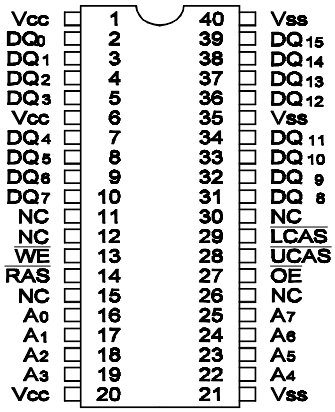
All inputs are TTL compatible. EDO Page Mode operation allows random access up to 256 x 16 bits, within a page, with cycle times as short as 12ns.

The GLT41016 is best suited for graphics, and DSP applications requiring high performance memories.

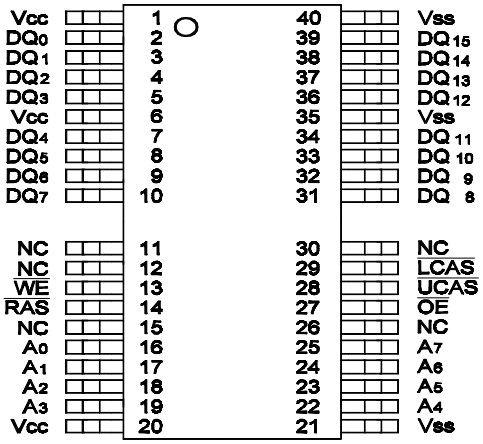
HIGH PERFORMANCE	30	35	40	45
Max. $\overline{RAS}$ Access Time, (t_{RAC})	30 ns	35 ns	40 ns	45 ns
Max. Column Address Access Time, (t_{AA})	15 ns	18 ns	20 ns	22 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	12 ns	13 ns	15 ns	18 ns
Min. Read/Write Cycle Time, (t_{RC})	65 ns	70 ns	75 ns	80 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	10 ns	11 ns	12 ns	12 ns

Pin Configuration :

GLT41016
SOJ Top View



TSOP(Type II)
Top View



Pin Descriptions:

Name	Function
A_0 - A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_{15}	Data Inputs / Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....-0°C to +70°C
Storage Temperature(plastic)....-55°C to +150°C
Voltage Relative to V_{SS}.....-1.0V to + 7.0V
Short Circuit Output Current.....50mA
Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=5V±10%, V_{SS}=0V

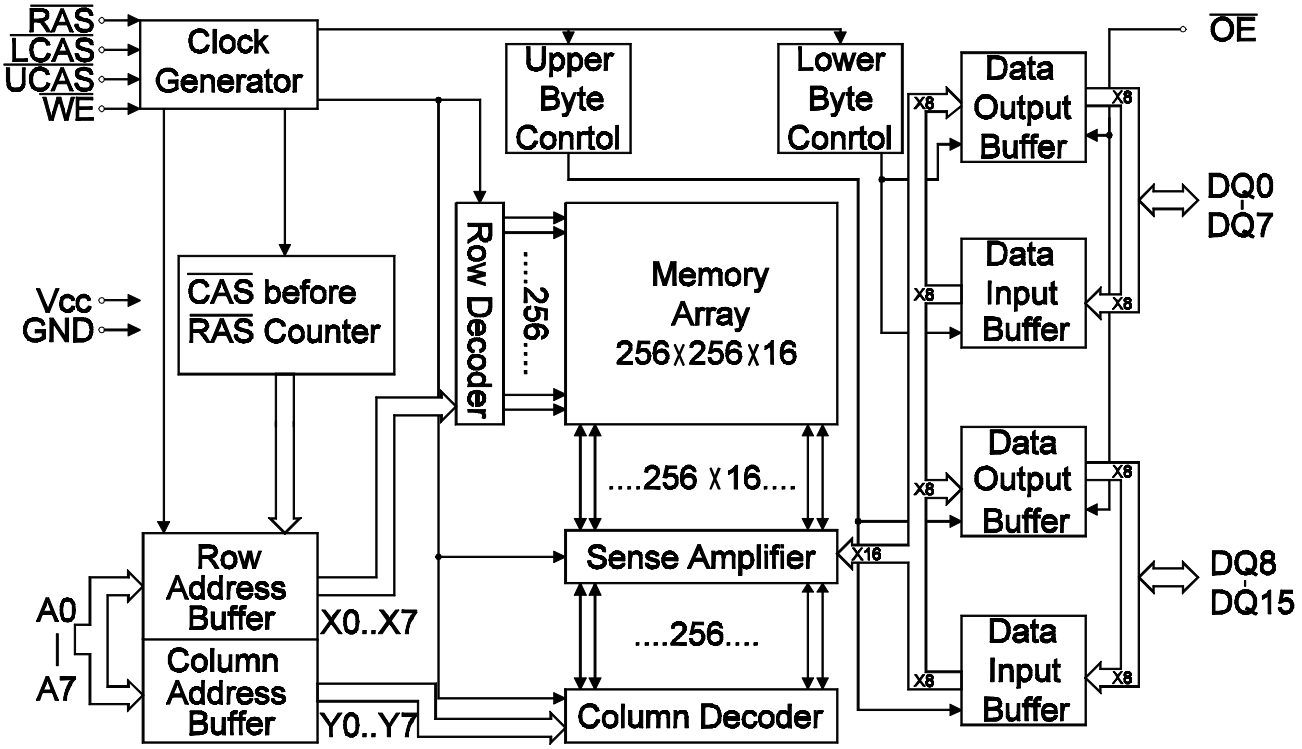
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/ Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Extended Data Output (EDO) Page Mode

The EDO page mode is a kind of page mode with enhanced features. The two major features of the EDO page mode are as follows.

1. Data output time is extended.

In the EDO page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the EDO page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the EDO page mode, the timing margin in read cycle is larger than of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the EDO page mode is shorter than that in the fast page mode.

In the EDO page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60ns as an example, the $\overline{CAS}$ cycle time in the EDO page mode is 25ns while that in the fast page mode is 40ns.

In the EDO page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The EDO page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Truth Table: GLT41016

Function		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESS	DQs	Notes
Standby		H	H→X	H→X	X	X		High-Z	
Read: Word		L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte,Data-Out Upper Byte,High-Z	
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte,High-Z Upper Byte,Data-Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	H	L	L	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L	H→L	H	L	COL	Data-Out	1
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	H→L	L	X	COL	Data-In	2
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
$\overline{RAS}$ -Only Refresh		L	H	H	X	X	ROW	High-Z	
CBR Refresh		H→L	L	L	X	X		High-Z	4

Notes:

1. These READ cycles may also be BYTE READ cycles (either $\overline{UCAS}$ or $\overline{LCAS}$ active).
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{UCAS}$ or $\overline{LCAS}$ active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active ($\overline{UCAS}$ or $\overline{LCAS}$).

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ 5.5V (All other pins not under test=0V)		-10		+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ 5.5V Output is disabled (Hiz)		-10		+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} other inputs ≥V_{SS}				4	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$ -Only	$\overline{RAS}$ cycling, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{PC} = t_{PC}(min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	1,2
I_{CC5}	Refresh Current, CAS Before $\overline{RAS}$	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{RC} = t_{RC} (min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥V_{CC}-0.2V, $\overline{UCAS}$ ≥V_{CC}-0.2V, $\overline{LCAS}$ ≥V_{CC}-0.2V, All other inputs V_{SS}				2	mA	
V_{IL}	Input Low Voltage			-1		+0.8	V	3
V_{IH}	Input High Voltage			2.4		V_{CC}+1	V	3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5mA		2.4			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified ICC(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
3. Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to -1.0V for a period not to exceed 20ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.

AC Characteristics

T_A = 0°C to 70°C , V_{CC} = 5 V ± 10%, VIH/VIL = 2.4/0.8 V, V_{OH}/V_{OL} = 2.0/0.8V

An initial pause of 100 μs and 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles are required after power-up.

Parameter	Symbol	30		35		40		45		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	65		70		75		80		ns	
Read Modify Write Cycle Time	t_{RWC}	90		95		100		103		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	25		25		25		30		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	30	100k	35	100k	40	100k	45	100k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		30		35		40		45	ns	1,2,3
Access Time from $\overline{CAS}$	t_{CAC}		10		11		12		12	ns	1,5,10
Access Time from Column Address	t_{AA}		15		18		20		22	ns	1,5,6
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	0		0		0		0		ns	
$\overline{CAS}$ to Output High-Z	t_{CEZ}	3	8	3	8	3	8	3	8	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10		12		12		13		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	7		8		8		9		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	25		30		34		40		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	6	10k	6	10k	6	10k	7	10k	ns	
$\overline{RAS}$ to CAS Delay Time	t_{RCD}	13	20	17	24	18	28	18	33	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	10	15	12	17	13	20	13	23	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	6		7		8		8		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	6		6		6		6		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	15		18		20		23		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	26		30		34		39		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	6		6		6		6		ns	
Write Command Pulse Width	t_{WP}	6		6		6		6		ns	

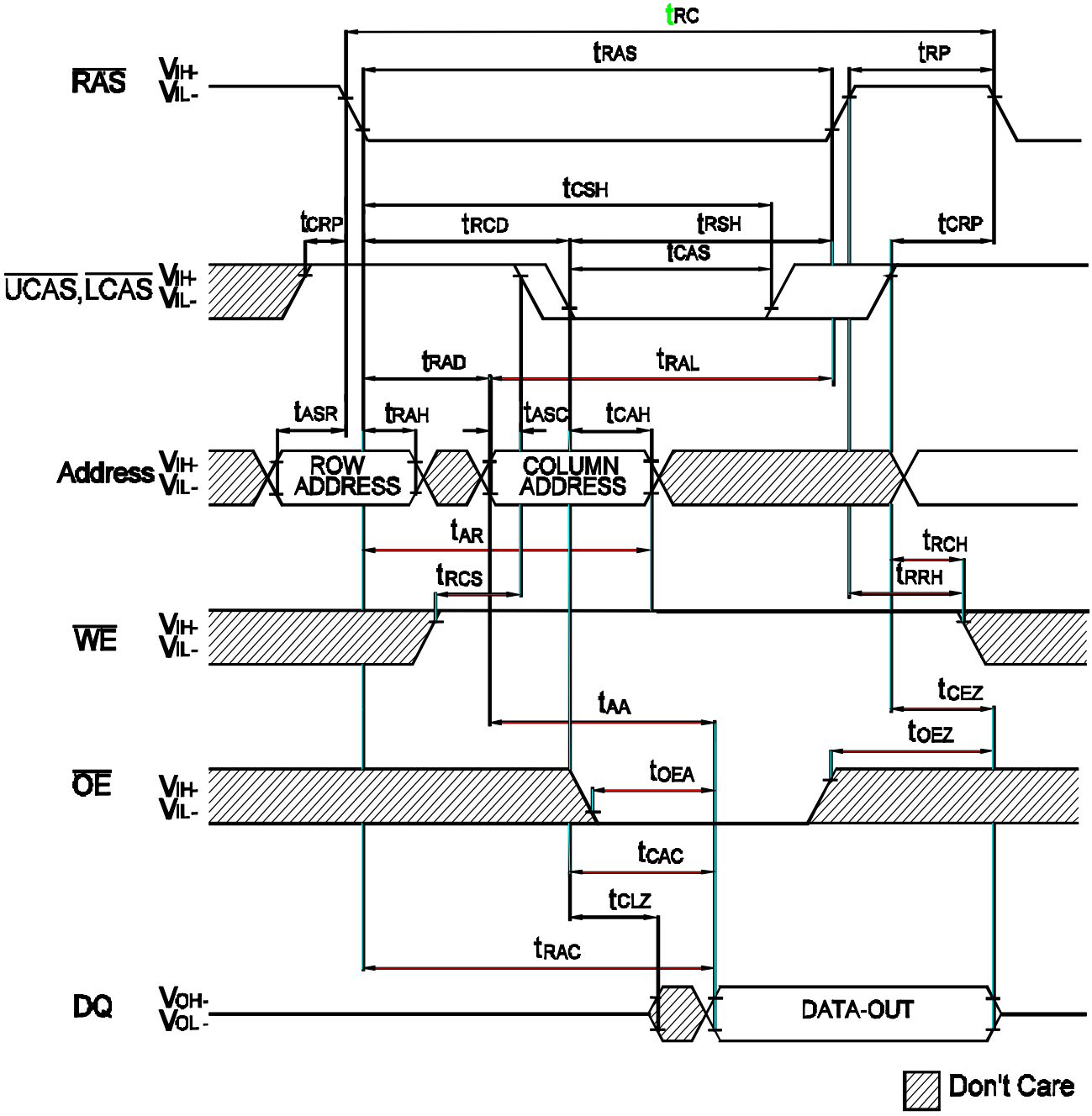
AC Characteristics

Parameter	Symbol	30		35		40		45		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	10		11		12		12		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	10		11		12		12		ns	
Data Set-Up Time	t_{DS}	0		0		0		0		ns	
Data Hold Time	t_{DH}	6		7		8		8		ns	
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	26		31		36		41		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	44		49		54		59		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	22		23		24		24		ns	
Column Address to WE Delay Time	t_{AWD}	25		30		32		34		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	0		0		0		0		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		17		20		22		24	ns	
EDO Page Mode Cycle Time	t_{PC}	12		13		15		18		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	43		47		50		52		ns	
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	5		5		5		7		ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode Only)	t_{RASP}	30	100k	35	100k	40	100k	45	100k	ns	
Access Time from $\overline{OE}$	t_{OEA}		10		11		12		12	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	8		8		8		8		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	3	8	3	8	3	8	3	8	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	6		6		7		7		ns	
Data Output Hold after $\overline{CAS}$ low	t_{DOH}	3		3		3		5		ns	
$\overline{RAS}$ to Output High-Z	t_{REZ}	3	8	3	8	3	8	3	8	ns	
$\overline{WE}$ to Output High-Z	t_{WEZ}	3	10	3	10	3	10	3	10	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	8		8		8		8		ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	8		8		8		8		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	8		8		8		8		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CHR}	10		10		10		10		ns	
Transition Time	t_T	1.5	50	2	50	2	50	2	50	ns	
Refresh Period	t_{REF}		4		4		4		4	ms	

Notes:

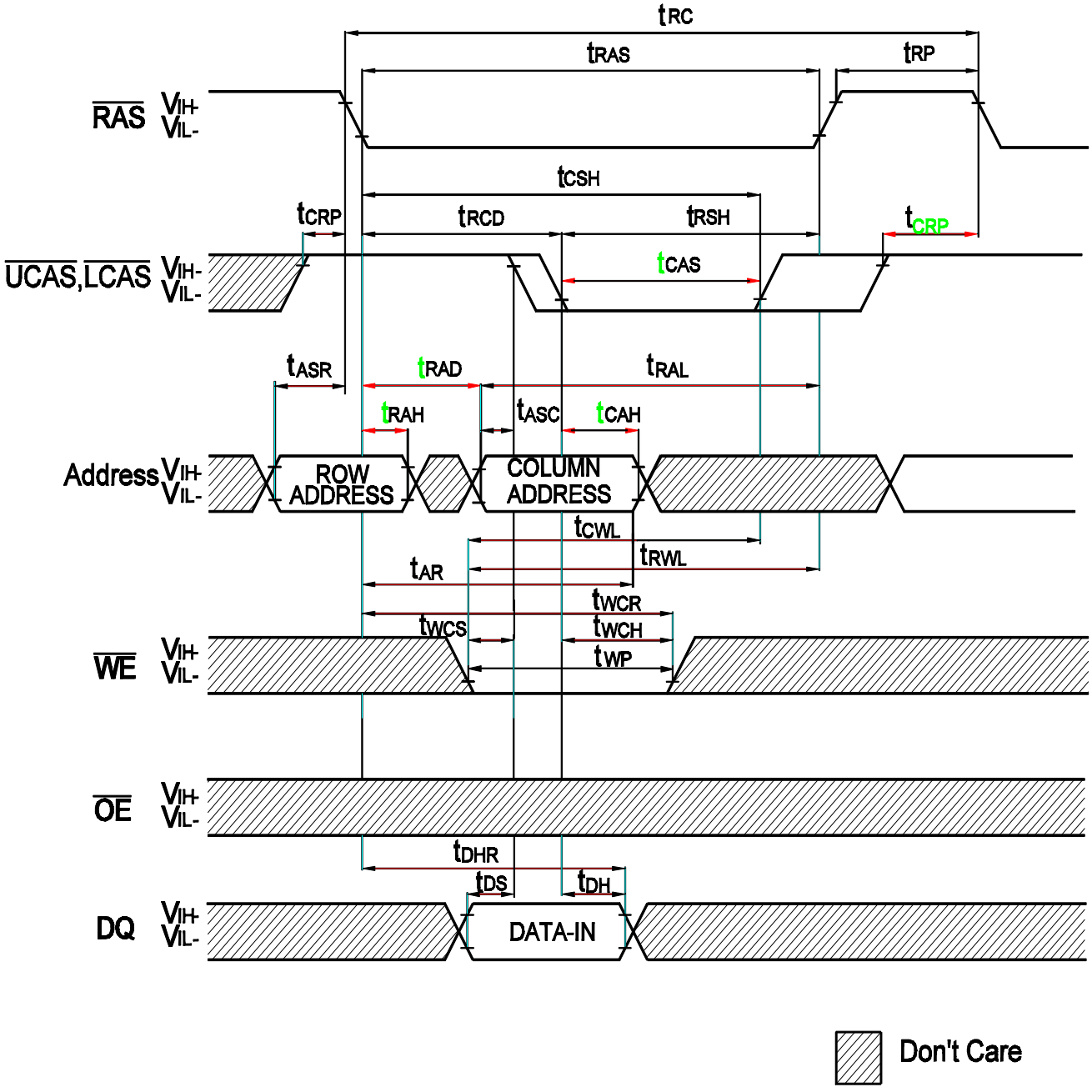
1. Measure with a load equivalent to two TTL inputs and 50 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RCD} (max.), access time will be controlled by t_{CAC}.
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA}, t_{CAC} and t_{CPA}.
6. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
7. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{AA} and t_{CAC}.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ of $\overline{WE}$.
11. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 2 ns.

Read CYCLE
Note : D_{IN} = OPEN



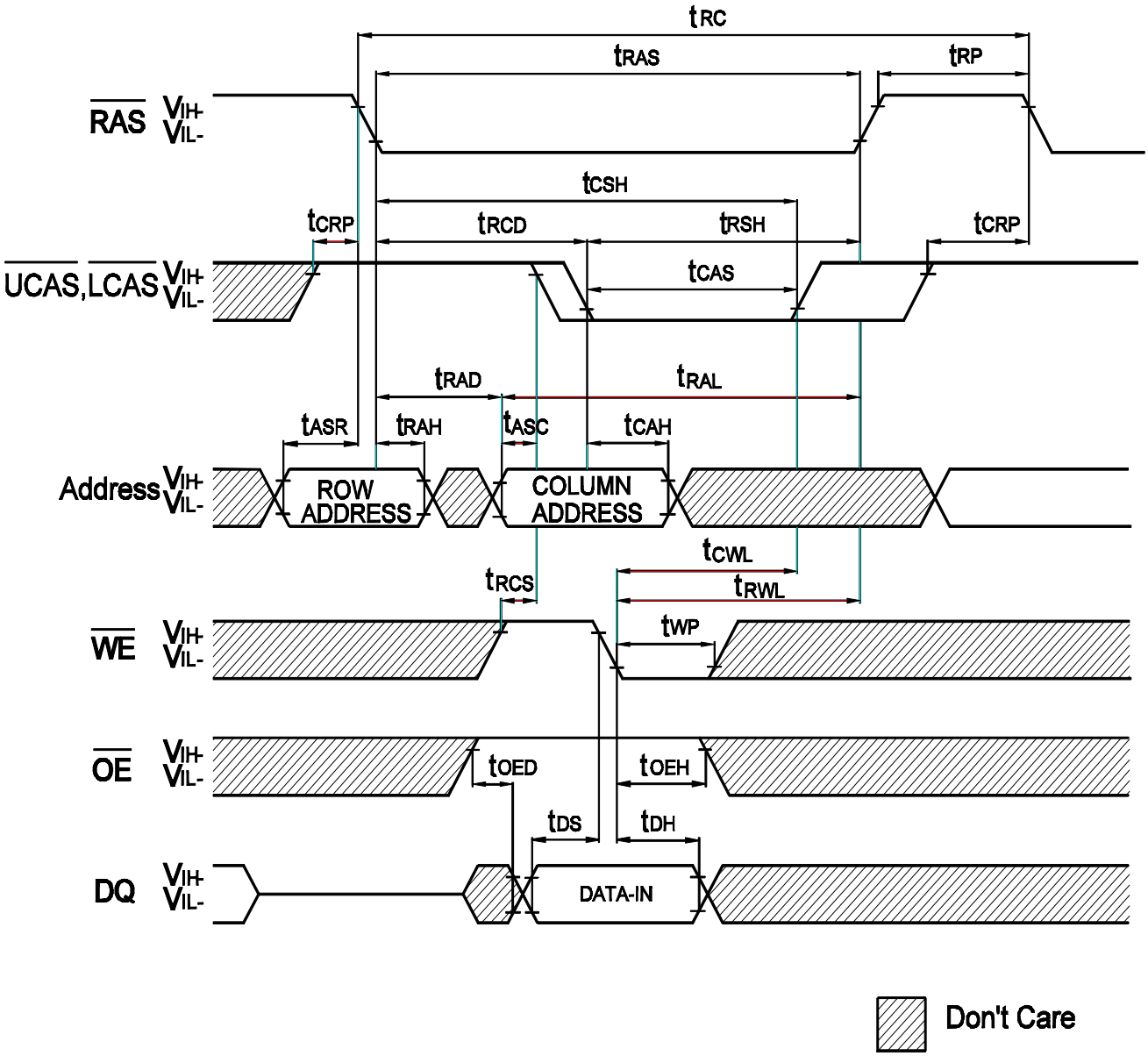
Early Write Cycle

NOTE : D_{OUT} = OPEN

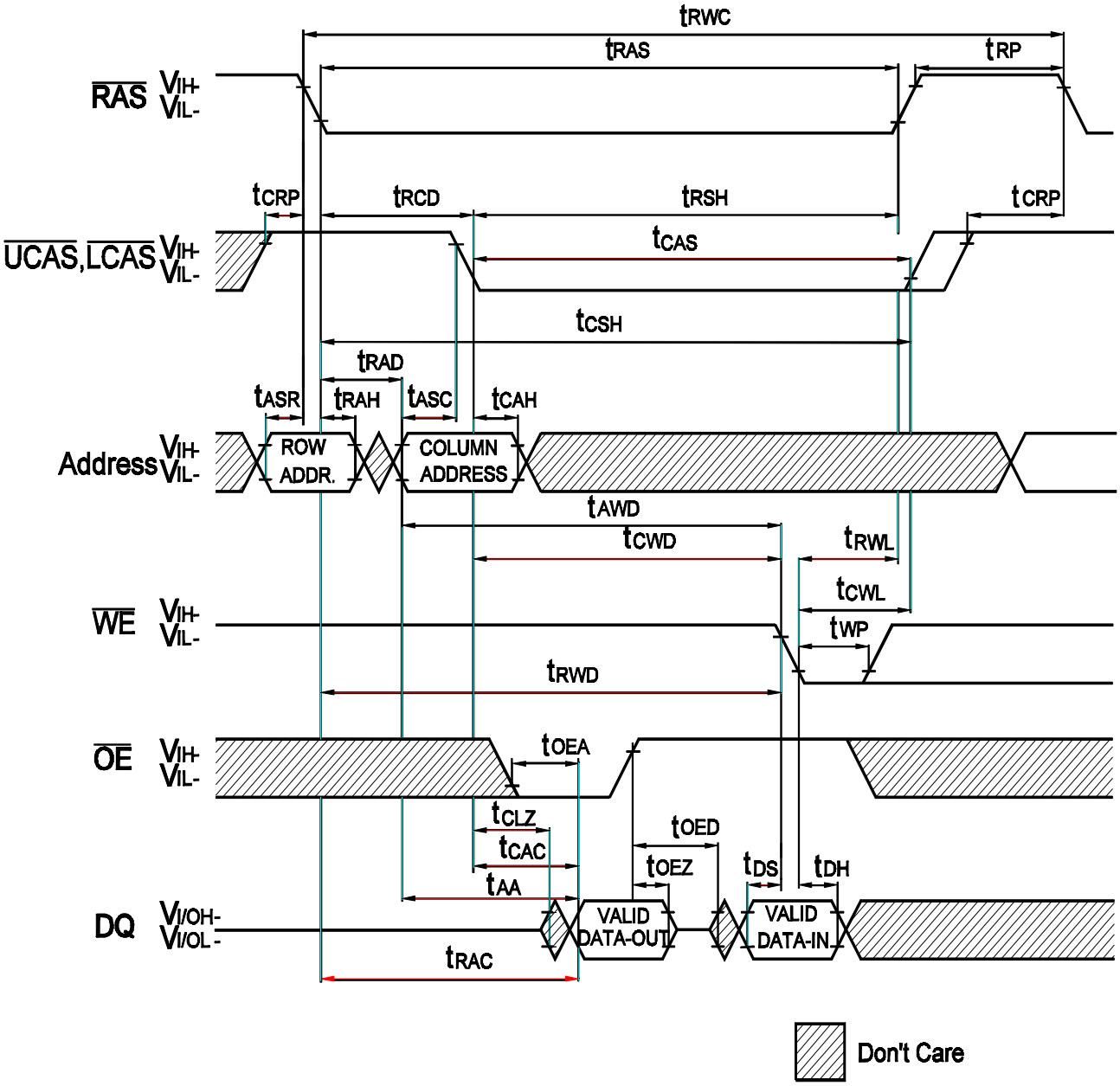


$\overline{OE}$ Controlled Write Cycle

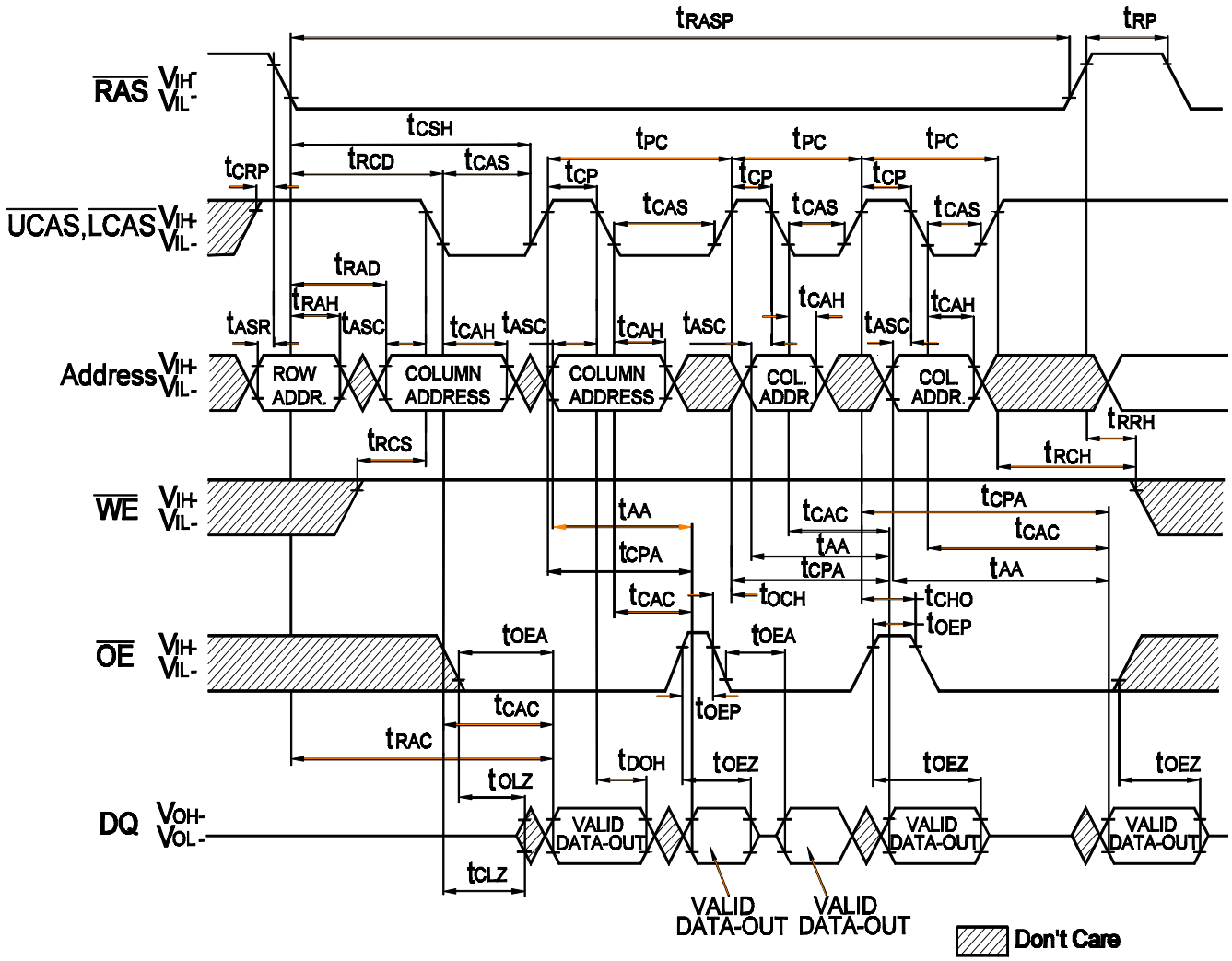
NOTE : D_{OUT} = OPEN



Read - Modify - Write Cycle

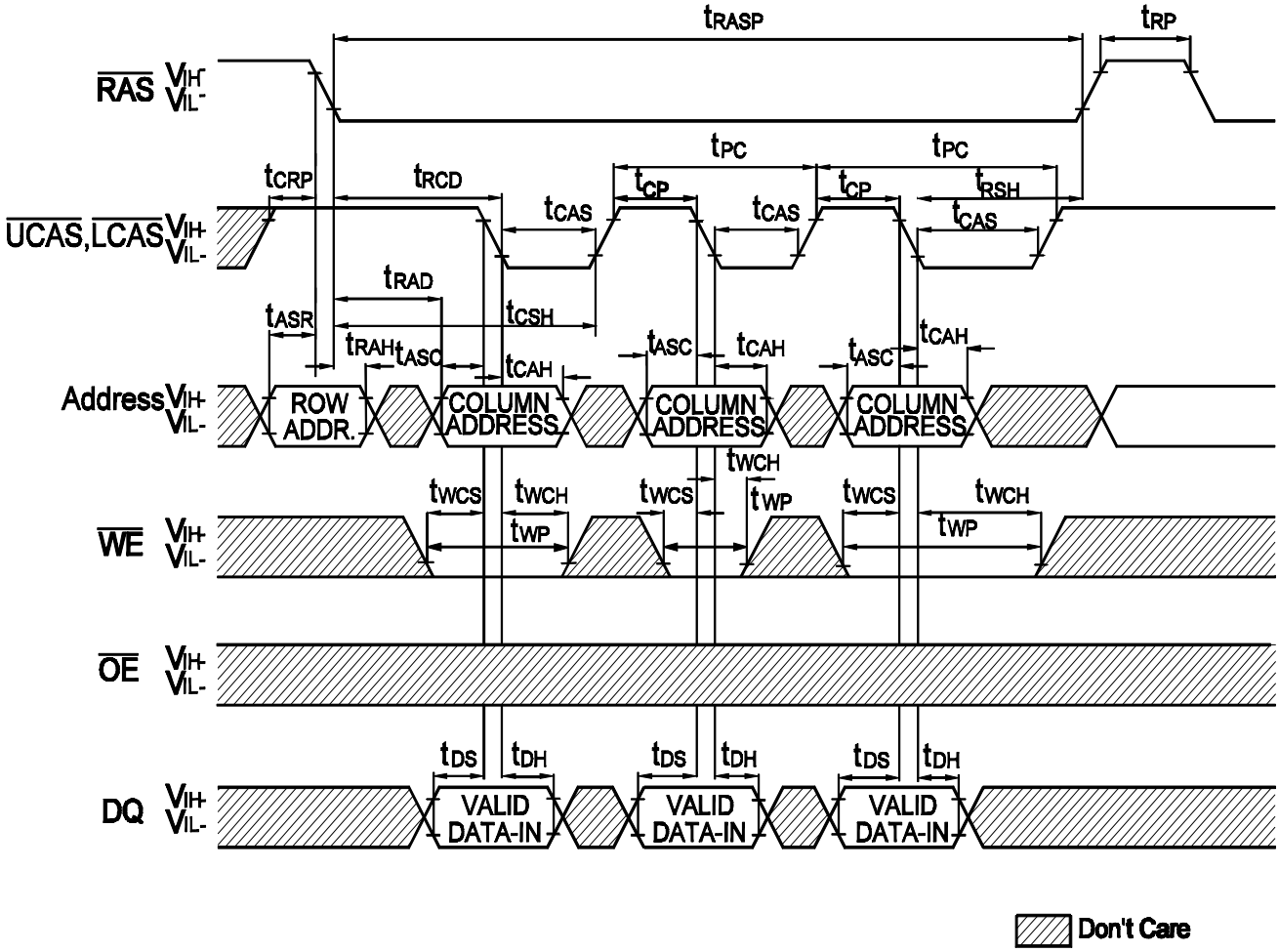


EDO Page Mode Read Cycle



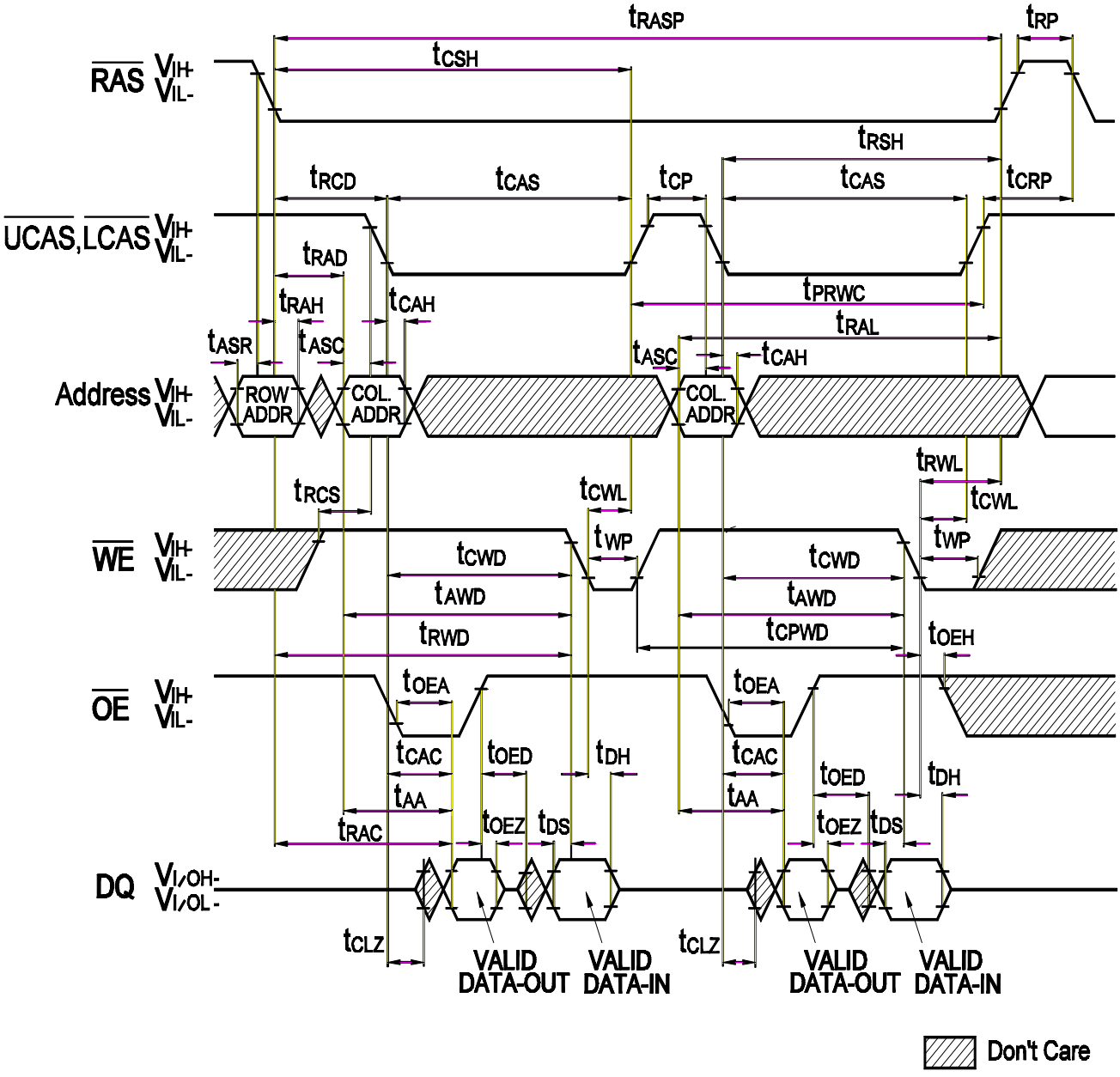
EDO Page Mode Early Write Cycle

NOTE : D_{OUT} = OPEN

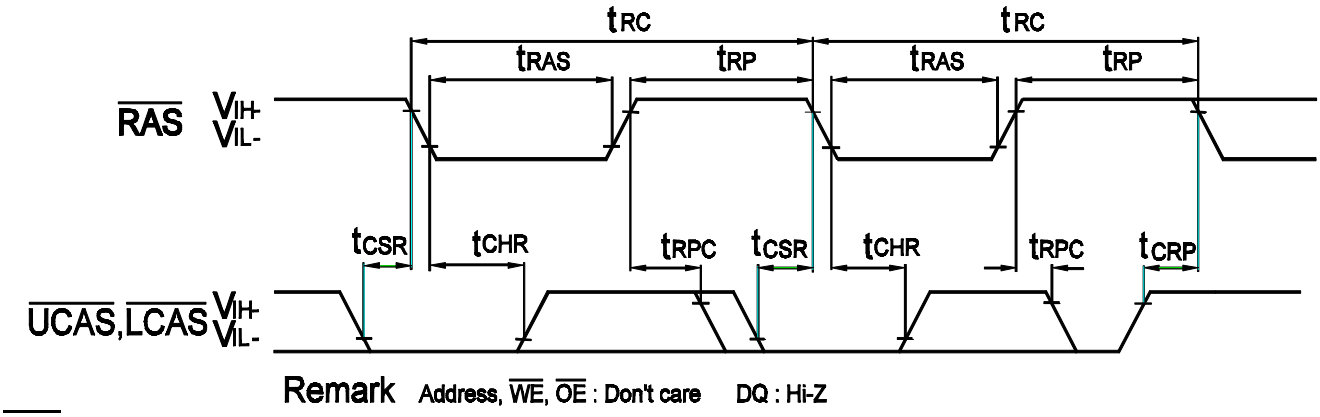


EDO Page Mode Read - Modify - Write Cycle

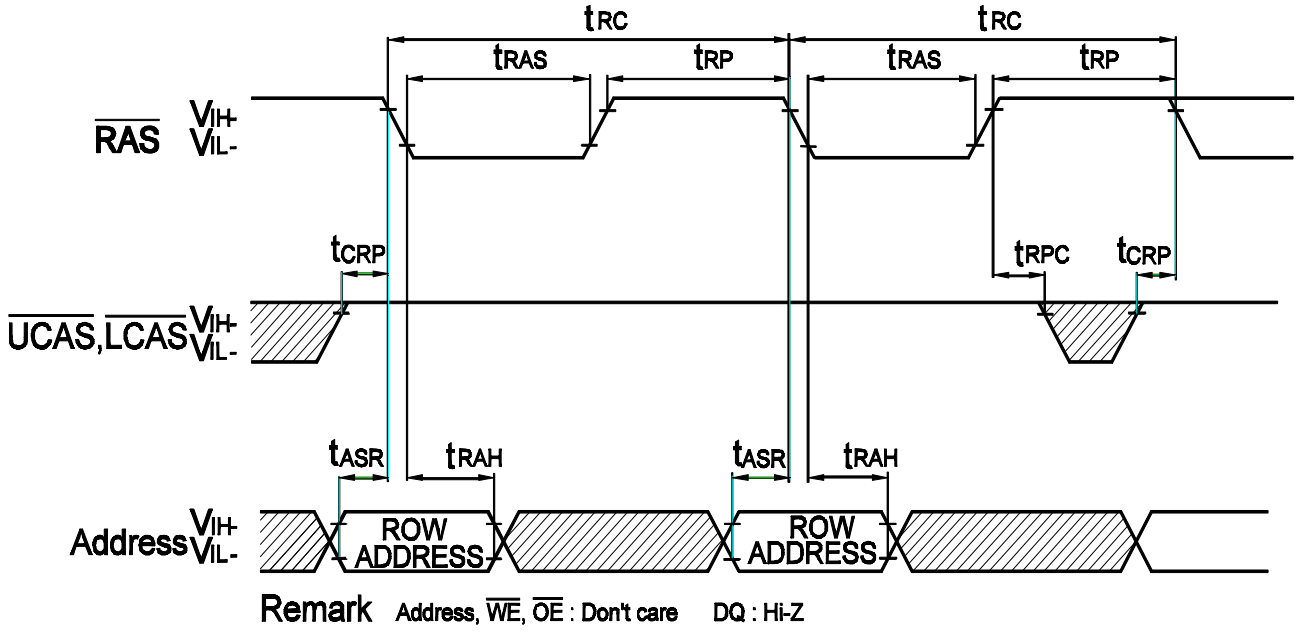
NOTE : D_{OUT} = OPEN



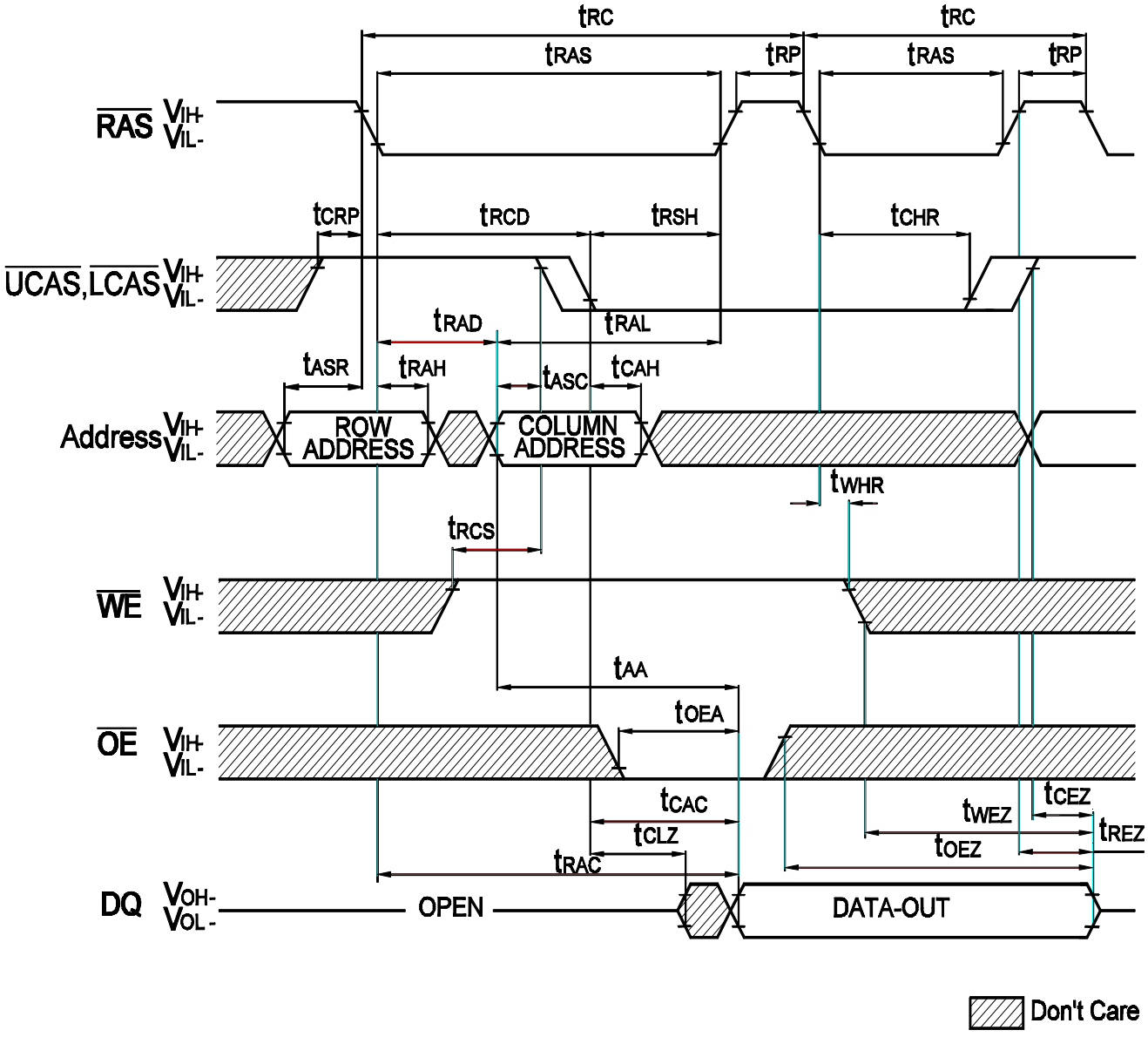
$\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Cycle



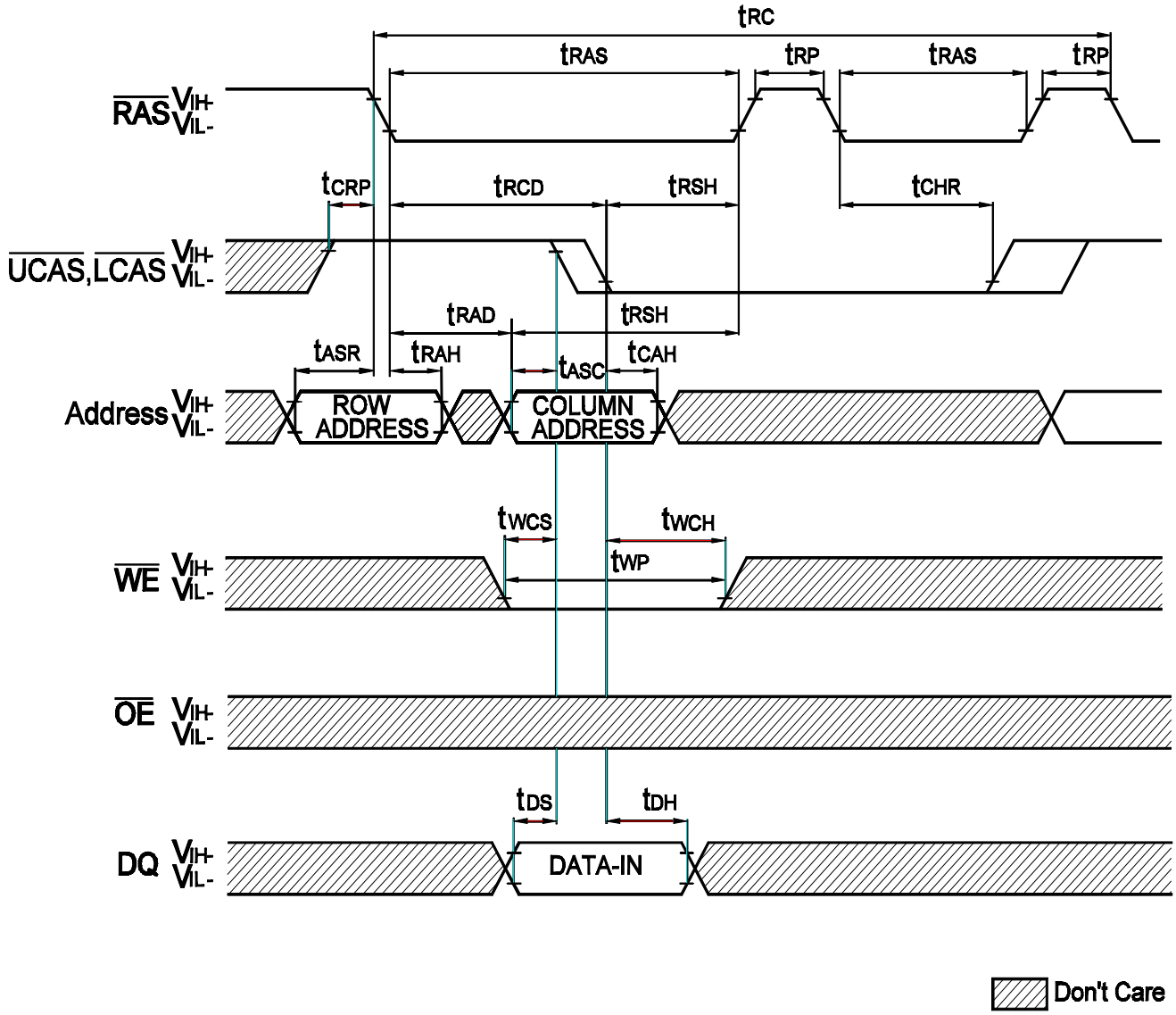
$\overline{RAS}$-Only Refresh Cycle



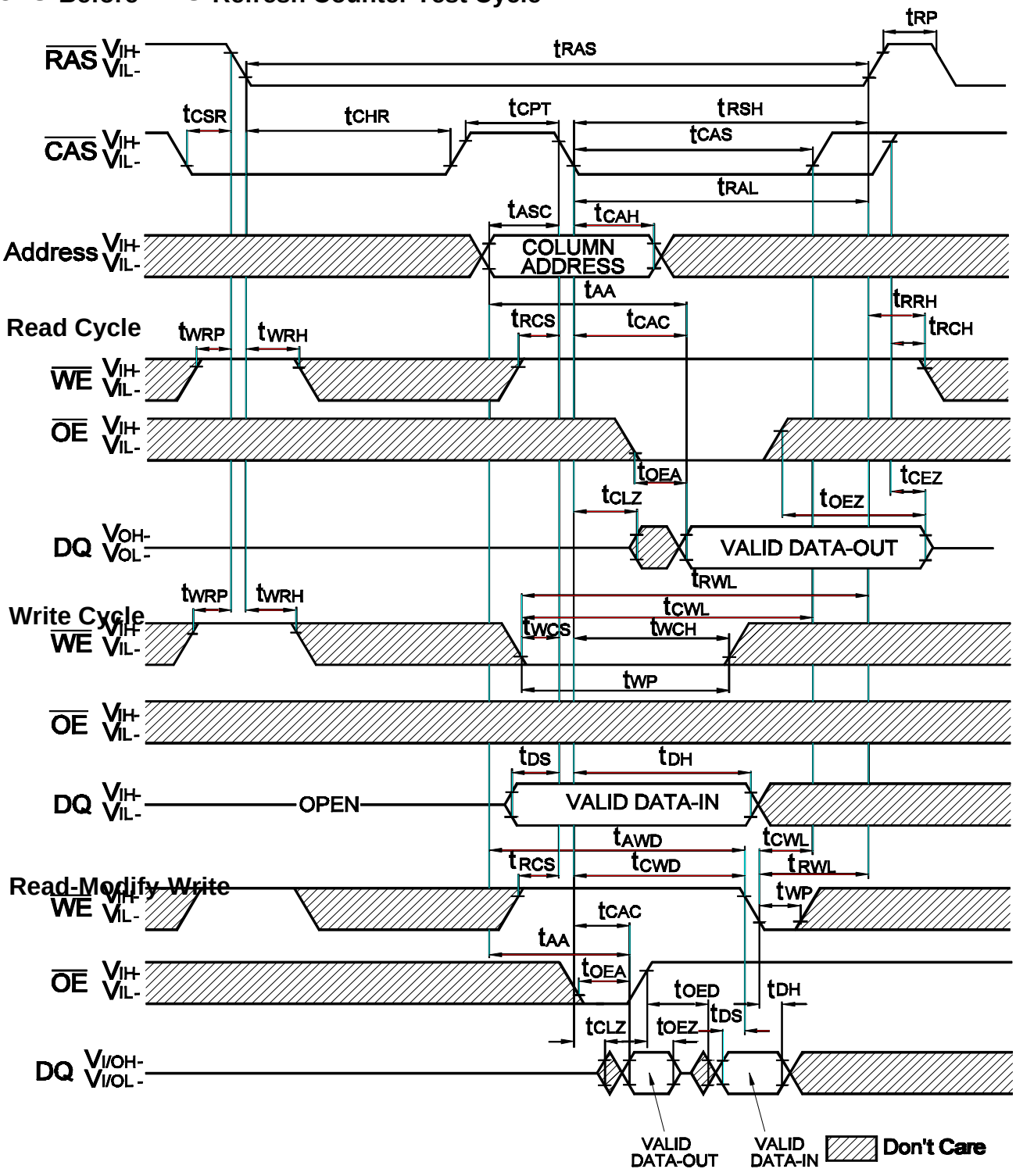
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)
NOTE : D_{OUT} = OPEN



CAS-Before-RAS Refresh Counter Test Cycle



Ordering Information

Part Number	*SPEED*	*POWER*	*FEATURE*	*PACKAGE*
GLT41016-30J4	30ns	Normal	EDO	SOJ 400mil 40L
GLT41016-35J4	35ns	Normal	EDO	SOJ 400mil 40L
GLT41016-40J4	40ns	Normal	EDO	SOJ 400mil 40L
GLT41016-45J4	45ns	Normal	EDO	SOJ 400mil 40L
GLT41016-30TC	30ns	Normal	EDO	TSOP 400mil 44L
GLT41016-35TC	35ns	Normal	EDO	TSOP 400mil 44L
GLT41016-40TC	40ns	Normal	EDO	TSOP 400mil 44L
GLT41016-45TC	45ns	Normal	EDO	TSOP 400mil 44L

. Parts Numbers (Top Mark) Definition :

GLT 4 10 16 - 40 J4

4 : DRAM
5 : Synchronous DRAM
6 : Standard SRAM /Pseudo SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM
9 : SGRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M
200 : 2M
400 : 4M

-DRAM
10 : 1M(C/EDO)
11 : 1M(C/FPM)
12 : 1M(H/EDO)
13 : 1M(H/FPM)
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
160 : 16M(EDO)
161 : 16M(FPM)
640 : 64M(EDO)
641 : 64M(FPM)

-SDRAM
40 : 4M
160 : 16M
320 : 32M,4Bank
640 : 64M
1280 : 128M

-PSEUDO SDRAM
020 – 2M
160 – 16M
320 – 32M

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.0V

POWER
Blank : Standard
L : Low Power
LL : Low Low Power
SL : Super Low Power

SPEED

-SRAM/PSEUDO SRAM
12 : 12ns
15 : 15ns
20 : 20ns
55 : 55ns
70 : 70ns
85 : 85ns
120 : 120ns

-DRAM
25 : 25ns
28 : 28ns
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns
70 : 70ns
80 : 80ns
100 : 100ns

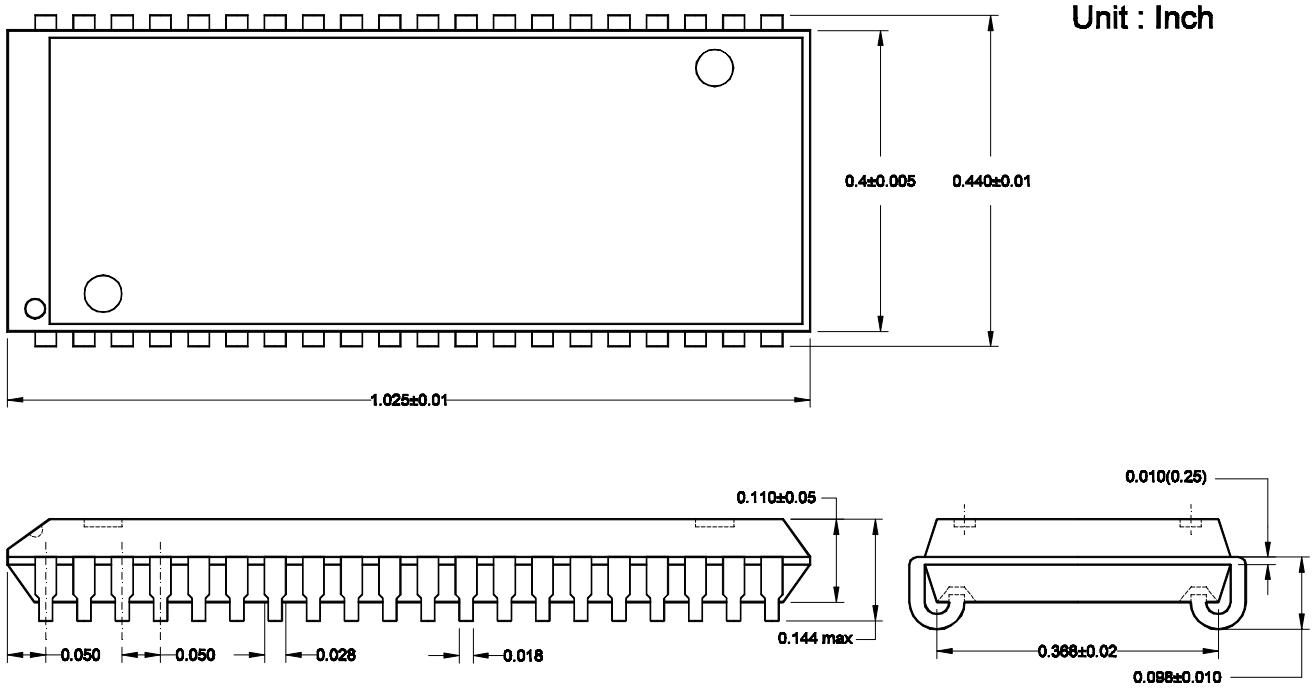
-SDRAM
5 : 5ns/200 MHZ
5.5 : 5.5ns/183 MHZ
6 : 6ns/166 MHZ
7 : 7ns/143 MHZ
8 : 8ns/125 MHZ
10 : 10ns/100 MHZ

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
ST : sTSOP(Type I)
TC : TSOPII (40/44)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP
FG : 48Pin BGA 9x12
FH : 48Pin BGA 8x10
FI : 48Pin BGA 6x8
FJ : 60Ball VFBGA

Temperature Range
E : Extended Temperature
II : Industrial Temperature
Blank : Commercial Temperature
P : Pb – free part

Package Information

400mil 40 pin Small Outline J-form Package (SOJ)



40/44 Lead Thin Small Outline Package TSOP(Type II)