

K1602TE Series

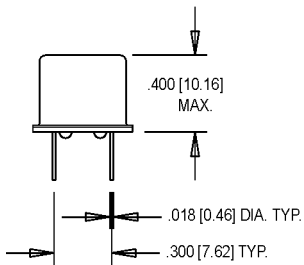
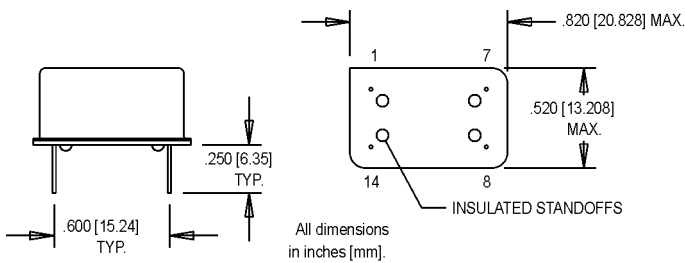
14 pin DIP, 5.0 Volt, CMOS/TTL, TCVCXO



- Former **Champion** Product
TECHNOLOGIES, INC.
- Phase-Locked Loops Clocking “Sync” to NTSC Video Standards, Reference Signal, Signal Tracking

Ordering Information

	K1602TE	X	-R	00.0000	MHz
Product Series					
Pullability					
Blank:	±28 ppm min.				
W:	±40 ppm min.				
RoHS Compliance					
Blank:	non-RoHS compliant part				
-R:	RoHS compliant part				
Frequency (customer specified)					
(Consult factory for “TEW” option)					



Pin Connections

PIN	FUNCTION
1	Control Voltage
7	Ground/Case Gnd
8	Output
14	+Vdd

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	2.0 to 35.0	38.88 to 40.0		MHz	
Operating Temperature	T _A	-40		+85	°C	
Storage Temperature	T _s	-40		+85	°C	
Frequency Stability	ΔF/F			±7.0	ppm	See Note 1
Aging (10 Year)		-2		+2	ppm	
Pullability/APR		(See Ordering Information)				
Control Voltage	V _c	0.5	2.5	4.5	V	Positive Monotonic Slope
Tuning Range		±28 (“TEW” model ±40)			ppm	
Modulation Bandwidth	f _m	20			kHz	±3dB
Input Impedance	Z _{in}	50k			Ω	@ 10 kHz
Input Voltage	V _{dd}	4.75	5.0	5.25	V	
Input Current	I _{dd}			20	mA	
Output Type						HCMOS/TTL
Load		5 TTL or 15 pF HCMOS				See Note 2
Symmetry (Duty Cycle)						See Note 3
< 14 MHz		45		55	%	
≥14 MHz		40		60	%	
Logic “1” Level	V _{oh}	4.5			V	
Logic “0” Level	V _{ol}			0.5	V	
Rise/Fall Time	T _r /T _f		3.5	9.0	ns	
Start up Time				20	ms	
Phase Noise (Typical)		10 Hz	100 Hz	1 kHz	10 kHz	100 kHz
		-70	-95	-120	-140	-150
						Offset from carrier dBc/Hz

1. Inclusive of calibration, temperature, voltage, load and aging.
2. TTL load - see load circuit diagram #1. HCMOS load - see load circuit diagram #2.
3. Symmetry is measured at 1.4 V with TTL load, and at 50% V_{dd} with HCMOS load.

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