128MB to 1GB Industrial ATA Flash

FEATURES

- ATA Compatibility
  - 3.3V or 5.0V single power supply.
  - 68 pin two piece connector with Type-2 form factor (5mm thickness)
  - Support for CIS implementation with 256 bytes of attribute memory
- Interface modes
  - PC card memory mode
  - PC card I/O mode
  - True IDE mode
- High performance
  - Interface Transfer speed in PIO mode 4 or Multi Word DMA mode 2 cycle timing, 16.6 Mbytes/ second (theoretical)
  - Sustained write: max 6.0 Mbytes/s in ATA PIO mode 4 cycle timing
  - Sustained read: max 6.5 Mbytes/s in ATA PIO mode 4 cycle timing
- W/E Endurance: 100,000cycles[1] /300,000cycles[2]

  Notes: 1. T_A = -40 to 85°C
  2. T_A = 0 to 70°C

DESCRIPTION

The WED7PxxxATA70xxI25 series ATA card is an ATA interface flash memory card based on flash technology. The ATA card is constructed with a flash disk controller chip and NAND-type flash memory device. Operates from a single 5-Volt or 3.3-Volt power source. The card is available in ATA type-2 form factor with 128MB, 256MB, 512MB and 1.02GB unformatted capacity. Being able to emulate IDE hard disk drives, WEDC's ATA card is a perfect choice for solid-state mass-storage in industrial applications and applications that require performance and extended environmental tolerances.

- Dimensions:

  Type 2 card: 85.6mm(L) x 54.0mm (W) x 5.03mm (H)

  Lead free and RoHS compliant
- Storage Capacities:

  128MB, 256MB, 512MB and 1.02GB (unformatted)
- Operating Voltage:

  3.3V ± 5%
  5.0V ± 0.5V
- Power consumption:
  - 5V operation
    Active mode:
    Write operation: 28 mA (Typ.)
    Read operation: 23 mA (Typ.)
    Power down mode: 1.2mA (Typ.) 2.0mA (max.)
  - 3.3V operation
    Active mode:
    Write operation: 25 mA (Typ.)
    Read operation: 21 mA (Typ.)
    Power down mode: 1.0mA (Typ.) 1.5mA (max.)
- Environment conditions:
  - Operating temperature: -40°C to 85°C
  - Storage temperature: -45°C to 90°C
  - Storage humidity: 95% (max) (No condensation)

* This product is subject to change without notice.

PRODUCT TYPES

Card Density	Model No.	Cylinder	Head	Sector	Memory capacity[1]
128MB	7P128ATA70xxI25	978	8	32	128,188,416 Byte
256MB	7P256ATA70xxI25	978	16	32	256,376,832 Byte
512MB	7P512ATA70xxI25	993	16	63	512,483,328 Byte
1.02GB	7P1G0ATA70xxI25	1985	16	63	1024,450,560 Byte

1: It is the logical address capacity including the area used for File System.

PIN ASSIGNMENTS AND PIN TYPE

	Memory card mode		I/O Card Mode		True IDE Mode	
Pin #	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
1	GND		GND		GND	
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	CE1#	I	CE1#	I	CE1#	I
8	A10	I	A10	I	A10	I
9	OE#	I	OE#	I	ATASEL#	I
10	N.C.	–	N.C.	–	N.C.	–
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	N.C.	–	N.C.	–	N.C.	–
14	N.C.	–	N.C.	–	N.C.	–
15	WE#	I	WE#	I	WE#	I
16	RDY/BSY	O	IREQ#	O	INTRQ	O
17	Vcc		Vcc		Vcc	
18	N.C.	–	N.C.	–	N.C.	–
19	N.C.	–	N.C.	–	N.C.	–
20	N.C.	–	N.C.	–	N.C.	–
21	N.C.	–	N.C.	–	N.C.	–
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	IOIS16#	O	IOIS16#	O
34	GND	–	GND	–	GND	–

	Memory card mode		I/O Card Mode		True IDE Mode	
Pin #	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
35	GND	–	GND	–	GND	–
36	CD1#	O	CD1#	O	CD1#	O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I	D15	I	D15	I
42	CE2#	I	CE2#	I	CE2#	I
43	VS1	O	VS1	O	VS1	O
44	IORD#	I	IORD#	I	IORD#	I
45	IOWR#	I	IOWR#	I	IOWR#	I
46	NC	–	NC	–	NC	–
47	NC	–	NC	–	NC	–
48	NC	–	NC	–	NC	–
49	NC	–	NC	–	NC	–
50	NC	–	NC	–	NC	–
51	Vcc	–	Vcc	–	Vcc	–
52	NC	–	NC	–	NC	–
53	NC	–	NC	–	NC	–
54	NC	–	NC	–	NC	–
55	NC	–	NC	–	NC	–
56	CSEL#	I	CSEL#	I	CSEL#	I
57	VS2	O	VS2	O	VS2	O
58	RESET	I	RESET	I	RESET#	I
59	Wait#	O	Wait#	O	IORDY	O
60	INPACK#	O	INPACK#	O	INPACK#	O
61	REG#	I	REG#	I	REG#	I
62	BVD2	I/O	SPKR#	I/O	DASP	I/O
63	BVD1	I/O	STSCHG#	I/O	PDIAG#	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	O	D10	O	D10	O
67	CD2#	O	CD2#	O	CD2#	O
68	GND	–	GND	–	GND	–

ACCESS SPECIFICATIONS

1. Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of REG# = ”L” as follows. That region can be accessed by Byte/Word/Odd-byte modes, which are defined by PC card standard specifications.

Attribute Read Access Mode

Mode	REG#	CE2#	CE1#	A0	OE#	WE#	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	High-Z	High-Z
Byte access (8bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	Invalid
Word access (16bit)	L	L	L	X	L	H	invalid	even byte
Odd byte access (8bit)	L	L	H	X	L	H	invalid	High-Z

Note: X → L or H

Attribute Write Access Mode

Mode	REG#	CE2#	CE1#	A0	OE#	WE#	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	Don’t care	Don’t care
Byte access (8bit)	L	H	L	L	H	L	Don’t care	even byte
	L	H	L	H	H	L	Don’t care	Don’t care
Word access (16bit)	L	L	L	X	H	L	Don’t care	even byte
Odd byte access (8bit)	L	L	H	X	H	L	Don’t care	Don’t care

Note: X → L or H
Write CIS-ROM region is invalid.

2. Task File register access specifications

There are two types of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each type of Task File register read and write operation is executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte modes, which are defined by PC card standard specifications.

(1) I/O address map – Task File Register Read Access Mode (1)

Mode	REG#	CE2#	CE1#	A0	IORD#	IOWR#	OE#	WE#	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	L	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	L	L	H	X	L	H	H	H	odd byte	High-Z

Note: X → L or H

Task File Register Write Access Mode (1)

Mode	REG#	CE2#	CE1#	A0	IORD#	IOWR#	OE#	WE#	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	Don't care	Don't care
Byte access (8bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16bit)	L	L	L	X	H	L	H	H	odd byte	even byte
Odd byte access (8bit)	L	L	H	X	H	L	H	H	odd byte	Don't care

Note: X → L or H

(2) Memory address map – Task File Register Read Access Mode (2)

Mode	REG#	CE2#	CE1#	A0	OE#	WE#	IORD#	IOWR#	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	H	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	L	H	H	H	odd byte	High-Z

Note: X → L or H

Task File Register Write Access Mode (2)

Mode	REG#	CE2#	CE1#	A0	OE#	WE#	IORD#	IOWR#	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	Don't care	Don't care
Byte access (8bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16bit)	H	L	L	X	H	L	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	H	L	H	H	odd byte	Don't care

Note: X → L or H

3. TRUE IDE MODE

The card can be configured in a True IDE. This card is configured in this mode only when the OE# input signal is asserted to GND by the host during power on . In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register is allowed. If this card is configured during power on sequence, data register is accessed in word (16-bit). The card permits 8-bit accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

True IDE Mode Read I/O Function

Mode	CE2#	CE1#	A0~A2	DMACK#	DIOR#	DIOW#	D8~D15	D0~D7
Invalid mode	L	L	X	X	X	X	High-Z	High-Z
Standby mode	H	H	X	H	X	X	High-Z	High-Z
PIO Data register access	H	L	0	H	L	H	Odd byte	even byte
Multiword DMA Data register access	H	H	X	L	L	H	Odd byte	even byte
Alternate status access	L	H	6H	H	L	H	High-Z	Status out
Other task file access	H	L	1~7H	H	L	H	High-Z	Data

Note: X → L or H

True IDE Mode Write I/O Function

Mode	CE2#	CE1#	A0~A2	DMACK#	DIOR#	DIOW#	D8~D15	D0~D7
Invalid mode	L	L	X	X	X	X	Don't care	Don't care
Standby mode	H	H	X	H	X	X	Don't care	Don't care
PIO Data register access	H	L	0	H	H	L	Odd byte	even byte
Multiword DMA Data register access	H	H	X	L	H	L	Odd byte	even byte
Control register access	L	H	6H	H	H	L	Don't care	Control in
Other task file access	H	L	1~7H	H	H	L	Don't care	Data

Note: X → L or H

CARD SYSTEM PERFORMANCE

ITEM	PERFORMANCE
Set up time (Reset to Ready)	250 ms (max.)
Set up time (Power down to Ready)	5.5 ms (max.)
Data transfer rate to / from host	16.6 M byte / s burst (max.), theoretically
Sustained read transfer rate	6.5 M byte / s (max.), actually *1
Sustained write transfer rate	6.0 M byte / s (max.), actually *1
Command to DRQ (Sector Re ad at Ready state)	4 ms (max.)
Command to DRQ (Sector Write at Ready state)	700 ms (max.)
Data transfer cycle end to ready (Sector write)	2 ms (typ.), 200 ms (max.)
Auto Power down time	1.5s (min.), 1.8s (typ.)

Notes:

1. The actual transfer rate is measured under ATA PIO mode 4 with single cycle time as 120ns.

ELECTRICAL SPECIFICATION

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT
V_{IN}, V_{OUT}	All input / output voltage	-0.3	V_{CC}+0.3	—	V
V_{CC}	Power Supply Voltage (Absolute Maximum Ratings)	-0.6	6.0	—	V
V_{CC}	Power Supply Voltage (Recommended Operation Condition)	4.5	5.5	5.0	V
		3.135	3.465	3.3	V
T_{OPR}	Operating Temperature	-40	85	—	°C
T_{STG}	Storage Temperature	-45	90	—	°C

Input Leakage Current

Type	SYMBOL	PARAMETER	CONDITION	MIN	MAX	TYP	UNIT	NOTES
IxZ	IL	Input leakage current	V_{IH} = Vcc / V_{IL} = GND	-1	1	—	µA	*1
IxU	RPU1	Pull Up Resistor	Vcc = 5.0V	50	500	—	kΩ	*1
IxD	RPD1	Pull Down Resister	Vcc = 5.0V	50	500	—	kΩ	*1

Notes:

1. x refers to the characteristics described in section “DC Characteristics (Input Characteristics)”. For example, I1U indicates a pull up resister with a type 1 input characteristics.

Output Drive Type

Type	OUTPUT TYPE	VALID CONDITIONS	NOTES
OTx	Totempole	I_{OH} & I_{OL}	*1
OZx	Tri-State N-P Channel	I_{OH} & I_{OL}	*1
OPx	P-Channel only	I_{OH} Only	*1
ONx	N-Channel only	I_{OL} Only	*1

Notes:

1. x refers to the characteristics described in section “DC Characteristics (Output Drive Characteristics)”. Fo r example, OT1 refers to Totempole output with a type 1 Output drive characteristics.

DC CHARACTERISTICS

V_{CC} = 3.3 V ± 5%, 5 V ± 0.5V, -40°C ≤ T_A ≤ 85°C

SYMBOL	PARAMETER	MIN	MAX	TYP.	UNIT	TEST CONDITIONS
I_{LI}	Input leakage current	—	1	—	µA	—
I_{LO}	Output leakage current	—	1	—	µA	V_{OUT} = high impedance
I_{PU}	Pull-up current (Resistivity)	—	—	43 (75)	µA (kΩ)	V_{FORCE} = 3.3V
I_{PD}	Pull-down current (Resistivity)	—	—	-43 (75)	µA (kΩ)	V_{FORCE} = 0V
I_{CCS}	Power down mode current	— —	1.5 2.0	1.0 1.2	mA	V_{CC} = 3.3V V_{CC} = 5V
I_{CCO}	Operating current @ 3.3V Write operation Read operation	— —	— —	25 21	mA	V_{CC} = 3.3V operation
	Operating current @ 5V Write operation Read operation	— —	— —	28 23	mA	V_{CC} = 5V operation

Input Characteristics

Type	SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	CONDITION
1	V_{IH}	Input High Voltage CMOS	2.0 2.0	—	—	V	V_{CC} = 3.3 V V_{CC} = 5 V
	V_{IL}	Input Low Voltage CMOS	—	1.0 1.0	—		V_{CC} = 3.3 V V_{CC} = 5 V
2	V_{IH}	Input High Voltage	2.0 2.0	—	—		V_{CC} = 3.3 V V_{CC} = 5 V
	V_{IL}	Input Low Voltage CMOS	—	1.0 0.8	—		V_{CC} = 3.3 V V_{CC} = 5 V
3	V_{T+}	Input Low to High threshold Schmitt trigger	—	2.5 2.5	2.1 2.1		V_{CC} = 3.3 V V_{CC} = 5 V
	V_{T-}	Input High to Low threshold Schmitt trigger	0.9 0.9	—	1.2 1.2		V_{CC} = 3.3 V V_{CC} = 5 V
	V_t	Hysteresis voltage	0.5 0.8				V_{CC} = 3.3 V V_{CC} = 5 V
4	V_{T+}	Input Low to High threshold Schmitt trigger	—	2.3 2.0	2.1 1.8		V_{CC} = 3.3 V V_{CC} = 5 V
	V_{T-}	Input High to Low threshold Schmit trigger	1.0 0.8		1.2 1.1		V_{CC} = 3.3 V V_{CC} = 5 V
	V_t	Hysteresis voltage	0.5 0.8				V_{CC} = 3.3 V V_{CC} = 5 V

Output Drive Characteristics

Type	SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	CONDITION
1	V_{OH}	Output High Voltage	V_{CC} - 0.8	—	—	V	I_{OH} = -4mA I_{OL} = 4mA
	V_{OL}	Output Low Voltage	—	Gnd + 0.4	—		

AC CHARACTERISTICS

V_{CC} = 3.3 V ± 5%, 5 V ± 0.5V, -40°C ≤ T_A ≤ 85°C

Attribute Memory Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_C	Read cycle time	250	—	ns
t_A	Address access time	—	250	
t_A	CE# access time	—	250	
t_A	OE# access time	—	125	
t_{DIS}	Output disable time (CE#)	—	100	
t_{DIS}	Output disable time (OE#)	—	100	
t_{EN}	Output enable time (CE#)	5	—	
t_{EN}	Output enable time (OE#)	5	—	
t_V	Data valid time (A)	0	—	
t_{SU}	Address setup time	30	—	

Attribute Memory Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_C	Write cycle time	250	—	ns
t_W	Write pulse time	150	—	
t_{SU}	Address setup time	30	—	
t_{SU}	Data setup time (-WE)	80	—	
t_H	Data hold time	30	—	
t_{REC}	Write recover time	30	—	

I/O Access Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_D	Data delay after IORD#	—	100	ns
t_H	Data hold following IORD#	0	—	
t_W	IORD# pulse width	165	—	
t_{SU}A	Address setup before IORD#	70	—	
t_HA	Address hold following IORD#	20	—	
t_{SU}CE	CE# setup before IORD#	5	—	
t_HCE	CE# hold following IORD#	20	—	
t_{SU}REG	REG# setup before IORD#	5	—	
t_HREG	REG# hold following -IORD	0	—	
t_{DF}INPACK	INPACK# delay failing from IORD#	0	45	
t_{DR}INPACK	INPACK# delay rising from IORD#	—	45	
t_{DF}IOIS1$_6$	IOIS#16 delay failing from address	—	35	
t_{DR}IOIS16	IOIS#16 delay rising from address	—	35	

I/O Access Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SU}	Data setup before IOWR#	60	—	ns
t_H	Data hold following IOWR#	30	—	
t_W	IOWR# pulse width	165	—	
$t_{SU}A$	Address setup before IOWR#	70	—	
t_HA	Address hold following IOWR#	20	—	
$t_{SU}CE$	CE# setup before IOWR#	5	—	
t_HCE	CE# hold following IOWR#	20	—	
$t_{SU}REG$	REG# setup before IOWR#	5	—	
t_HREG	REG# hold following IOWR#	0	—	
t_{DF}IOIS16	IOIS16# delay failing from address	—	35	
t_{DR}IOIS16	IOIS16# delay rising from address	—	35	

Common Memory Access Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_A	OE# access time	—	125	ns
t_{DIS}	Output disable time (OE#)	—	100	
t_{SU}	Address setup time	30	—	
t_H	Address hold time	20	—	
t_{SU}	CE# setup before OE#	0	—	
t_H	OE# hold following OE#	20	—	

Common Memory Access Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SU}	Data setup before WE#	80	—	ns
t_H	Data hold following WE#	30	—	
t_W	Write pulse width	150	—	
t_H	Address hold time	20	—	
t_{SU}	Address setup time	30	—	
t_{SU}	CE# setup time	0	—	
t_{REC}	Write recover time	30	—	
t_H	CE# hold following WE#	20	—	

True IDE Mode IO Read/Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t0	Cycle time	120	—	ns
t1	Address valid to -DIOW/-DIOR setup	25	—	
t2	DIOW#/-DIOR	70	—	
t2	DIOW#/-DIOR Register (8bit)	70	—	
t2i	DIOW#/-DIOR recoverry time	25	—	
t3	DIOW# data setup	20	—	
t4	DIOW# data hold	10	—	
t5	DIOR# data setup	20	—	
t6	DIOR# data hold	5	—	
t6z	DIOR# data tristate	—	30	
t7	Address valid to -IOIS16 assertion	—	35	
t8	Address valid to -IOIS16 released	—	35	
t9	DIOW#/-DIOR to address valid hold	10	—	

True IDE Mode Multiword DMA Read/Write AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
t0	Cycle time	120	—	ns
tD	DIOR#/DIOW# assert width	70	—	
tE	DIOR# data access	—	50	
tF	DIOR# data hold	5	—	
tG	DIOW#/DIOR# data setup	20	—	
tH	DIOW# data hold	10	—	
tI	DMACK# to DIOR#/DIOW# setup	0	—	
tJ	DIOR#/DIOW# to DMACK hold	5	—	
tKR	DIOR# negated width	25	—	
tKW	DIOW# negated width	25	—	
tLR	DIOR# to DMARQ delay	—	35	
tLW	DIOW# to DMARQ delay	—	35	
tM	CS0#/CS1# valid to -DIOR#/-DIOW#	25	—	
tN	CS0#/CS1# hold	10	—	
tZ	DMACK# to read data released	—	25	

Reset Characteristics (only Memory Card Mode or I/O Card Mode)

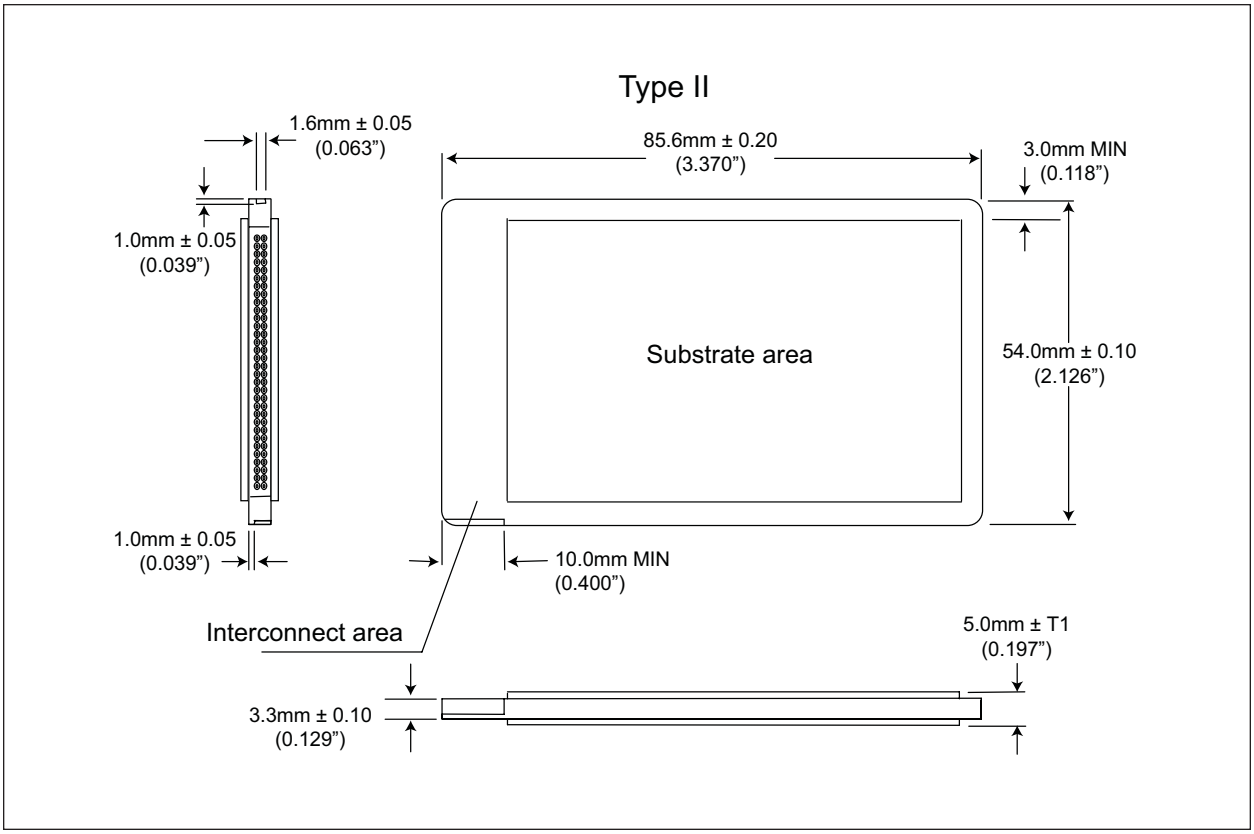
SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SU}	Reset setup time	100	—	m s
t_{REC}	CE# recover time	1	—	µs
t_{PR}	V_{CC} rising up time	0.1	100	m s
t_{PF}	V_{CC} falling down time	3	300	m s
t_W	Reset pulse width	10	—	µs
t_H		1	—	m s
t_S		0	—	m s

Power on Reset Characteristics

Power on reset sequence must need by PORST# at the rising edge of V_{CC}.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{SU}	CE# setup time	100	—	m s
t_{PR}	V_{CC} rising up time	0.1	100	m s

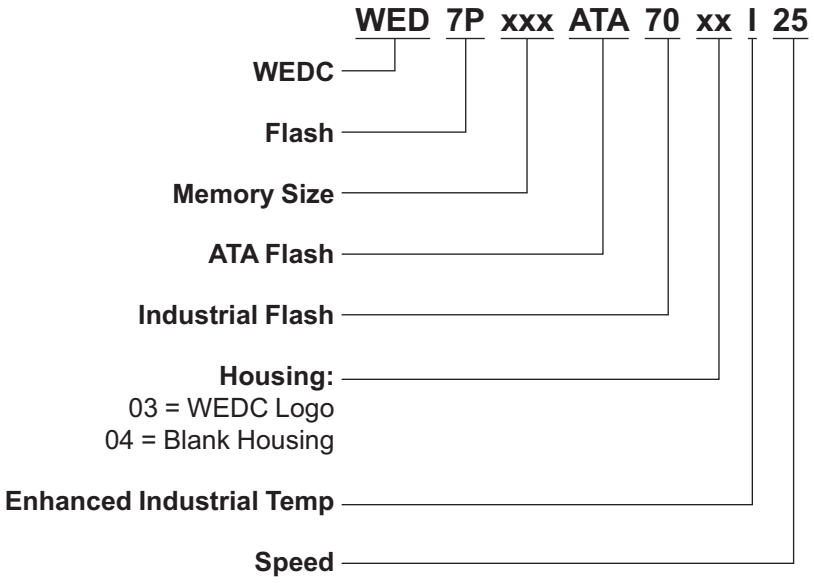
PACKAGE DIMENSIONS



ATTENTION FOR CARD USE

- In the reset or power off mode, the information in all registers are cleared.
- Note that the card insertion/removal should not be executed while host is active if the card is used in True IDE mode.
- After the hard reset, soft reset or power-on reset or ATA reset command is applied the card cannot be accessed while READY pin is “low.” Flash card can’t be operated in this mode.
- Before insertion V_{CC} cannot be supplied to the card. After confirmation that CD1#, CD2# pins are set, V_{CC} may be supplied to the card.
- OE# must be kept at the V_{CC} level during power on reset in memory card mode and I/O card mode. OE must be kept constantly at the GND level in True IDE mode.
- Do not turn off the power or remove WED7PxxxATA70xxI25 Series from the slot before read/write operation is complete. Avoid using WED7PxxxATA70xxI25 Series when the battery is low. Power shortage, power failure and/or removal of WED7PxxxATA70xxI25 Series from the slot before read/write operation is complete may cause malfunction of WED7PxxxATA70xxI25 Series, data loss and/or damage to data.
- Routine performance of backing-up data (or taking back-up of data) is strongly recommended.

PART NUMBERING GUIDE



Document Title

128MB to 1GB Industrial ATA Flash

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	March 2005	Final
Rev 1	1.1 Added "ED" to part marking	July 2005	Final