512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL, VLP Mini-DIMM

FEATURES

- 244-pin, very low profile dual in-line memory module (VLP Mini-DIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300*, and PC2-6400*
- Supports ECC error detection and correction
- V_{CC} = V_{CCQ} = 1.8V ±0.1V
- V_{CCSPD} = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- On-die termination (ODT)
- Programmable burst lenghts: 4 or 8
- Serial Presence Detect (SPD) with EEPROM
- Auto and Self Refresh Capability (64ms: 8,192 cycle refresh)
- Gold (Au) edge contacts
- RoHS compliant
- Single Rank
- Package option
  - 244 Pin Mini-DIMM
  - PCB – 18.29mm (0.72")

DESCRIPTION

The W3HG64M72EER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of nine 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 244-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option
- Parity option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t_{RCD}-t_{RP}	3-3-3	4-4-4	5-5-5	6-6-6

* Contact factory for availability

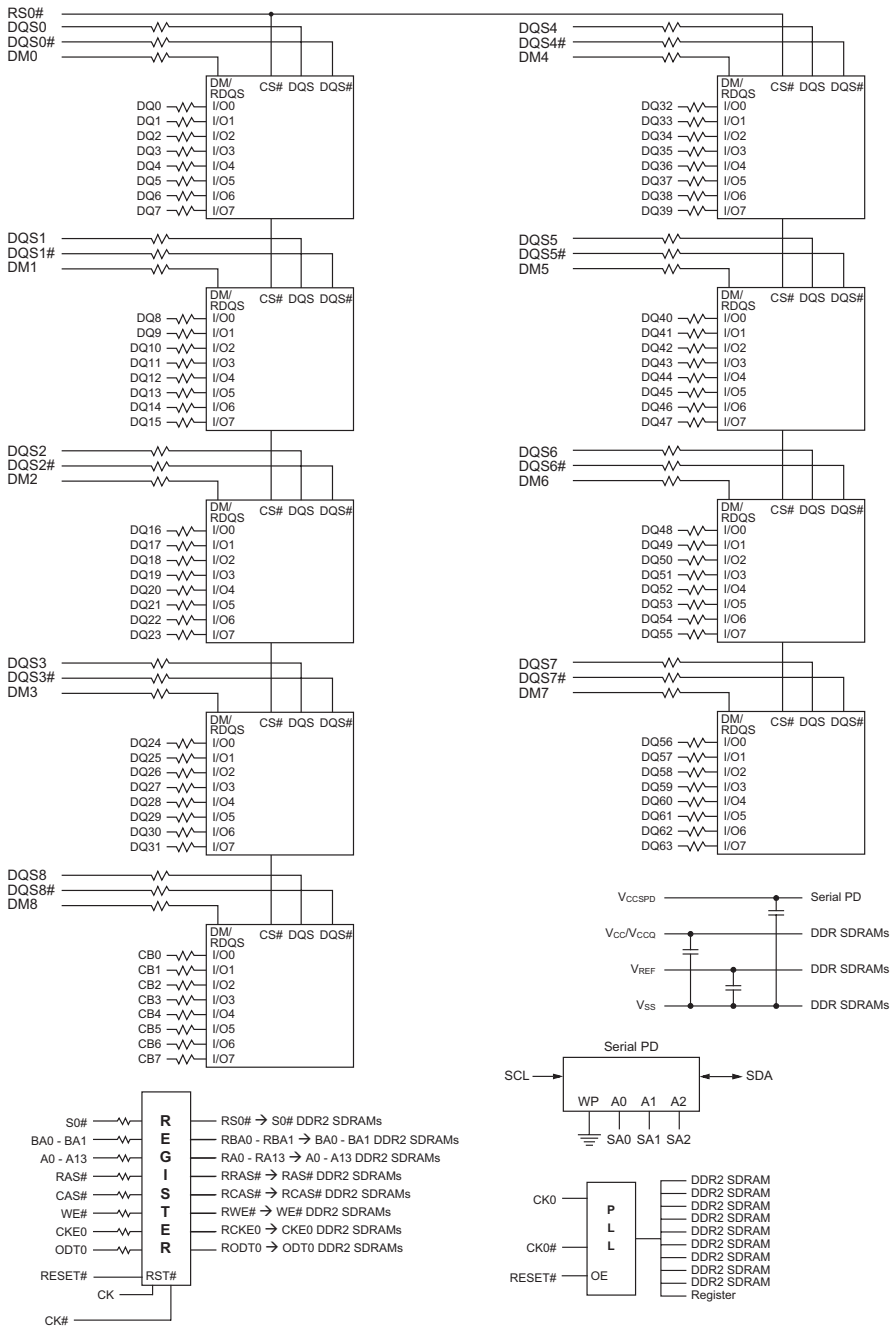
PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	62	A4	123	V_{SS}	184	V_{CCQ}
2	V_{SS}	63	V_{CCQ}	124	DQ4	185	A3
3	DQ0	64	A2	125	DQ5	186	A1
4	DQ1	65	V_{CC}	126	V_{SS}	187	V_{CC}
5	V_{SS}	66	V_{SS}	127	DM0	188	CK0
6	DQS0#	67	V_{SS}	128	NC	189	CK0#
7	DQS0	68	NC/PAR_IN	129	V_{SS}	190	V_{CC}
8	V_{SS}	69	V_{CC}	130	DQ6	191	A0
9	DQ2	70	A10/AP	131	DQ7	192	BA1
10	DQ3	71	BA0	132	V_{SS}	193	V_{CC}
11	V_{SS}	72	V_{CC}	133	DQ12	194	RAS#
12	DQ8	73	WE#	134	DQ13	195	V_{CCQ}
13	DQ9	74	V_{CCQ}	135	V_{SS}	196	S0#
14	V_{SS}	75	CAS#	136	DM1	197	V_{CCQ}
15	DQS1#	76	V_{CCQ}	137	NC	198	ODT0
16	DQS1	77	NC	138	V_{SS}	199	A13
17	V_{SS}	78	NC	139	NC	200	V_{CC}
18	RESET#	79	V_{CCQ}	140	NC	201	NC
19	NC	80	NC	141	V_{SS}	202	V_{SS}
20	V_{SS}	81	V_{SS}	142	DQ14	203	DQ36
21	DQ10	82	DQ32	143	DQ15	204	DQ37
22	DQ11	83	DQ33	144	V_{SS}	205	V_{SS}
23	V_{SS}	84	V_{SS}	145	DQ20	206	DM4
24	DQ16	85	DQS4#	146	DQ21	207	NC
25	DQ17	86	DQS4	147	V_{SS}	208	V_{SS}
26	V_{SS}	87	V_{SS}	148	DM2	209	DQ38
27	DQS2#	88	DQ34	149	NC	210	DQ39
28	DQS2	89	DQ35	150	V_{SS}	211	V_{SS}
29	V_{SS}	90	V_{SS}	151	DQ22	212	DQ44
30	DQ18	91	DQ40	152	DQ23	213	DQ45
31	DQ19	92	DQ41	153	V_{SS}	214	V_{SS}
32	V_{SS}	93	V_{SS}	154	DQ28	215	DM5
33	DQ24	94	DQS5#	155	DQ29	216	NC
34	DQ25	95	DQS5	156	V_{SS}	217	V_{SS}
35	V_{SS}	96	V_{SS}	157	DM3	218	DQ46
36	DQS3#	97	DQ42	158	NC	219	DQ47
37	DQS3	98	DQ43	159	V_{SS}	220	V_{SS}
38	V_{SS}	99	V_{SS}	160	DQ30	221	DQ52
39	DQ26	100	DQ48	161	DQ31	222	DQ53
40	DQ27	101	DQ49	162	V_{SS}	223	V_{SS}
41	V_{SS}	102	V_{SS}	163	CB4	224	NC
42	CB0	103	SA2	164	CB5	225	NC
43	CB1	104	NC	165	V_{SS}	226	V_{SS}
44	V_{SS}	105	V_{SS}	166	DM8	227	DM6
45	DQS8#	106	DQS6#	167	NC	228	NC
46	DQS8	107	DQS6	168	V_{SS}	229	V_{SS}
47	V_{SS}	108	V_{SS}	169	CB6	230	DQ54
48	CB2	109	DQ50	170	CB7	231	DQ55
49	CB3	110	DQ51	171	V_{SS}	232	V_{SS}
50	V_{SS}	111	V_{SS}	172	NC	233	DQ60
51	NC	112	DQ56	173	V_{CCQ}	234	DQ61
52	V_{CCQ}	113	DQ57	174	NC	235	V_{SS}
53	CKE0	114	V_{SS}	175	V_{CC}	236	DM7
54	V_{CC}	115	DQS7#	176	NC	237	NC
55	NC	116	DQS7	177	NC	238	V_{SS}
56	NC/ERR_OUT	117	V_{SS}	178	V_{CCQ}	239	DQ62
57	V_{CCQ}	118	DQ58	179	A12	240	DQ63
58	A11	119	DQ59	180	A9	241	V_{SS}
59	A7	120	V_{SS}	181	V_{CC}	242	SDA
60	V_{CC}	121	SA0	182	A8	243	SCL
61	A5	122	SA1	183	A6	244	V_{CCSPD}

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
DQS0#-DQS8#	Data strobes complement
ODT0	On-die termination control
CK0,CK0#	Clock Inputs, positive line
CKE0	Clock Enables
S0#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input
DM (0-8)	Data Masks
V_{CCSPD}	SPD Power
V_{CC}	Core Power
V_{CCQ}	I/O Power
A10/AP	Address Input/Auto Precharge
V_{SS}	Ground
PAR_IN	Parity bit for the addess and control bus
ERR_OUT	Parity error found on the address and control bus
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Clock Input
NC	No connect
V_{REF}	Input/Output Reference

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms ±5% unless otherwise specified.

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{CC}	1 .7	1 .8	1 .9	V	1
I/O Supply voltage	V_{CCQ}	1 .7	1 .8	1 .9	V	4
V_{CCL} Supply voltage	V_{CCL}	1 .7	1 .8	1 .9	V	4
I/O Reference voltage	V_{REF}	0.49 x V_{CCQ}	0.50 x V_{CCQ}	0.51 x V_{CCQ}	V	2
I/O Termination voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF} + 0.04	V	3

Notes:

1. V_{CC} and V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
2. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not excedd ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{CCQ} tracks with V_{CC}; V_{CC}L track with V_{CC}.

ABSOLUTE MAXIMUM DC RATINGS

Symbol	Parameter		MIN	MAX	U nit
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-1.0	2.3	V
V_{CCQ}	Voltage on V_{CCQ} pin relative to V_{SS}		-0.5	2.3	V
V_{CCL}	Voltage on V_{CCL} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage temperature		-55	100	°C
T_{CASE}	Device operating temperature		0	85	°C
T_{OPR}	Operating temperature (ambient)		0	55	°C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-5	5	µA
		CK, CK#	-5	5	µA
		DM	-5	5	µA
I_{OZ}	Output leakage current; 0V<V_{OUT}<V_{CCQ}; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-18	18	µA

INPUT/OUTPUT CAPACITANCE

TA=25 0 C, f=1 00MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 - A1 3, BA0 - BA1 ,RAS#,CAS#,WE#)	C_{IN1}			pF
Input capacitance (CKE0), (ODT0)	C_{IN2}			pF
Input capacitance (CS0#)	C_{IN3}			pF
Input capacitance (CK0, CK0#)	C_{IN4}			pF
Input capacitance (DM0 - DM8), (DQS0 - DQS8)	C_{IN5}			pF
Input capacitance (DQ0 - DQ63), (CB0 - CB7)	C_{OUT1}			pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T_{OPER}	0°C to 85°C	°C	V

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. Forthe measurement conditions, please refer to JEDEC JESD51 .2
2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 125	V_{REF} + 300	mV
Input Low (Logic 0) Voltage	V_{IL}(DC)	-300	V_{REF} - 125	mV

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage (DDR2-400/533)	V_{IH}(AC)	V_{REF} + 250	—	mV
AC Input High (Logic 1) Voltage (DDR2-667)	V_{IH}(AC)	V_{REF} + 200		mV
AC Input Low (Logic 0) Voltage	V_{IL}(AC)	—	V_{REF} - 250	mV

DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only; T_A = 0°C, V_{CC} = 1.9V

Symbol	Parameter	Condition		806	667	534	403	Unit
I_{CC0}*	Operating one bank active-precharge;	$t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	810	720	720	mA
I_{CC1}*	Operating one bank active-read-precharge;	I_{OUT} = OmA; BL = 4; CL = CL(I_{CC}); $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; Data pattern is sames as I_{CC4W}.		TBD	945	855	810	mA
I_{CC2P}**	Precharge power-down current;	All banks idle; $t_{CK} = t_{CK(I_{CC})}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	45	45	45	mA
I_{CC2Q}**	Precharge quite standby current;	All banks idle; $t_{CK} = t_{CK(I_{CC})}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	450	360	315	mA
I_{CC2N}**	Precharge standby current;	All banks idle; $t_{CK} = t_{CK(I_{CC})}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING		TBD	495	405	360	mA
I_{CC3P}**	Active power-down current;	All banks open; $t_{CK} = t_{CK(I_{CC})}$, CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	315	270	225	mA
			Slow PDN Exit MRS(12) = 1	TBD	90	90	90	mA
I_{CC3N}**	Active standby current;	All banks open; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	585	495	405	mA
I_{CC4W}*	Operating burst write current;	All banks open; Continuous burst writes; BL = 4; CL = CL(I_{CC}); AL = 0; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1,395	1,170	990	mA
I_{CC4R}*	Operating burst read current;	All banks open; Continuous burst reads; TOUT = OmA; BL = 4; CL = CL(I_{CC}); AL = 0; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC4W}.		TBD	1,575	1,305	1,035	mA
I_{CC5}**	Burst auto refresh current;	$t_{CK} = t_{CK(I_{CC})}$; Refresh command at every $t_{RC(I_{CC})}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1,890	1,800	1,710	mA
I_{CC6}**	Self refresh current;	CK and CK# at OV; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	45	45	45	mA
I_{CC7}*	Operating bank interleave read curent;	All bank interleaving reads; I_{OUT} = OmA; BL = 4; CL = CL(I_{CC}); AL = $t_{RCD(I_{CC})}$ - 1*$t_{CK(I_{CC})}$; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RRD} = t_{RRD\ MIN(I_{CC})}$ = 1*$t_{CK(I_{CC})}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING		TBD	2,520	2,340	2,070	mA

Notes:

I_{CC} specification is based on **MICRON** components. Other DRAM manufacturers specification may be different.

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS

0°C ≤ T_{CASE} < +85°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

	AC CHARACTERISTICS			806		667		534		403			
	PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	Notes
Clock	Clock cycle time	CL = 6	$t_{CK\ (6)}$	TBD	TBD							ps	16, 24
		CL = 5	$t_{CK\ (5)}$	TBD	TBD	3,000	8,000					ps	16, 24
		CL = 4	$t_{CK\ (4)}$	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps	16, 24
		CL = 3	$t_{CK\ (3)}$	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps	16, 24
	CK high-level width		t_{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	18
	CK low-level width		t_{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	18
	Half clock period		t_{HP}	TBD	TBD	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps	19
Data	DQ output access time from CK/CK#		t_{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#		t_{HZ}	TBD	TBD		t_{AC} (MAX)		t_{AC} MAX		t_{AC} MAX	ps	8, 9
	Data-out low-impedance window from CK/CK#		t_{LZ}	TBD	TBD	t_{AC} (MIN)	t_{AC} (MAX)	t_{AC} (MIN)	t_{AC} (MAX)	t_{AC} (MIN)	t_{AC} (MAX)	ps	8, 10
	DQ and DM input setup time relative to DQS		t_{DSa}	TBD	TBD	300		350		400		ps	7, 15, 21
	DQ and DM input hold time relative to DQS		t_{DHa}	TBD	TBD	300		350		400		ps	7, 15, 21
	DQ and DM input setup time relative to DQS		t_{DSb}	TBD	TBD	100		100		150		t_{CK}	7, 15, 21
	DQ and DM input hold time relative to DQS		t_{QHb}	TBD	TBD	175		225		275		ps	7, 15, 21
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access relative to DQS		t_{DIPW}	TBD	TBD	0.35		0.35		0.35		ps	
	Data hold skew factor		t_{QHS}	TBD	TBD		340		400		450		
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	TBD	TBD	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}			15, 17
	Data valid output window (DVW)		t_{DVW}	TBD	TBD	t_{QH}-t_{DQSQ}		t_{QH}-t_{DQSQ}		t_{QH}-t_{DQSQ}			15, 17
Data Strobe	DQS input high pulse width		t_{DQSH}	TBD	TBD	0.35		0.35		0.35		t_{CK}	
	DQS input low pulse width		t_{DQSL}	TBD	TBD	0.35		0.35		0.35		t_{CK}	
	DQS output access time from CK/CK#		t_{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising– setup time		t_{DSS}	TBD	TBD	0.2		0.2		0.2		t_{CK}	
	DQS falling edge from CK rising – hold time		t_{DSH}	TBD	TBD	0.2		0.2		0.2		t_{CK}	
	DQS–DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	TBD	TBD		240		300		350	ps	15, 17
	DQS read preamble		t_{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	35

NOTE:

- AC specification is based on **MICRON** components. Other DRAM manufactures specification may be different.

AC TIMING PARAMETERS (Continued)

$0°C \le T_{CASE} < +85°C$; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

	AC CHARACTERISTICS		806		665		534		403			
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	Notes
Data Strobe	DQS read preamble	t_{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	35
	DQS write preamble setup time	t_{WPRES}	TBD	TBD	0		0		0		ps	12, 13, 36
	DQS write preamble	t_{WPRE}	TBD	TBD	0.35		0.25		0.25		t_{CK}	
	DQS write postamble	t_{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	11
	Write command to first DQS latching transition	t_{DQSS}	TBD	TBD	WL-0.25		WL-0.25		WL-0.25		t_{CK}	
Command and Address	Address and control input pulse width for each input	t_{IPW}	TBD	TBD	0.6		0.6		0.6		t_{CK}	
	Address and control input setup time	t_{ISa}	TBD	TBD	400		500		600		ps	6, 21
	Address and control input hold time	t_{IHa}	TBD	TBD	400		500		600		ps	6, 21
	Address and control input setup time	t_{ISb}	TBD	TBD	200		250		350		ps	6, 21
	Address and control input hold time	t_{IHb}	TBD	TBD	275		375		475		ps	6, 21
	CAS# to CAS# command delay	t_{CCD}	TBD	TBD	2		2		2		t_{CK}	
	Active to Active (same bank) command	t_{RC}	TBD	TBD	55		55		55		ns	33
	Active bank a to Active b bank command	t_{RRD}	TBD	TBD	7.5		7.5		7.5		ns	27
	Active to Read or Write delay	t_{RCD}	TBD	TBD	15		15		15		ns	
	Four Bank Activate period	t_{FAW}	TBD	TBD	37.5		37.5		37.5		ns	30
	Active to precharge command	t_{RAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns	20, 33
	Internal Read to precharge command delay	t_{RTP}	TBD	TBD	7.5		7.5		7.5		ns	23, 27
	Write recovery time	t_{WR}	TBD	TBD	15		15		15		ns	27
	Auto precharge wirte recovery and precharge time	t_{DAL}	TBD	TBD	$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		ns	22
	Interval Write to Read command delay	t_{WTR}	TBD	TBD	10		7.5		10		ns	27
	Precharge command period	t_{RP}	TBD	TBD	15		15		15		ns	31
	Precharge All command period	t_{RPA}	TBD	TBD	$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		ns	31
	Load Mode command cycle time	t_{MRD}	TBD	TBD	2		2		2		t_{CK}	
	CKE low to CK,CK# uncertainty	t_{DELAY}	TBD	TBD	$t_{IS}+t_{CK}+t_{IH}$		$t_{IS}+t_{CK}+t_{IH}$		$t_{IS}+t_{CK}+t_{IH}$		ns	28

NOTE:

- AC specification is based on **MICRON** components. Other DRAM manufactures specification may be different.

AC TIMING PARAMETERS (Continued)

$0°C \le T_{CASE} < +85°C$; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

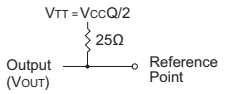
	AC CHARACTERISTICS		806		665		534		403			
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	Notes
Self Refresh	Refresh to Active or Refresh to Refresh command interval	t_{RFC}	TBD	TBD	105	70,000	105	70,000	105	70,000	ns	14
	Average periodic refresh interval	t_{REFI}	TBD	TBD	200	7.8		7.8		7.8	µs	14
	Exit self refresh to non-read command	t_{XSNR}	TBD	TBD	$t_{RFC\ (MIN)}$+10		$t_{RFC\ (MIN)}$+10		$t_{RFC\ (MIN)}$+10		ns	
	Exit self refresh to read command	t_{XSRD}	TBD	TBD	200		200		200		t_{CK}	
	Exit self refresh timing reference	t_{ISXR}	TBD	TBD	t_{IS}		t_{IS}		t_{IS}		ps	6, 29
ODT	ODT turn-on delay	t_{AOND}	TBD	TBD	2	2	2	2	2	2	t_{CK}	
	ODT turn-on	t_{AON}	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +700	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +1,000	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +1,000	ps	25
	ODT turn-off delay	t_{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}	
	ODT turn-off	t_{AOF}	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +600	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +600	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +600	ps	26
	ODT turn-on (power-down mode)	t_{AONPD}	TBD	TBD	$t_{AC(MIN)}$ +2,000	2x t_{CK} + $t_{AC\ (MAX)}$ + 1,000	$t_{AC(MIN)}$ +2,000	2x t_{CK} + $t_{AC\ (MAX)}$ + 1,000	$t_{AC(MIN)}$ +2,000	2x t_{CK} + $t_{AC\ (MAX)}$ + 1,000	ps	
	ODT turn-off (power-down mode)	t_{AOFPD}	TBD	TBD	$t_{AC(MIN)}$ +2,000	2x t_{CK} + $t_{AC\ (MAX)}$ + 1,000	$t_{AC(MIN)}$ +2,000	2x t_{CK} + $t_{AC\ (MAX)}$ + 1,000	$t_{AC(MIN)}$ +2,000	2x t_{CK} + $t_{AC\ (MAX)}$ + 1,000	t_{CK}	
	ODT to power-down entry latency	t_{ANPD}	TBD	TBD	3		3		3		t_{CK}	
	ODT power-down exit latency	t_{AXPD}	TBD	TBD	8		8		8		t_{CK}	
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	TBD	TBD	2		2		2		t_{CK}	
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	TBD	TBD	7-AL		6-AL		6-AL		t_{CK}	
	Exit precharge power-down to any non-READ command.	t_{XP}	TBD	TBD	2		2		2		t_{CK}	
	CKE minimum high/low time	t_{CKE}	TBD	TBD	3		3		3		t_{CK}	34

NOTE:

- AC specification is based on **MICRON** components. Other DRAM manufactures specification may be different.

Notes

1. All voltages referenced to V_{SS}
2. Tests for AC timing, I_{CC}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{CC} tests may use a V_{IL} to V_{IH} swing of up to 1.0V in the test environment parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between V_{IL} (AC) and V_{IH} (AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Command/Address minimum input slew rate is at 1.0V/ns. Command/Address input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated using t_{ISb} and the Setup and Hold Time Derating Values table. t_{IS} timing (t_{ISb}) is referenced from V_{IH} (AC) for a rising signal and V_{IL} (AC) for a falling signal. t_{IH} timming (t_{IHb}) is referenced from V_{IH} (AC) for a rising signal and V_{IL} (DC) for a falling signal. The timing table also lists the t_{ISb} and t_{IHb} values for a 1.0V/ns slew rate; these are the “base” values.
7. Data minimum input slew rate is at 1.0V/ns. Data input timing must be derated if the slew rate is not 1.0V/ns. This is easily accommodated if the timing is referenced from the logic trip points. t_{DS} timing (t_{DSb}) is referenced from V_{IH} (AC) for a rising signal and V_{IL} (AC) for a falling signal. t_{IH} timing (t_{IHb}) is referenced from V_{IH} (DC) for a risng signal and V_{IL} (DC) for a falling signal. The timing table lists the t_{DS}b and t_{DH}b values for a 1.0V/ns slew rate. If the DQS/DQS# differential strobe feature is not enabled, timing is no longer referenced to the crosspoint of DQS/DQS#. Data timing is now referenced to V_{REF}, provided the DQS slew rate is not less than 1.0V/ns. If the DQS slew rate is less than 1.0V/ns, then data timing is now referenced to V_{IH} (AC) for a rising DQS and V_{IL} (DC) for a falling DQS.
8. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (when the device output is no longer driving (t_{HZ}) or begins driving (t_{LZ}).
9. This maximum value is derived from the referenced test load. t_{HZ} (MAX) will prevail over t_{DQSCK} (MAX) + t_{RPST} (MAX) condition.
10. t_{LZ} (MIN) t_{LZ} will prevail over a t_{DQSCK} (MIN) + t_{RPRE} (MAX) condition.
11. The intent of the Don’t Care state after completion of the postamble is the DQS-driven signal should either be high, low or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above V_{IH} DC (MIN) then it must not transition low (below V_{IH} (DC) prior to t_{DQSH} (MIN).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turn around.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DQSS}.
14. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, a REFRESH command must be asserted at least once every 70.3µs or t_{RFC} (MAX). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms.
15. Each half-byte lane has a corresponding DQS.
16. CK and CK# input slew rate must be ≥ 1V/ns (≥ 2V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications - t_{HP}. (t_{CK}/2), t_{DQSQ}, and t_{QH} (t_{QH} = t_{HP} - t_{QHS}). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. This value can be greater than the minimum specification limits for t_{CL} and t_{CH}. For example, t_{CL} and t_{CH} are = 50 percent of the period, less the half period jitter [t_{JIT}(HP)] of the clock source, and less the half period jitter due to cross talk [t_{JIT}(cross talk)] into the clock traces.
19. t_{HP} (MIN) is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK# inputs.
20. READs and WRITEs with auto precharge are allowed to be issued before tRAS (MIN) is satisfied since t_{RAS} lockout feature is supported in DDR2 SDRAM devices.
21. V_{IL}/V_{IH} DDR2 overshoot/undershoot. REFER to the 512Mb DDR2 SDRAM data sheet for more detail.
22. t_{DAL} = (nWR) + (t_{RP}/t_{CK}): For each of the terms above, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period; nWR refers to the t_{WR} parameter stored in the MR[11,10,9]. Example: For 534 at t_{CK}= 3.75 ns with t_{WR} programmed to four clocks. t_{DAL} = 4 + (15 ns/3.75ns) clock = 4 + (4) clocks = 8 clocks.
23. The minimum READ to internal PRECHARGE time. This parameter is only applicable when t_{RTP}/2*t_{CK}) > 1. If t_{RTP}/2*t_{CK}) ≤ 1, then equation AL + BL/2 applies. Notwithstanding, t_{RAS} (MIN) has to be satisfied as well. The DDR2 SDRAM device will automatically delay the internal PRECHARGE command until t_{RAS} (MIN) has been satisfied.
24. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, and system reset condition.
25. ODT turn-on time t_{AON} (MIN) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn-on time t_{AON} (MAX) is when the ODT resistance is fully on. Both are measured from t_{AOND}.

26. ODT turn-off time t_{AOF} (MIN) is when the device starts to turn off ODT resistance. ODT turn off time t_{AOF} (MAX) is when the bus is in high impedance. Both are measured from t_{AOFD}.
27. This parameter has a two clock minimum requirement at any t_{CK}.
28. t_{DELAY} is calculated from t_{IS} + t_{CK} + t_{IH} so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.
29. t_{ISXR} is equal to t_{IS} and is used for CKE setup time during self refresh exit.
30. No more than 4 bank ACTIVE commands may be issued in a given t_{FAW} (MIN) period. t_{RRRD} (MIN) restriction still applies. The t_{FAW} (MIN) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
31. t_{RPA} timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, t_{RP} timing applies. t_{RPA} (MIN) applies to all 8-bank DDR2 devices.
32. Value is minimum pulse width, not the number of clock registrations.
33. Applicable to Read cycles only. Write cycles generally require additional time due to Write recovery time (t_{WR}) during arto precharge.
34. t_{CKE} (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2* t_{CK} + t_{IH}.
35. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving (t_{RPST}) or beginning to drive (t_{RPRE}).
36. When DQS is used single-ended, the minimum limit is reduced by 100ps.

ORDERING INFORMATION FOR AD7

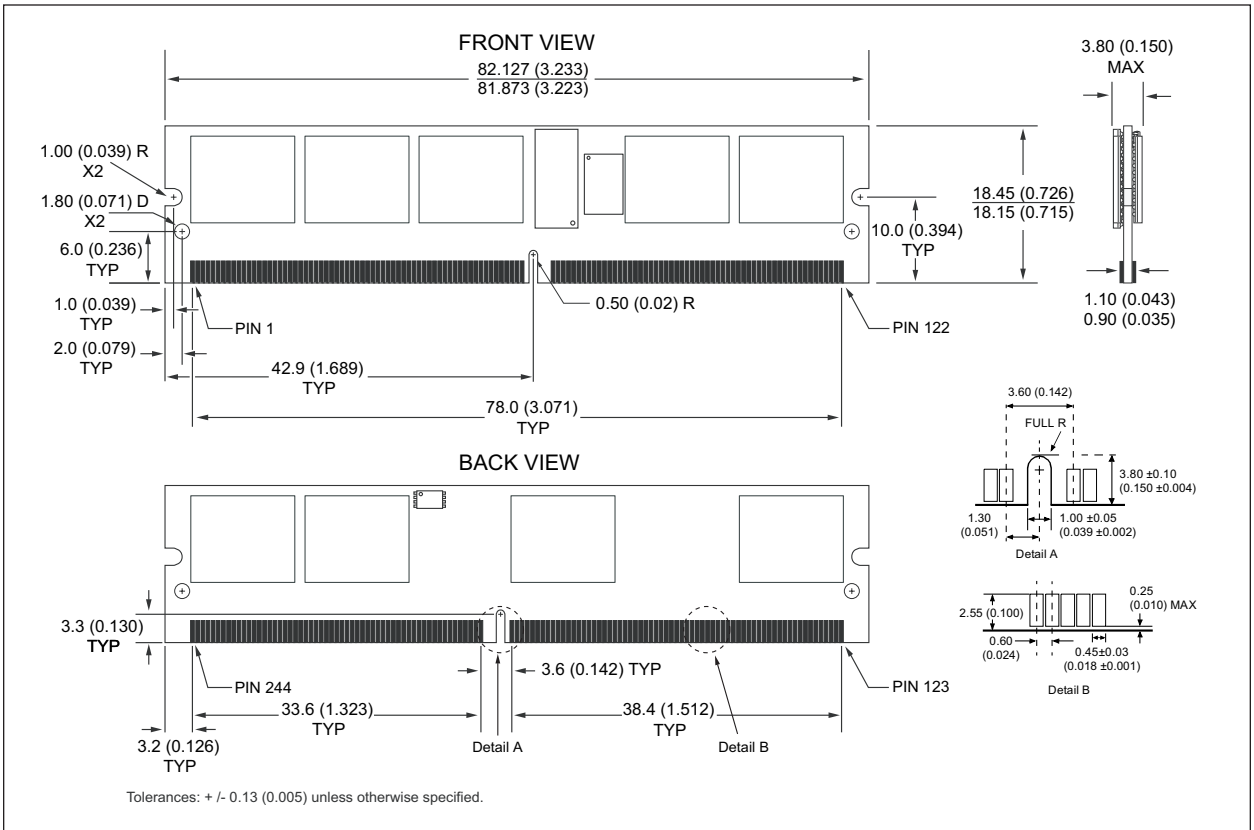
Part Number	Speed/Data Rate	CAS Latency	t_{RCD}	t_{RP}	Height*
W3HG64M72EER806AD7xG**	400MHz/800Mb/s	6	6	6	18.29mm (0.72")
W3HG64M72EER665AD7xG**	333MHz/667Mb/s	5	5	5	18.29mm (0.72")
W3HG64M72EER534AD7xG	266MHz/533Mb/s	4	4	4	18.29mm (0.72")
W3HG64M72EER403AD7xG	200MHz/400Mb/s	3	3	3	18.29mm (0.72")

**Contact factory for availability.

NOTES:

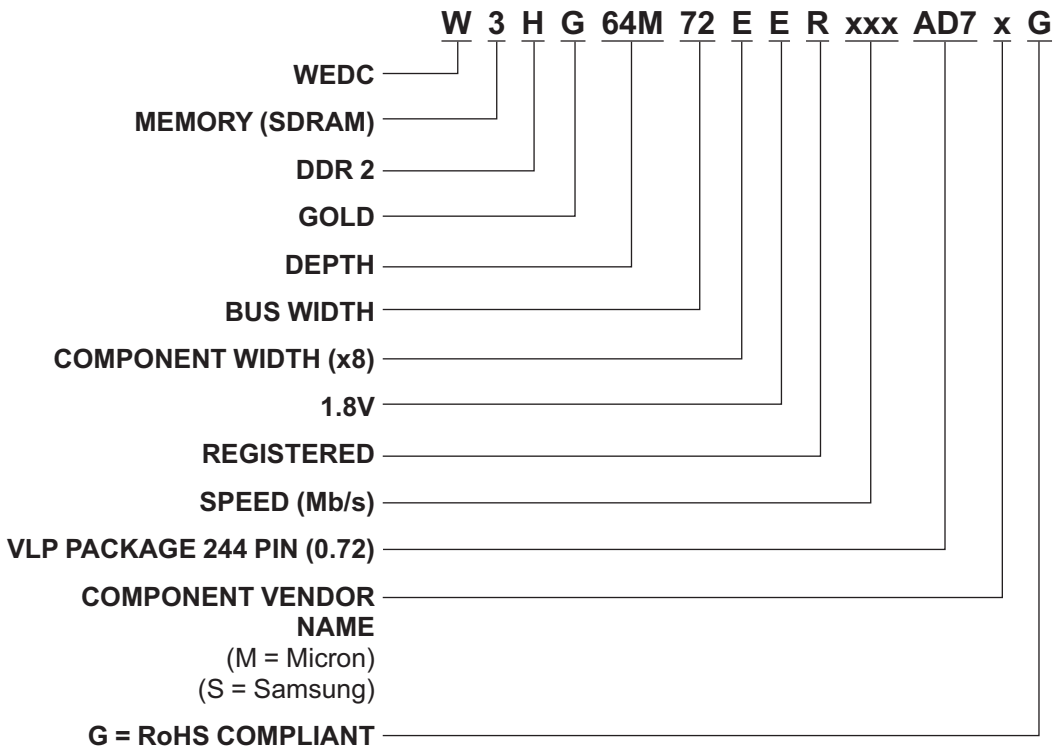
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR VLP AD7



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL, VLP Mini-DIMM

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	September 2005	Advanced
Rev 1	1.1 Updated I_{CC} and AC specs	December 2005	Advanced