



CMOS/BI-DIRECTIONAL BUS INTERFACE REGISTERS

KEY FEATURES

- Two Banks of 8 × 16 Registers
- Contents of Each Register Available at Output
- Provides Temporary Address or Data Storage Between Two Processor Ports or Buses
- Bi-Directional Buses Interface — Dual 4-Deep or 8-Deep Registers in Each Direction
- Separate Control for Each Register Bank
- Direct Processor Bus-to-Bus Interface
- TTL Compatible
- Replaces Eight WS59520's

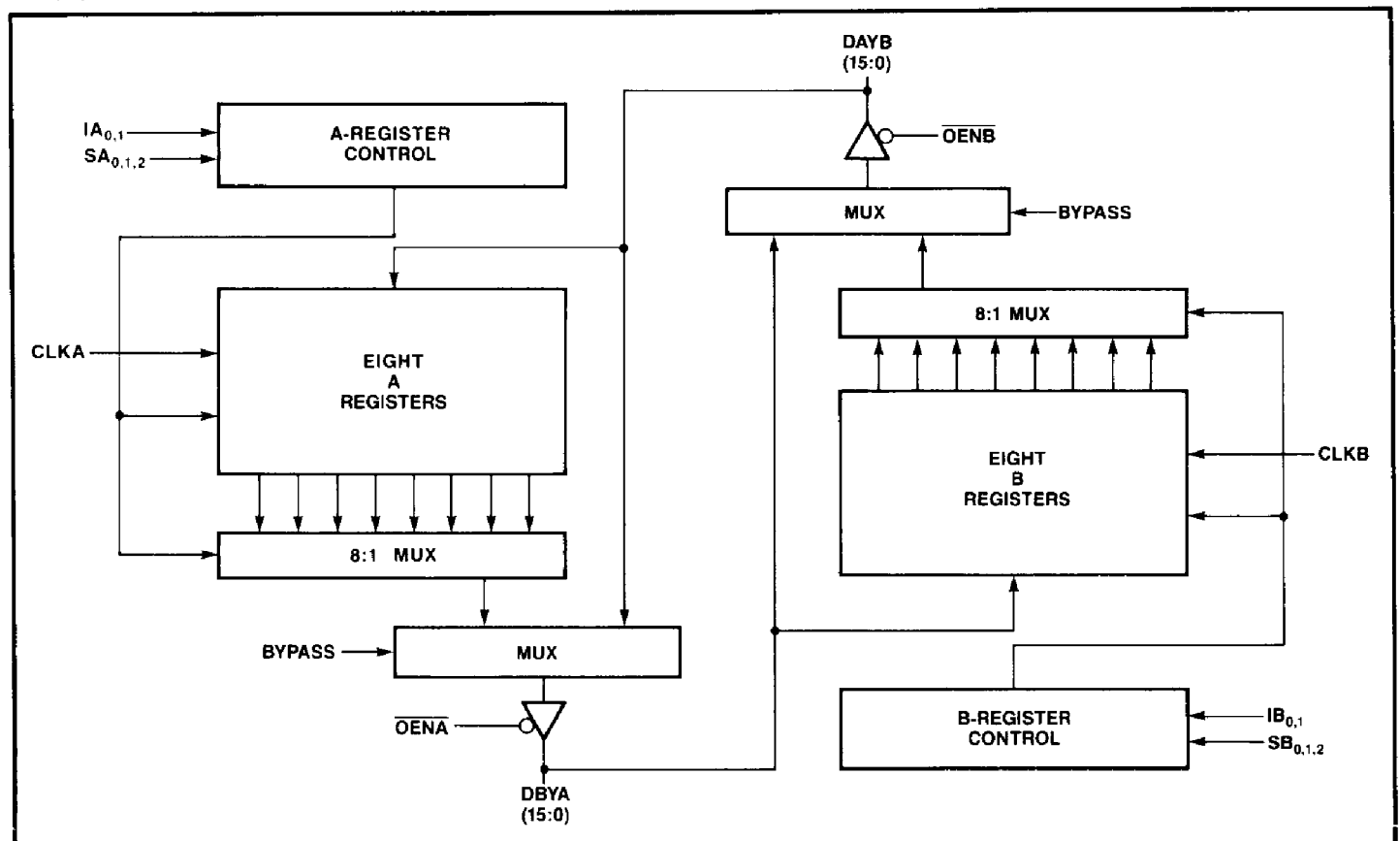
GENERAL DESCRIPTION

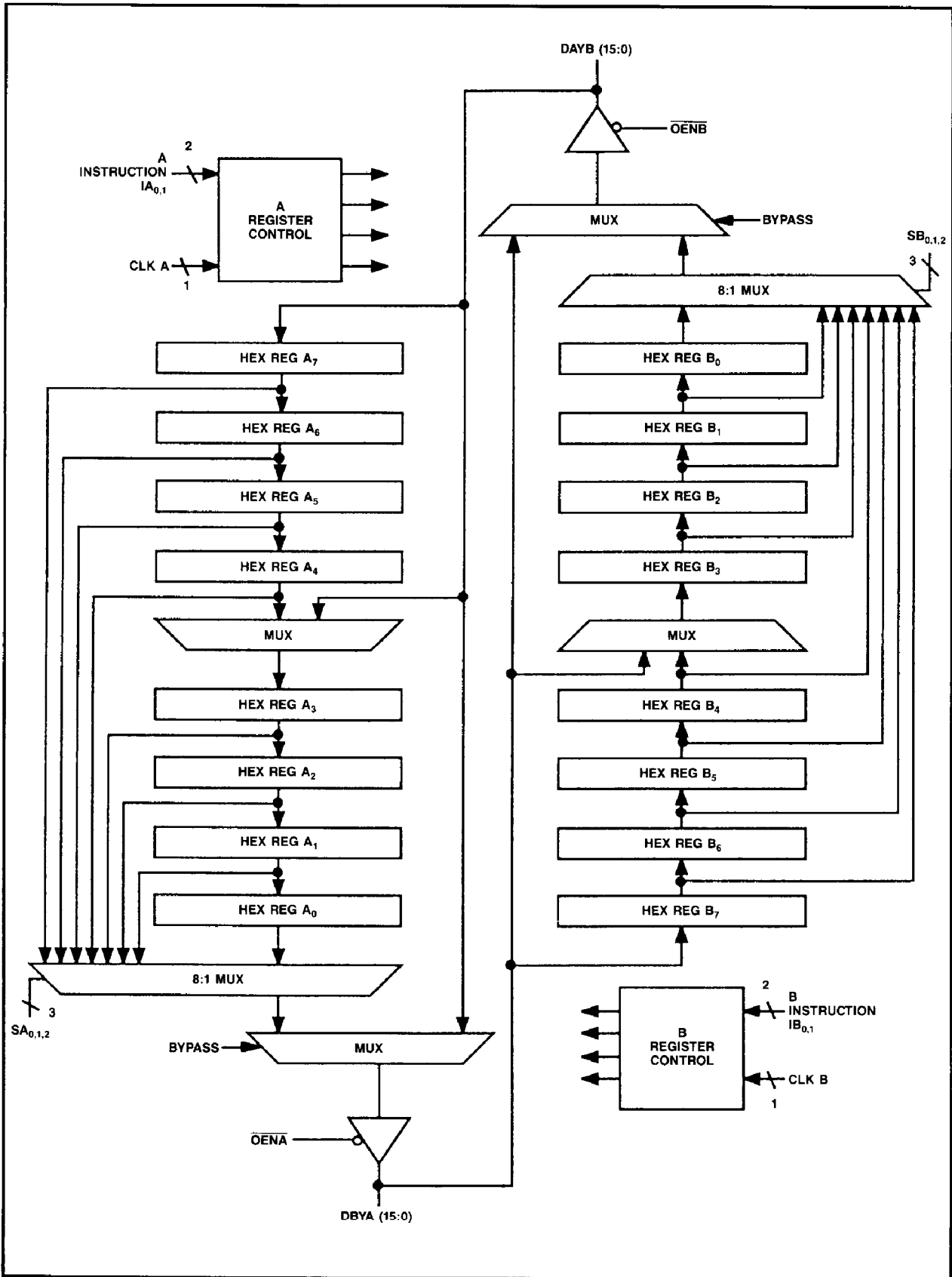
The WS59820/WS59820B consists of two banks of registers, eight registers in each bank, each register 16 bits wide. A single bank can be configured as an eight level pipeline or two each four level pipelines. The architectural configuration is determined by the instruction inputs (I0 and I1) for each register bank.

Each of the eight registers in each bank is available at the multiplexed output. The output register is determined by the control inputs (S0, S1, and S2) for each register bank. The multiplexed output is 16 bits wide and is enabled by the \overline{OEN} signal. Each bank of registers has its own clock (CLK), instruction inputs (I0-1) and multiplex controls.

The WS59820 and WS59820B differ only in pin assignments. The WS59820B has additional V_{CC} and ground pin assignments and is recommended for new designs.

BLOCK DIAGRAM



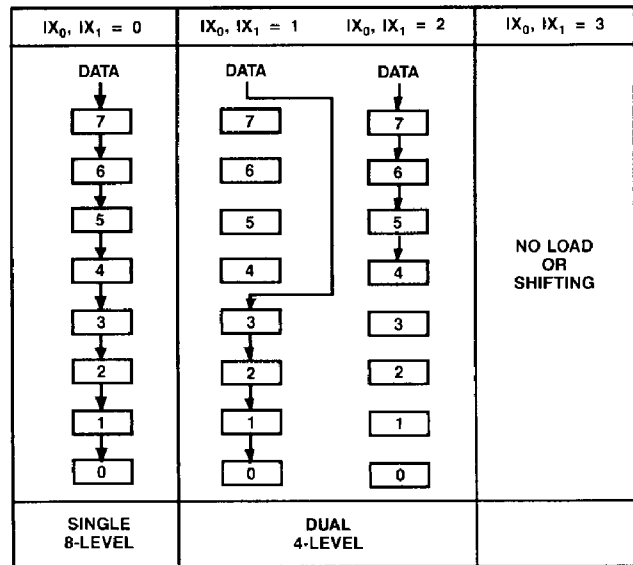


SELECTION TABLE FOR REGISTER A OR B

SX2	SX1	SX0	REGISTER SELECTED
0	0	0	REG 0
0	0	1	REG 1
0	1	0	REG 2
0	1	1	REG 3
1	0	0	REG 4
1	0	1	REG 5
1	1	0	REG 6
1	1	1	REG 7

X = Register A or B.

REGISTER SHIFT OPTIONS FOR REGISTERS A OR B



X = Register A or B.

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MULTIPLEX CONTROL

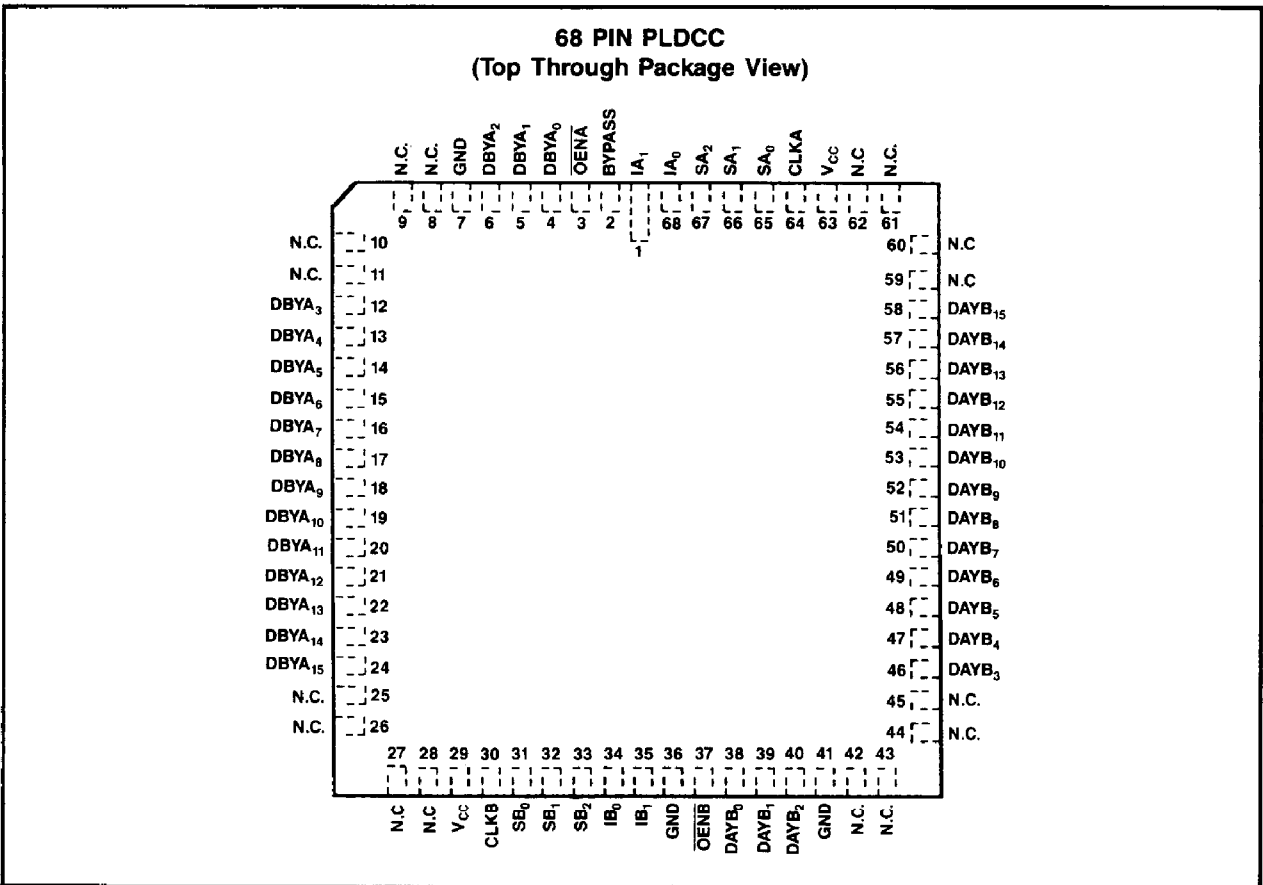
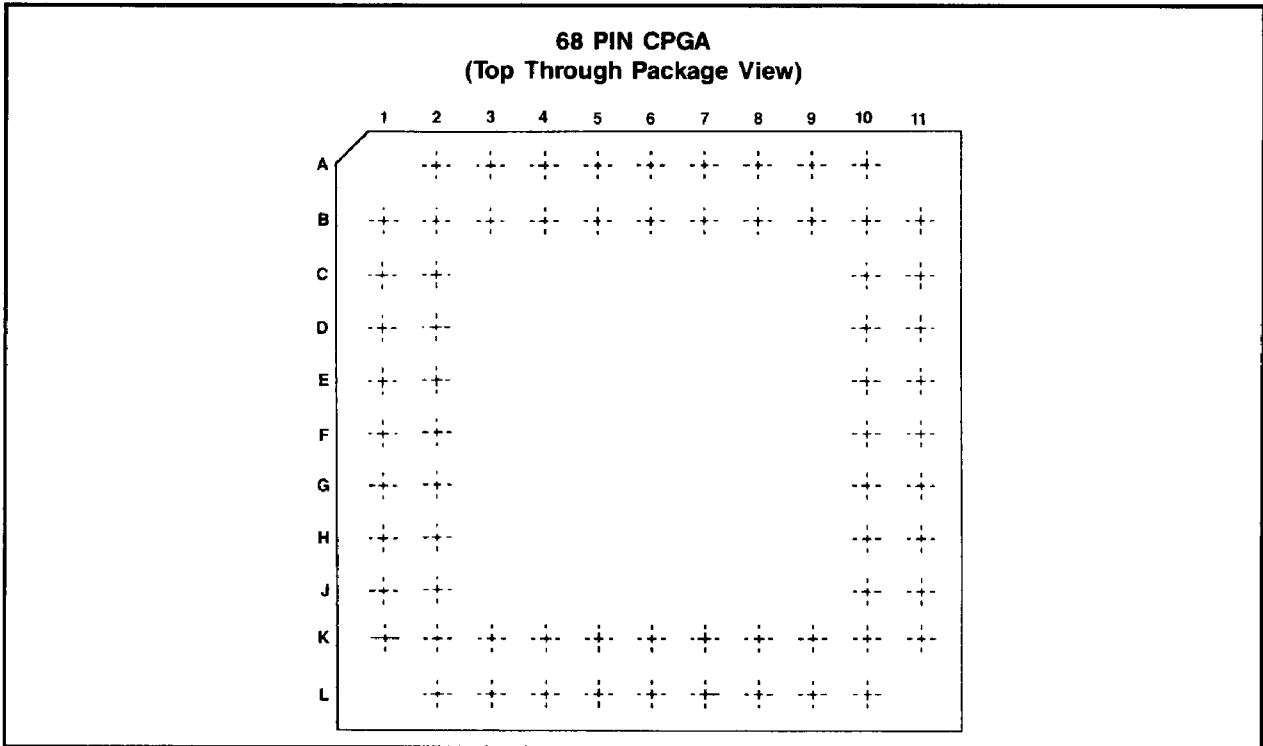
\overline{OENA}	\overline{OENB}	BYPASS	OPERATION
0	0	1	Pass Output of 8:1 Muxes to Outputs
0	0	0	Not Allowed (Input is Preferred)
0	1	0	Pass Input From DAYB (15:0) to Output DBYA (15:0)
0	1	1	Pass Output From 8:1 Mux to Outputs DBYA (15:0)
1	0	0	Pass Input From DBYA (15:0) to Output DAYB (15:0)
1	0	1	Pass Output From 8:1 Mux to Outputs DAYB (15:0)
1	1	X	Inhibit Outputs (High Impedance)

PIN DESCRIPTION

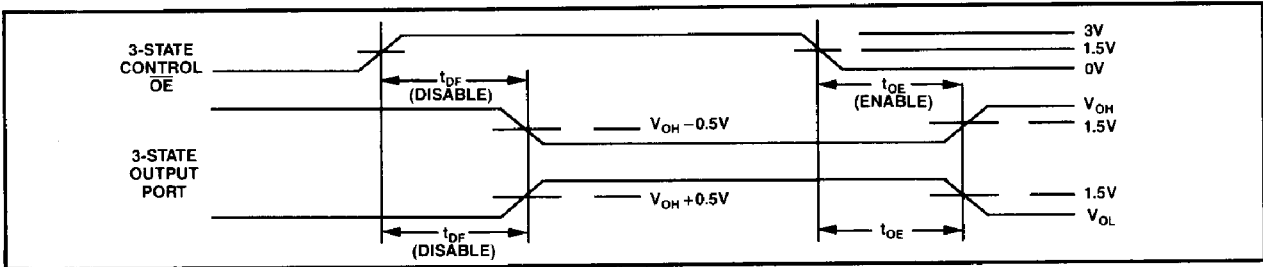
SIGNAL NAME	I/O	DESCRIPTION
IA ₀ , IA ₁	I	Instruction Inputs for Register Bank A
IB ₀ , IB ₁	I	Instruction Inputs for Register Bank B
SA ₀ -SA ₂	I	Multiplex Select for Register Bank A
SB ₀ -SB ₂	I	Multiplex Select for Register Bank B
\overline{OENA}	I	Output Enable for Output Port DBYA
\overline{OENB}	I	Output Enable for Output Port DAYB
CLKA	I	Clock Input for Register Bank A
CLKB	I	Clock Input for Register Bank B
DBYA 15:0	I/O	Register Bank B Input Port, Register Bank A Output Port
DAYB 15:0	I/O	Register Bank A Input Port, Register Bank B Output Port
BYPASS	I	BYPASS Control (Active Low). See Table on Output Control



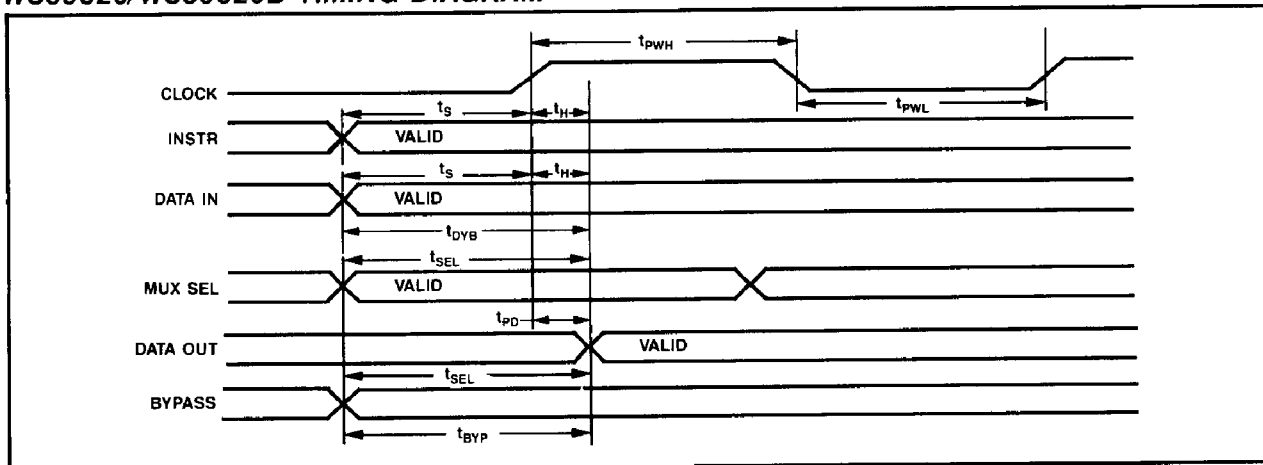
PACKAGE ORIENTATION (WS59820)



WS59820/WS59820B THREE STATE TIMING



WS59820/WS59820B TIMING DIAGRAM



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68 PIN CPGA PIN DESIGNATOR (WS59820)

PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A ₆	IA ₁	B ₆	BYPASS	A ₅	$\overline{O}ENA$	B ₅	DBYA ₀
A ₄	DBYA ₁	B ₄	DBYA ₂	A ₃	GND	B ₃	Not Used
A ₂	Not Used	B ₁	Not Used	B ₂	Not Used	C ₁	DBYA ₃
C ₂	DBYA ₄	D ₁	DBYA ₅	D ₂	DBYA ₆	E ₁	DBYA ₇
E ₂	DBYA ₈	F ₁	DBYA ₉	F ₂	DBYA ₁₀	G ₁	DBYA ₁₁
G ₂	DBYA ₁₂	H ₁	DBYA ₁₃	H ₂	DBYA ₁₄	J ₁	DBYA ₁₅
J ₂	Not Used	K ₁	Not Used	L ₂	Not Used	K ₂	Not Used
L ₃	V _{CC}	K ₃	CLKB	L ₄	SB ₀	K ₄	SB ₁
L ₅	SB ₂	K ₅	IB ₀	L ₆	IB ₁	K ₆	GND
L ₇	$\overline{O}ENB$	K ₇	DAYB ₀	L ₈	DAYB ₁	K ₈	DAYB ₂
L ₉	GND	K ₉	Not Used	L ₁₀	Not Used	K ₁₁	Not Used
K ₁₀	Not Used	J ₁₁	DAYB ₃	J ₁₀	DAYB ₄	H ₁₁	DAYB ₅
H ₁₀	DAYB ₆	G ₁₁	DAYB ₇	G ₁₀	DAYB ₈	F ₁₁	DAYB ₉
F ₁₀	DAYB ₁₀	E ₁₁	DAYB ₁₁	E ₁₀	DAYB ₁₂	D ₁₁	DAYB ₁₃
D ₁₀	DAYB ₁₄	C ₁₁	DAYB ₁₅	C ₁₀	Not Used	B ₁₁	Not Used
A ₁₀	Not Used	B ₁₀	Not Used	A ₉	V _{CC}	B ₉	CLKA
A ₈	SA ₀	B ₈	SA ₁	A ₇	SA ₂	B ₇	IA ₀



ABSOLUTE MAXIMUM RATINGS*

Operating Temp. (Comm'l) 0°C to +70°C
 (Mil) -55°C to +125°C
 Storage Temp. (No Bias) -65°C to +150°C
 Voltage on any pin with
 respect to GND -0.6V to +7V
 Latch Up Protection > 200 mA
 ESD Protection > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Range (See Notes)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V _{OH}	Output High Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6.5 mA	2.4		V
V _{OL}	Output Low Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 mA Comm'l I _{OL} = 16 mA Mil		0.5	
V _{IH}	Input High Voltage	Guaranteed Input High Voltage		2.0		V
V _{IL}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	
I _{IX}	Input Load Current	V _{CC} = Max, V _{IN} = GND or V _{CC}		-10	10	μA
I _{OZ}	High Impedance Output Current	V _{CC} = Max, V _O = GND or V _{CC}		-50	50	
I _{CC}	Power Supply Current	V _{CC} = Max	0°C to +70°C (Comm'l)		12	mA
			-55°C to +125°C (Mil)		15	

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 3) C_L = 50 pF except for t_{DF} where C_L = 5 pF.
 2) Military: V_{CC} = +5V ± 10%, T_A = -55°C to +125°C.

SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

PARAMETER	DESCRIPTION	WS59820/WS59820B				UNITS
		COMMERCIAL		MILITARY		
		MIN	MAX	MIN	MAX	
t _{PD}	Clock to Data Out		20		22	ns
t _{SEL}	Mux Select to Data Out		20		22	
t _S	Input (Data/Instr.) Set Up	8		10		
t _H	Input (Data/Instr.) Hold	5		5		
t _{DF}	Output Disable	5	15		16	
t _{OE}	Output Enable	5	18		22	
t _{PWH}	Clock Pulse Width High	10		12		
t _{PWL}	Clock Pulse Width Low	11		12		
t _{BYP}	Bypass to Data Out		30		35	
t _{DYB}	Data Via BYPASS (Data In to Data Out When BYPASS is Active Low)		15		18	

NOTE: Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

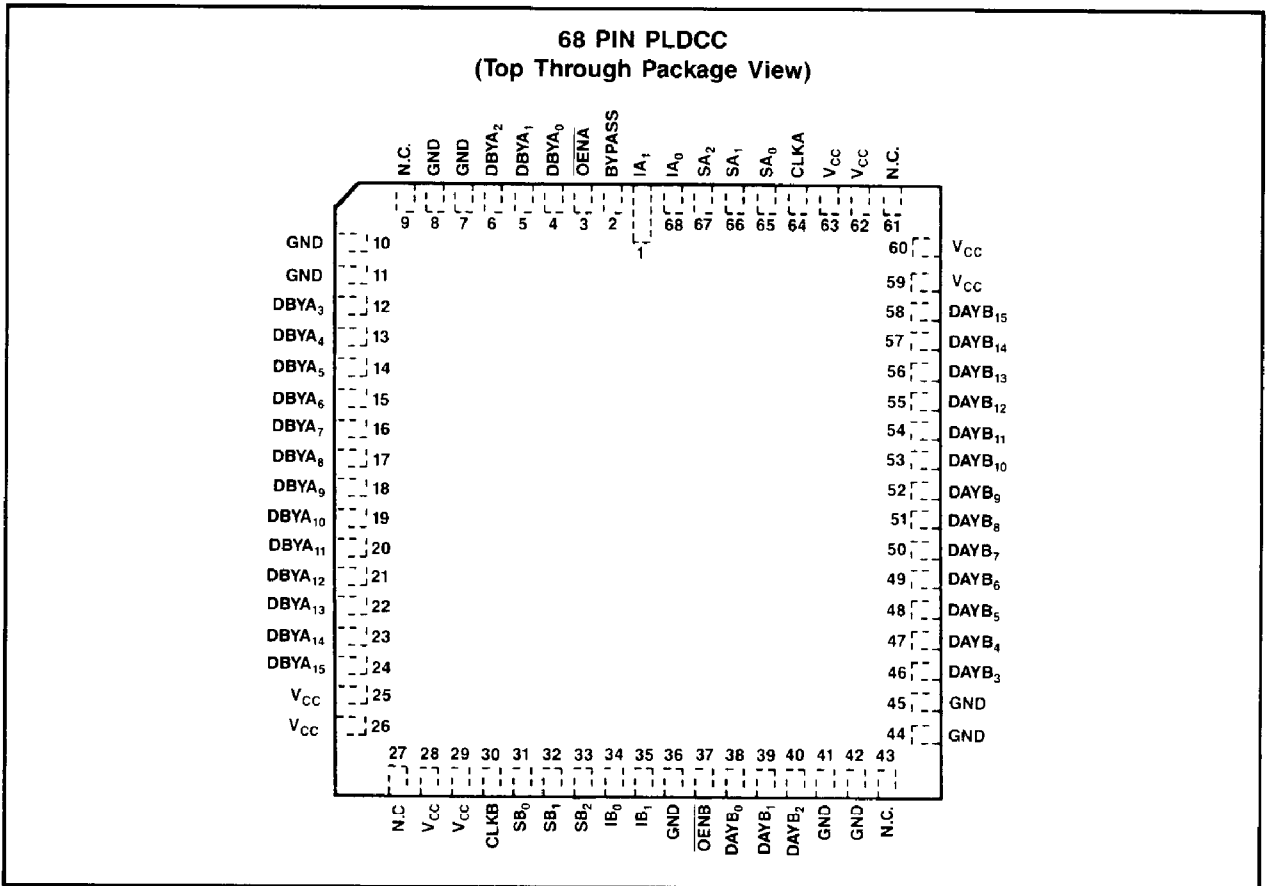
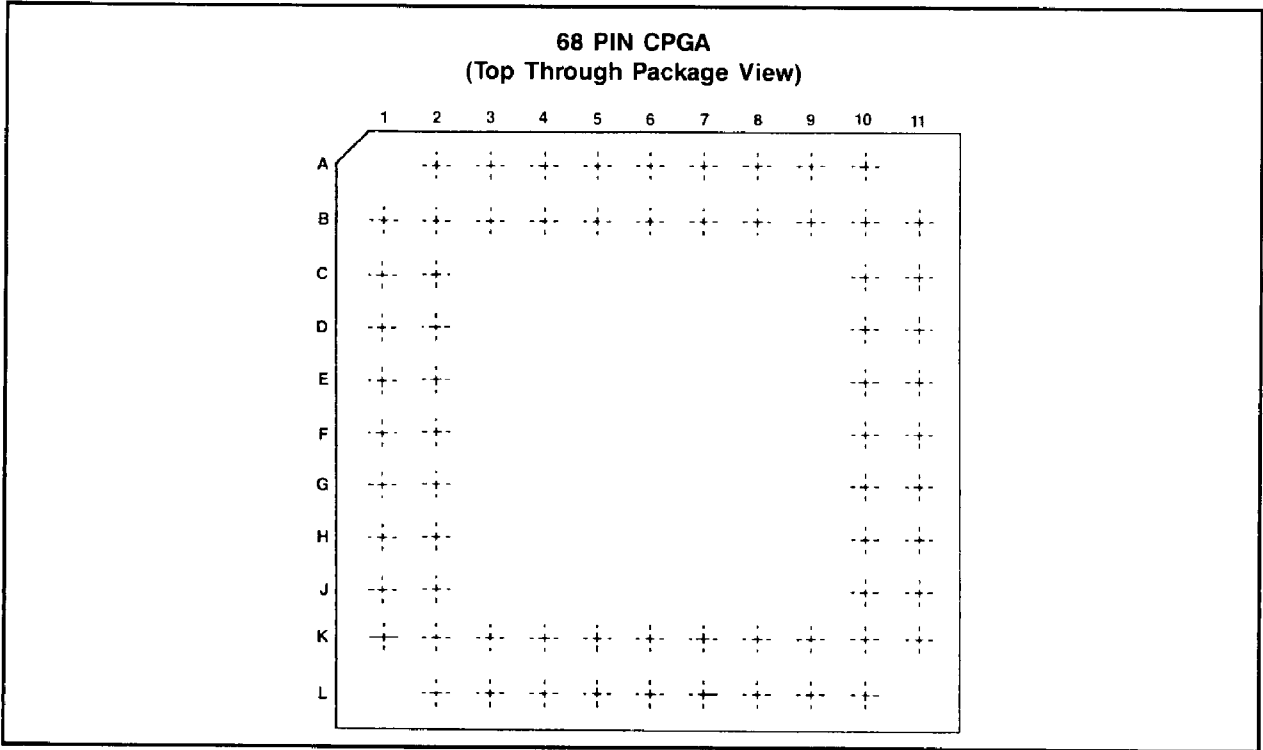


68 PIN CPGA PIN DESIGNATOR (WS59820B)

PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A ₆	IA ₁	B ₆	BYPASS	A ₅	$\overline{\text{OENA}}$	B ₅	DBYA ₀
A ₄	DBYA ₁	B ₄	DBYA ₂	A ₃	GND	B ₃	GND
A ₂	Not Used	B ₁	GND	B ₂	GND	C ₁	DBYA ₃
C ₂	DBYA ₄	D ₁	DBYA ₅	D ₂	DBYA ₆	E ₁	DBYA ₇
E ₂	DBYA ₈	F ₁	DBYA ₉	F ₂	DBYA ₁₀	G ₁	DBYA ₁₁
G ₂	DBYA ₁₂	H ₁	DBYA ₁₃	H ₂	DBYA ₁₄	J ₁	DBYA ₁₅
J ₂	V _{CC}	K ₁	V _{CC}	L ₂	Not Used	K ₂	V _{CC}
L ₃	V _{CC}	K ₃	CLKB	L ₄	SB ₀	K ₄	SB ₁
L ₅	SB ₂	K ₅	IB ₀	L ₆	IB ₁	K ₆	GND
L ₇	OENB	K ₇	DAYB ₀	L ₈	DAYB ₁	K ₈	DAYB ₂
L ₉	GND	K ₉	GND	L ₁₀	Not Used	K ₁₁	GND
K ₁₀	GND	J ₁₁	DAYB ₃	J ₁₀	DAYB ₄	H ₁₁	DAYB ₅
H ₁₀	DAYB ₆	G ₁₁	DAYB ₇	G ₁₀	DAYB ₈	F ₁₁	DAYB ₉
F ₁₀	DAYB ₁₀	E ₁₁	DAYB ₁₁	E ₁₀	DAYB ₁₂	D ₁₁	DAYB ₁₃
D ₁₀	DAYB ₁₄	C ₁₁	DAYB ₁₅	C ₁₀	V _{CC}	B ₁₁	V _{CC}
A ₁₀	Not Used	B ₁₀	V _{CC}	A ₉	V _{CC}	B ₉	CLKA
A ₈	SA ₀	B ₈	SA ₁	A ₇	SA ₂	B ₇	IA ₀

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PACKAGE ORIENTATION (WS59820B)



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59820G	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820J	23	68 Pin PLDCC	J5	Comm'l	Standard
WS59820BG	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820BJ	23	68 Pin PLDCC	J5	Comm'l	Standard