



Monolithic N-Channel JFET Duals

SST5198NL
SST5199NL

U5196NL
U5197NL

U5198NL
U5199NL

PRODUCT SUMMARY					
Part Number	V _{GS(off)} (V)	V _{(BR)GSS} Min (V)	g _{fs} Min (mS)	I _G Max (pA)	V _{GS1} - V _{GS2} Max (mV)
U5196NL	-0.7 to -4	-50	1	-15	5
U5197NL	-0.7 to -4	-50	1	-15	5
SST/U5198NL	-0.7 to -4	-50	1	-15	10
SST/U5199NL	-0.7 to -4	-50	1	-15	15

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 5 pA
- Low Noise
- High CMRR: 100 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

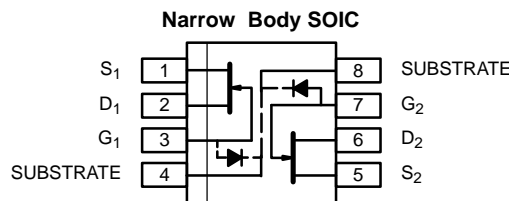
DESCRIPTION

The SST/U5196NL series of JFET duals are designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tightly matched specs, low gate leakage for accuracy, and wide dynamic range with I_G guaranteed at V_{DG} = 20 V.

Pins 4 and 8 of the SST series and pin 4 on the U series part numbers enable the substrate to be connected to a positive, external bias (V_{DD}) to avoid latchup.

The U series in the hermetically-sealed TO-78 package is available with full military processing. The SST series SO-8 package provides ease of manufacturing and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.

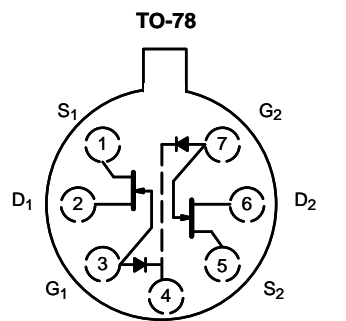
For similar products see the low-noise SST/U401NL series and the low-leakage U421NL/423NL data sheets.



Top View

Marking Codes:

SST5198NL - 5198NL
SST5199NL - 5199NL



Top View

U5196NL, U5198NL
U5197NL, U5199NL

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -50 V
 Gate Current 50 mA
 Lead Temperature (1/16" from case for 10 sec.) 300 °C
 Storage Temperature -65 to 200 °C
 Operating Junction Temperature -55 to 150 °C

Power Dissipation : Per Side^a 250 mW
 Total^b 500 mW

Notes

- a. Derate 2 mW/°C above 85 °C
- b. Derate 4 mW/°C above 85 °C



SPECIFICATIONS FOR U5196NL AND U5197NL (T _A = 25°C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Typ ^a	Limits				Unit
				U5196NL		U5197NL		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 20 V, I _D = 1 nA	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -30 V, V _{DS} = 0 V	-10		-25		-25	pA
		T _A = 150°C	-20		-50		-50	nA
Gate Operating Current	I _G	V _{DG} = 20 V, I _D = 200 μA	-5		-15		-15	pA
		T _A = 125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V _{GS}	V _{DG} = 20 V, I _D = 200 μA	-1.5	-0.2	-3.8	-0.2	-3.8	V
Dynamic								
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 20 V, V _{GS} = 0 V f = 1 kHz	3.0	1	4	1	4	mS
Common-Source Output Conductance	g _{os}		8		50		50	μS
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 20 V, I _D = 200 μA f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g _{os}		1		4		4	μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		1		2		2	
Equivalent Input Noise Voltage	e _n	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 kHz	11		20		20	nV/ √Hz
Noise Figure	NF	V _{DS} = 20 V, V _{GS} = 0 V f = 100 Hz, R _G = 10 MΩ			0.5		0.5	dB
Matching								
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 20 V, I _D = 200 μA			5		5	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 20 V, I _D = 200 μA T _A = -55 to 125°C			5		10	μV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 20 V, V _{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 20 V, I _D = 200 μA f = 1 kHz	0.99	0.97	1	0.97	1	
Differential Output Conductance	g _{os1} - g _{os2}		0.1		1		1	μS
Differential Gate Current	I _{G1} - I _{G2}	V _{DG} = 20 V, I _D = 200 μA, T _A = 125°C	0.1		5		5	nA
Common Mode Rejection Ratio	CMRR	V _{DG} = 10 to 20 V, I _D = 200 μA	100					dB



**SPECIFICATIONS FOR SST/U5198NL AND SST/U5199NL
(T_A = 25 °C UNLESS OTHERWISE NOTED)**

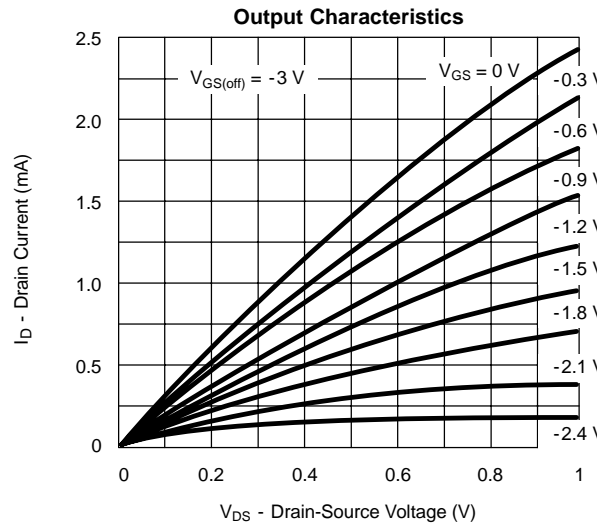
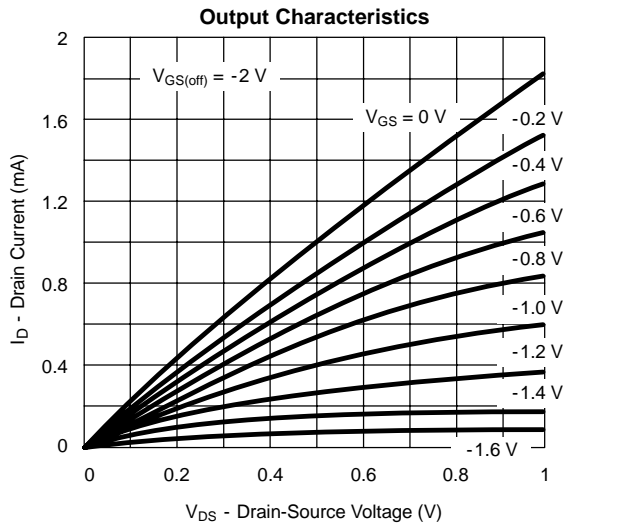
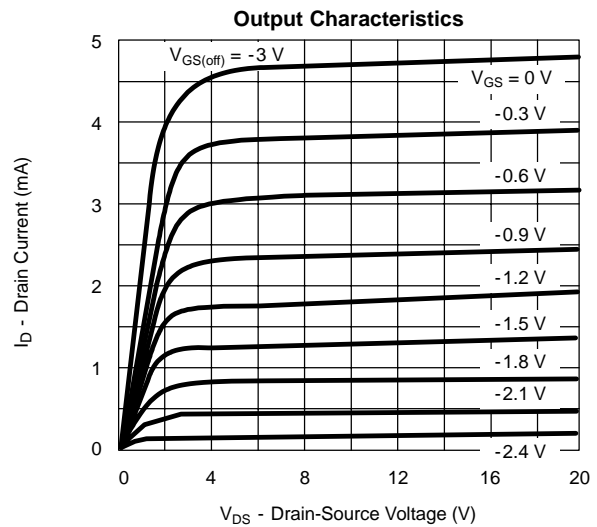
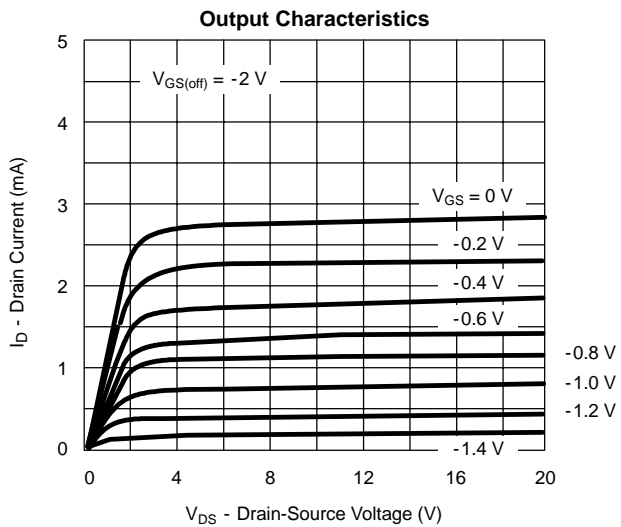
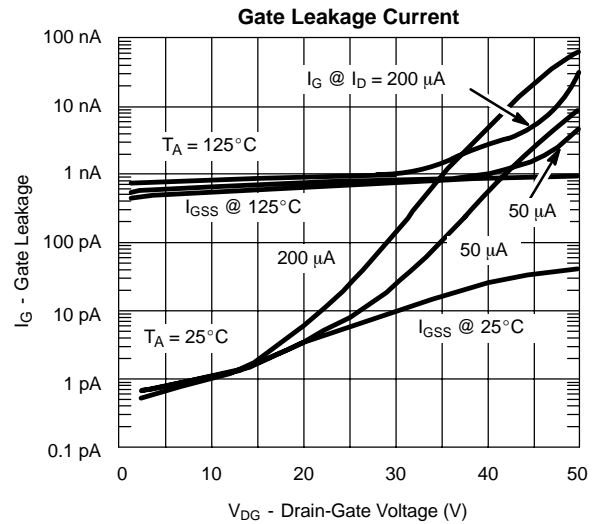
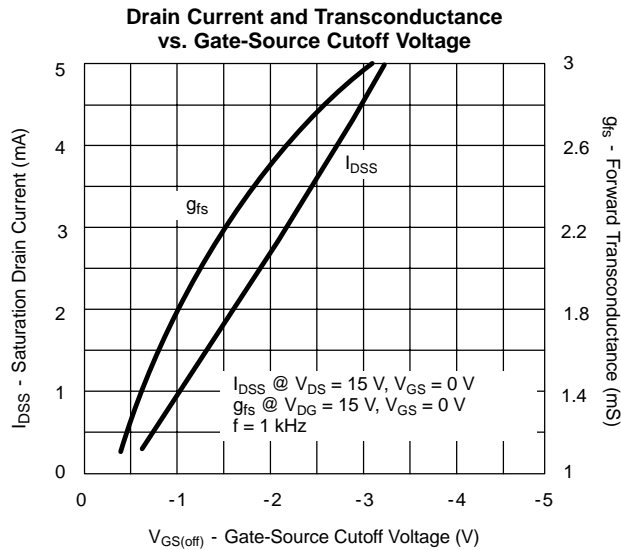
Parameter	Symbol	Test Conditions	Typ ^a	Limits				Unit
				SST/U5198NL		SST/U5199NL		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 20 V, I _D = 1 nA	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -30 V, V _{DS} = 0 V	-10		-25		-25	μA
		T _A = 150 °C	-20		-50		-50	nA
Gate Operating Current	I _G	V _{DG} = 20 V, I _D = 200 μA	-5		-15		-15	μA
		T _A = 125 °C	-0.8		-15		-15	nA
Gate-Source Voltage	V _{GS}	V _{DG} = 20 V, I _D = 200 μA	-1.5	-0.2	-3.8	-0.2	-3.8	V
Dynamic								
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 kHz	3.0	1	4	1	4	mS
Common-Source Output Conductance	g _{os}		8		50		50	μS
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 20 V, I _D = 200 μA f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g _{os}		1		4		4	μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		1		2		2	
Equivalent Input Noise Voltage	e _n	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 kHz	11					nV/ √Hz
Noise Figure	NF	V _{DS} = 20 V, V _{GS} = 0 V f = 100 Hz, R _G = 10 MΩ (U Only)	0.5					dB
Matching								
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 20 V, I _D = 200 μA			10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 20 V, I _D = 200 μA T _A = -55 to 125 °C	SST5198NL	15				μV/°C
			SST5199NL	30				
			U Only			20		
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 20 V, V _{GS} = 0 V	SST Only	0.97				μS
			U Only		0.95	1	0.95	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 20 V, I _D = 200 μA f = 1 kHz	SST Only	0.97				
			U Only		0.95	1	0.95	
Differential Output Conductance	g _{os1} - g _{os2}	V _{DS} = 20 V, I _D = 200 μA f = 1 kHz	SST Only	0.2				
			U Only			1		
Differential Gate Current	I _{G1} - I _{G2}	V _{DG} = 20 V, I _D = 200 μA, T _A = 125 °C	SST Only	0.1				nA
			U Only			5		
Common Mode Rejection Ratio	CMRR	V _{DG} = 10 to 20 V, I _D = 200 μA	97					dB

Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

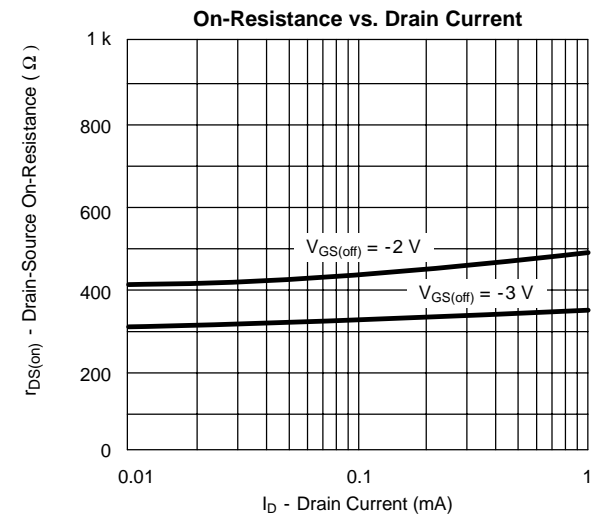
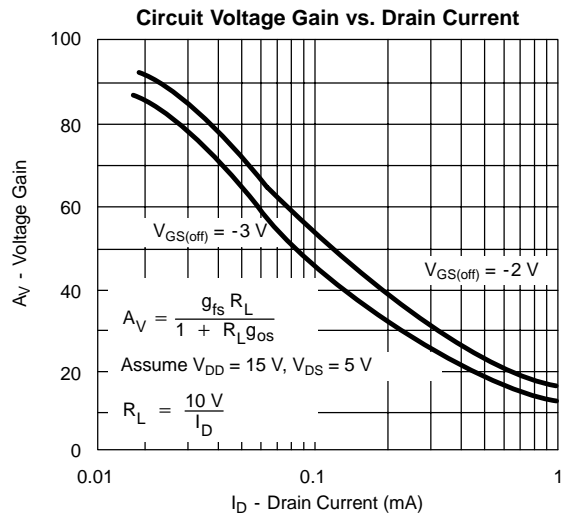
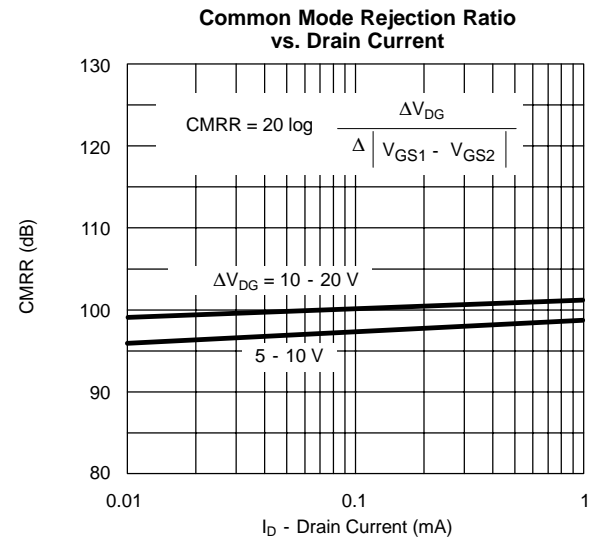
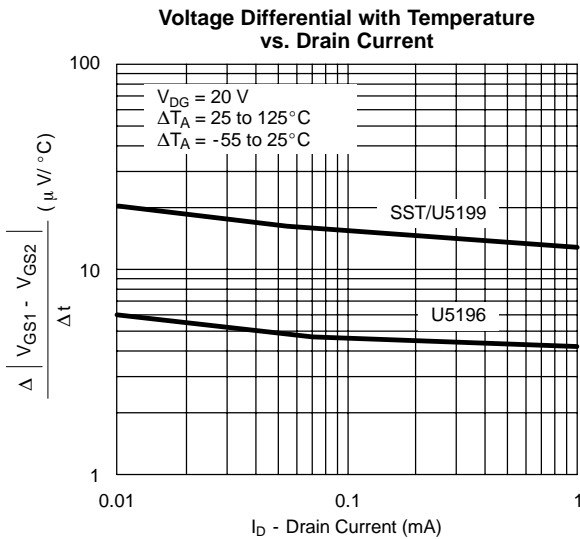
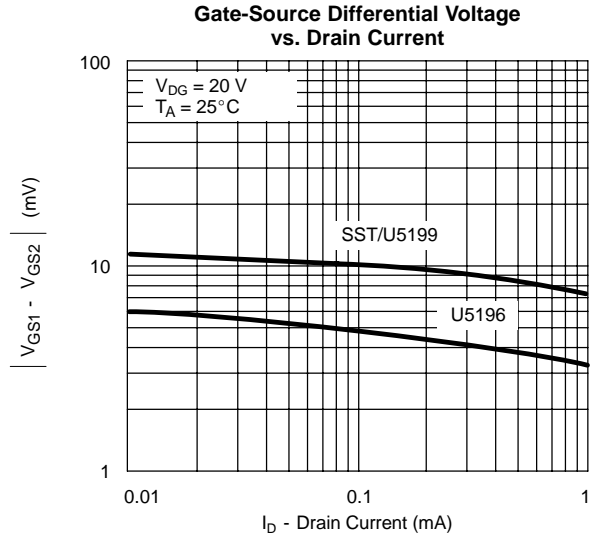
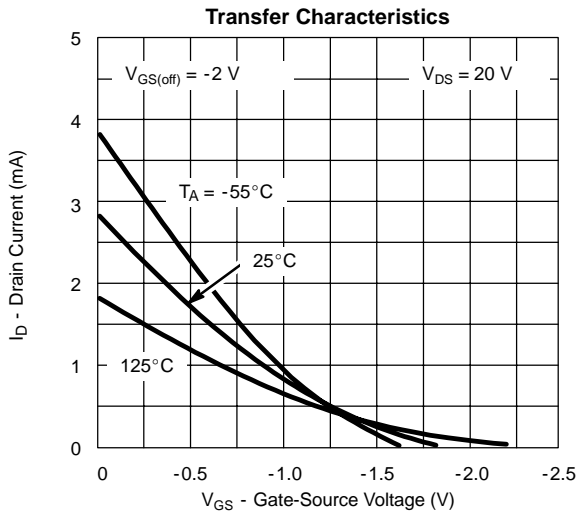
NQP

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)





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