Synchronous DRAM Module 128Mbyte (16Mx64bit), SMM ,16Mx8, 4Banks, 4K Ref. 3.3V **Part No. HSD16M64F8K**

GENERAL DESCRIPTION

The HSD16M64F8K is a 16M x 64 bit Synchronous Dynamic RAM high-density memory module. The module consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 120-pin glass-epoxy. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The HSD16M64F8K is a SMM(Stackable Memory Module type) .Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTL-compatible.

FEATURES

• Part Identification

HSD16M64F8K : 100MHz (CL=2 & CL=3)

• Burst mode operation

• Auto & self refresh capability (4096 Cycles/64ms)

• LVTTL compatible inputs and outputs

• Single 3.3V ±0.3V power supply

• MRS cycle with address key programs

- Latency (Access from column address)
- Burst length (1, 2, 4, 8 & Full page)
- Data scramble (Sequential & Interleave)

• All inputs are sampled at the positive going edge of the system clock

• The used device is 4M x 8bit x 4Banks SDRAM

PIN ASSIGNMENT

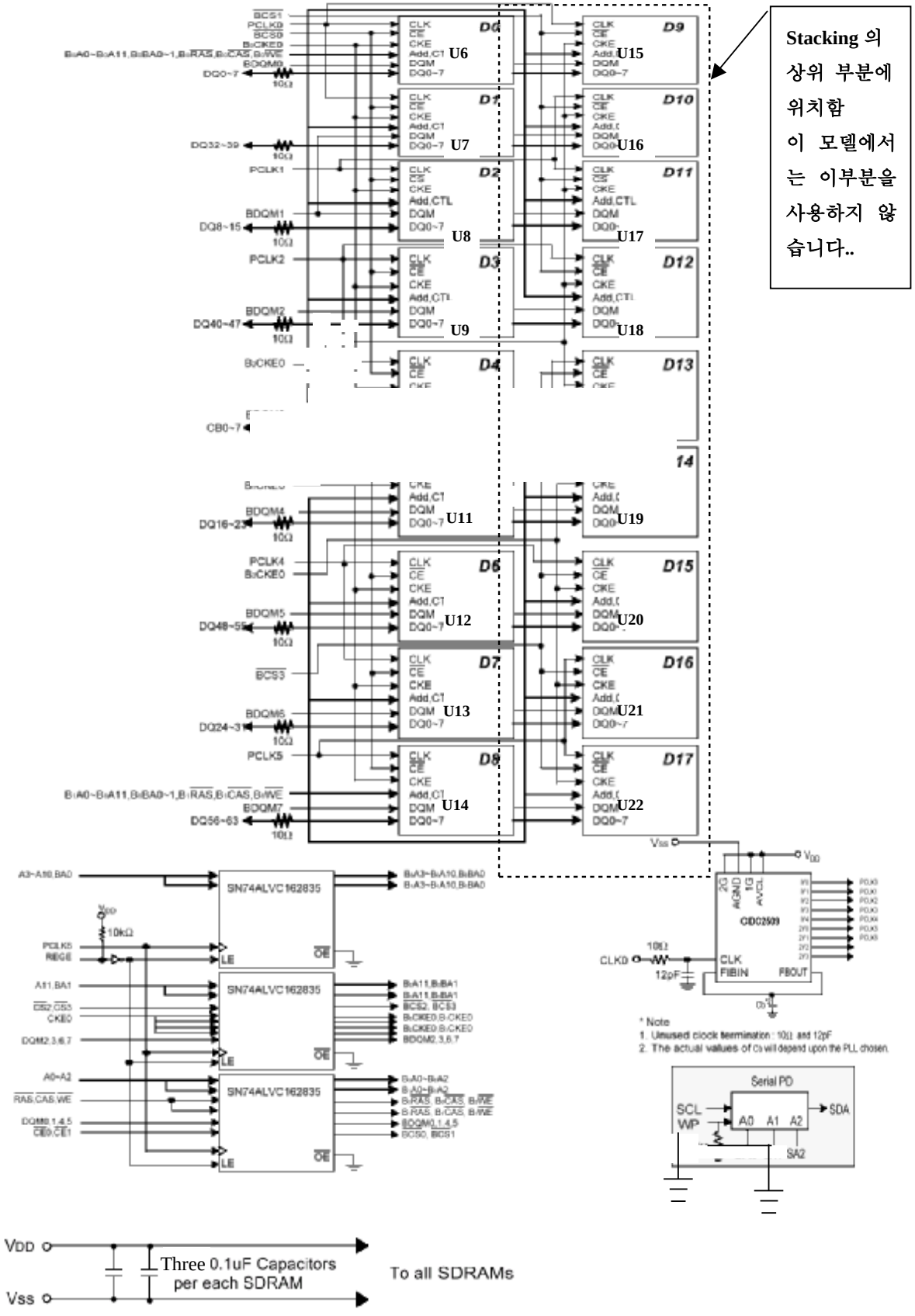
P1						P2					
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	29	NC	57	/RAS	1	Vss	29	A3	57	A6
2	DQ32	30	Vcc	58	/CS0	2	DQ16	30	Vss	58	A5
3	DQ33	31	Vss	59	NC	3	DQ17	31	Vcc	59	A4
4	DQ34	32	DQ0	60	Vss	4	DQ18	32	DQ48	60	Vcc
5	DQ35	33	DQ1			5	DQ19	33	DQ49		
6	DQ36	34	DQ2			6	DQ20	34	DQ50		
7	DQ37	35	DQ3			7	DQ21	35	DQ51		
8	DQ38	36	DQ4			8	DQ22	36	DQ52		
9	DQ39	37	DQ5			9	DQ23	37	DQ53		
10	Vcc	38	DQ6			10	Vss	38	DQ54		
11	DQ40	39	DQ7			11	DQ24	39	DQ55		
12	DQ41	40	Vss			12	DQ25	40	Vcc		
13	DQ42	41	DQ8			13	DQ26	41	DQ56		
14	DQ43	42	DQ9			14	DQ27	42	DQ57		
15	DQ44	43	DQ10			15	DQ28	43	DQ58		
16	DQ45	44	DQ11			16	DQ29	44	DQ59		
17	DQ46	45	DQ12			17	DQ30	45	DQ60		
18	DQ47	46	DQ13			18	DQ31	46	DQ61		
19	Vcc	47	DQ14			19	Vss	47	DQ62		
20	DQM4	48	DQ15			20	DQM2	48	DQ63		
21	DQM5	49	Vss			21	DQM3	49	Vcc		
22	REGE	50	DQM0			22	NC	50	DQM6		
23	CKE0	51	DQM1			23	BA0	51	DQM7		
24	NC	52	/WE			24	BA1	52	A12		
25	Vcc	53	CLK0			25	A10	53	A11		
26	SDA	54	CLK1			26	A0	54	A9		
27	SCL	55	Vss			27	A1	55	A8		
28	/CS2	56	/CAS			28	A2	56	A7		

*** Pin Names**

A0~A11: Address input (Multiplexed)
DQ0~DQ63: Data input/output
CKE0: Clock enable input
/RAS: Row address strobe
/CAS: Coulmn address strobe
DQM0~7: DQM
REGE: Register enable
SDA: Serial data I/O
NC: No connection

BA0~BA1: Select bank
CLK0: Clock input
/CS0, /CS2: Chip select input
/WE: Write enable
V_{SS}: Ground
Vcc: Power supply(3.3V)
SCL: Serial clock
DU: Don't use

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
/CE	Chip enable	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tsHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. The inputs are strobed in the latch/flip-flop on the riging edge of CLK. REGE is tied to V_{DD} through 10K ohm register on PCB. So if REGE of module is floating, this module will be operated as registerd mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
Vcc/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 4.6V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 4.6V
Power Dissipation	P_D	8W
Storage Temperature	T_{STG}	-55°C to 150°C
Short Circuit Output Current	I_{OS}	50mA

Notes:
Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C))

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Supply Voltage	Vcc	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	Vcc+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes :
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(Vcc = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input capacitance(A0~A11)	C_{IN1}	2.5	5.0	pF
Input capacitance(/RAS, /CAS,/WE)	C_{IN2}	2.5	5.0	pF
Input capacitance(CKE0)	C_{IN3}	2.5	5.0	pF
Input capacitance(CLK0)	C_{IN4}	2.5	4.0	pF
Input capacitance(/CE0,CE3)	C_{IN5}	2.5	5.0	pF
Input capacitance(DQM0~DQM7)	C_{IN3}	2.5	5.0	pF
Input capacitance(BA0~BA1)	C_{IN3}	2.5	5.0	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	4.0	6.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	VERSION					UNIT	NOTE
			-13	-12	-1H	-1L	-10		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0mA	960	960	880	880	880	mA	1
Precharge standby current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max) t_{CC}=10ns	8					mA	3
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max) t_{CC}=∞	8					mA	3
Precharge standby current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min) /CE ≥ V_{IH}(min), tcc=10ns Input signals are changed one time during 20ns	160					mA	3
	$I_{CC2}NS$	CKE ≥ V_{IH}(min) CLK ≤ V_{IL}(max), tcc=∞ Input signals are stable	56						
Active standby current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), tcc=10ns	40					mA	3
	$I_{CC3}PS$	CKE&CLK ≤ V_{IL}(max) tcc=∞	40						
Active standby current in non power-down mode (One bank active)	$I_{CC3}N$	CKE≥V_{IH}(min), /CE≥V_{IH}(min), tcc=10ns Input signals are changed one time during 20ns	240					mA	3
	$I_{CC3}NS$	CKE≥VIH(min) CLK ≤VIL(max), tcc=∞ Input signals are stable	160						
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	1.2	1.16	1	1	1	A	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1.76	1.76	1.68	1.68	1.68	A	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	12					mA	3

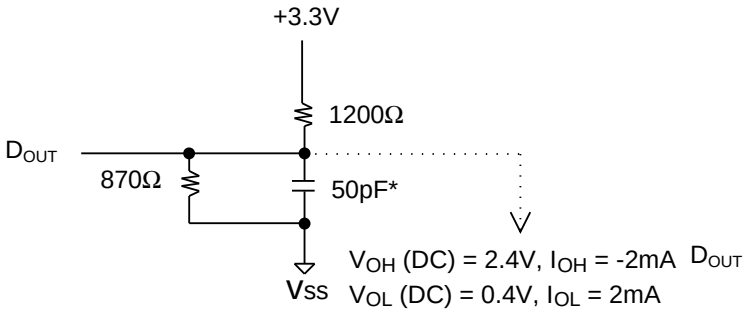
Notes:

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1PLL & 3 Drive Ics.
4. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

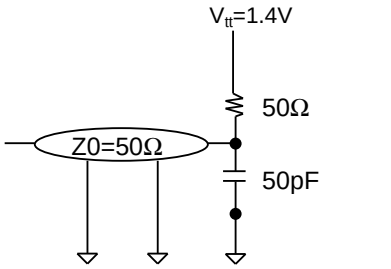
AC OPERATING TEST CONDITIONS

(Vcc = 3.3V ± 0.3V, T_A = 0 to 70°C)

PARAMETER	Value	UNIT
AC Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER	SYMBOL	VERSION					UNIT	NOTE
		-13	-12	-1H	-1L	-10		
Row active to row active delay	t_{RRD}(min)	15	16	20	20	20	ns	1
/RAS to /CAS delay	t_{RCD}(min)	20	20	20	20	24	ns	1
Row precharge time	t_{RP}(min)	20	20	20	20	24	ns	1
Row active time	t_{RAS}(min)	45	48	50	50	50	ns	1
	t_{RAS}(max)	100					ns	
Row cycle time	t_{RC}(min)	65	68	70	70	80	ns	1
Last data in to row precharge	t_{RDL}(min)	2					CLK	2,5
Last data in to Active delay	t_{DAL}(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay	t_{CDL}(min)	1					CLK	2
Last data in to burst stop	t_{BDL}(min)	1					CLK	2
Col. address to col. address delay	t_{CCD}(min)	1					CLK	3
Number of valid output data	CAS latency=3	2					ea	4
	CAS latency=2	1						

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
.5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
(recommend : tRDL=2CLK and tDAL=2CLK + 20ns.)

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-13		-12		-1H		-1L		-10		UNIT	NOTE
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	t_{SAC}		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	t_{OH}	2.7		3		3		3		3		ns	2
	CAS latency=2						3		3		3			
CLK high pulse width		t_{CH}	2.5		3		3		3		3.5		ns	3
CLK low pulse width		t_{CL}	2.5		3		3		3		3.5		ns	3
Input setup time		t_{SS}	1.5		2		2		2		2.5		ns	3
Input hold time		t_{SH}	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7	ns	

Notes :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

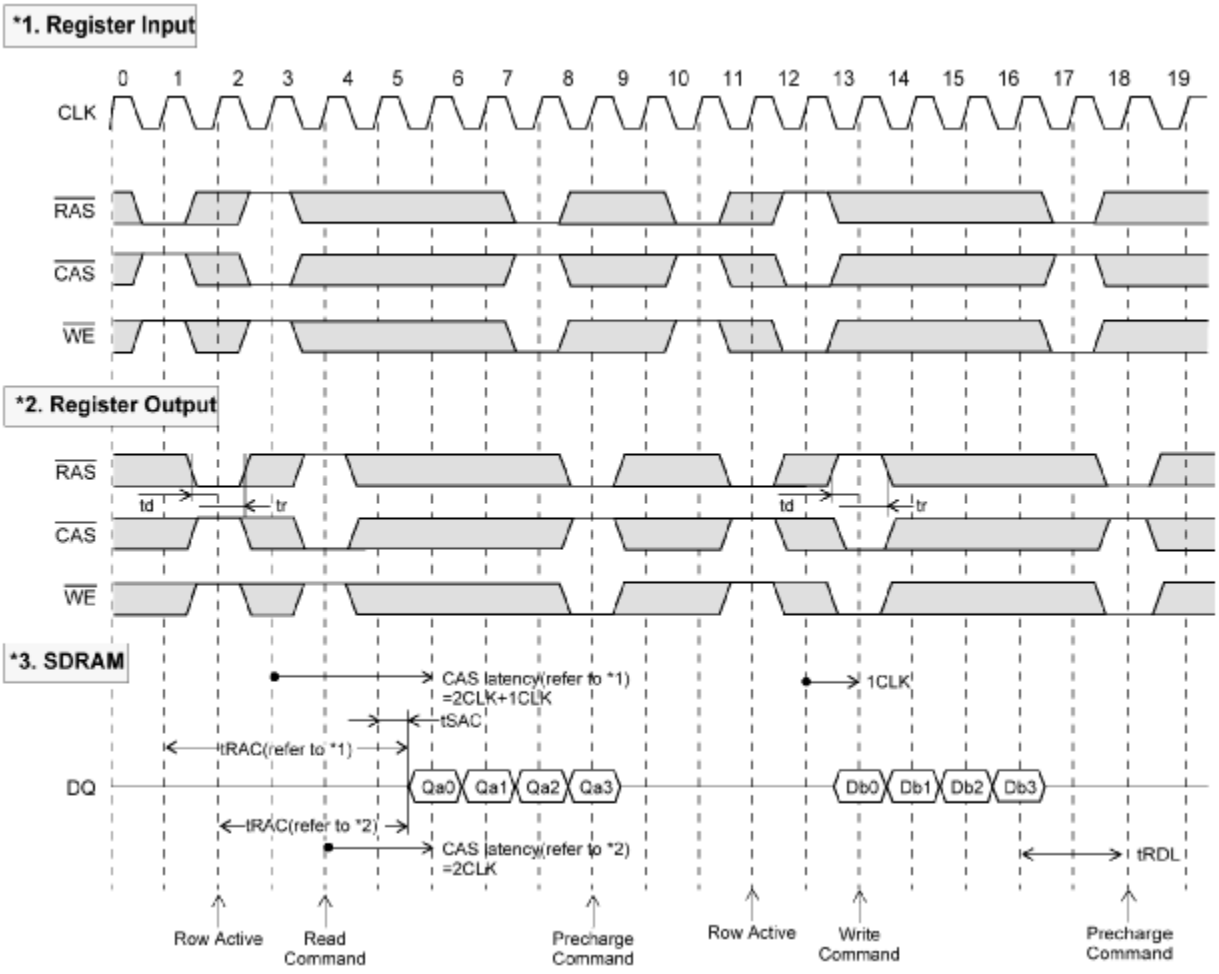
COMMAND			CKE n-1	CKE n	/CE	/RAS	/CAS	/WE	DQM	BA 0,1	A10/AP	A11 A9~A0	NOTE
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge eable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :

1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

TIMING DIAGRAMS

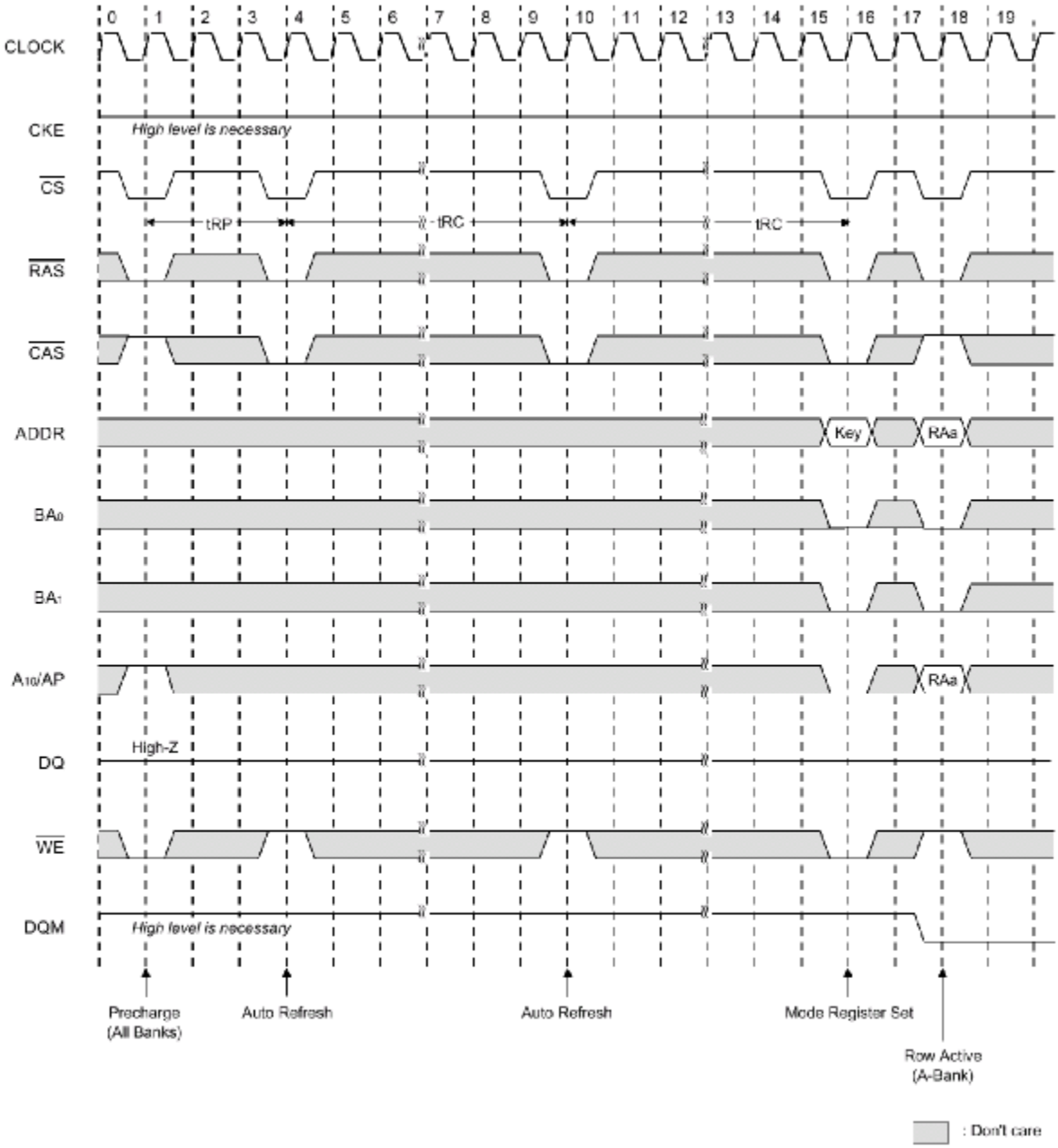


td, tr = Delay of register (74LVC162835)

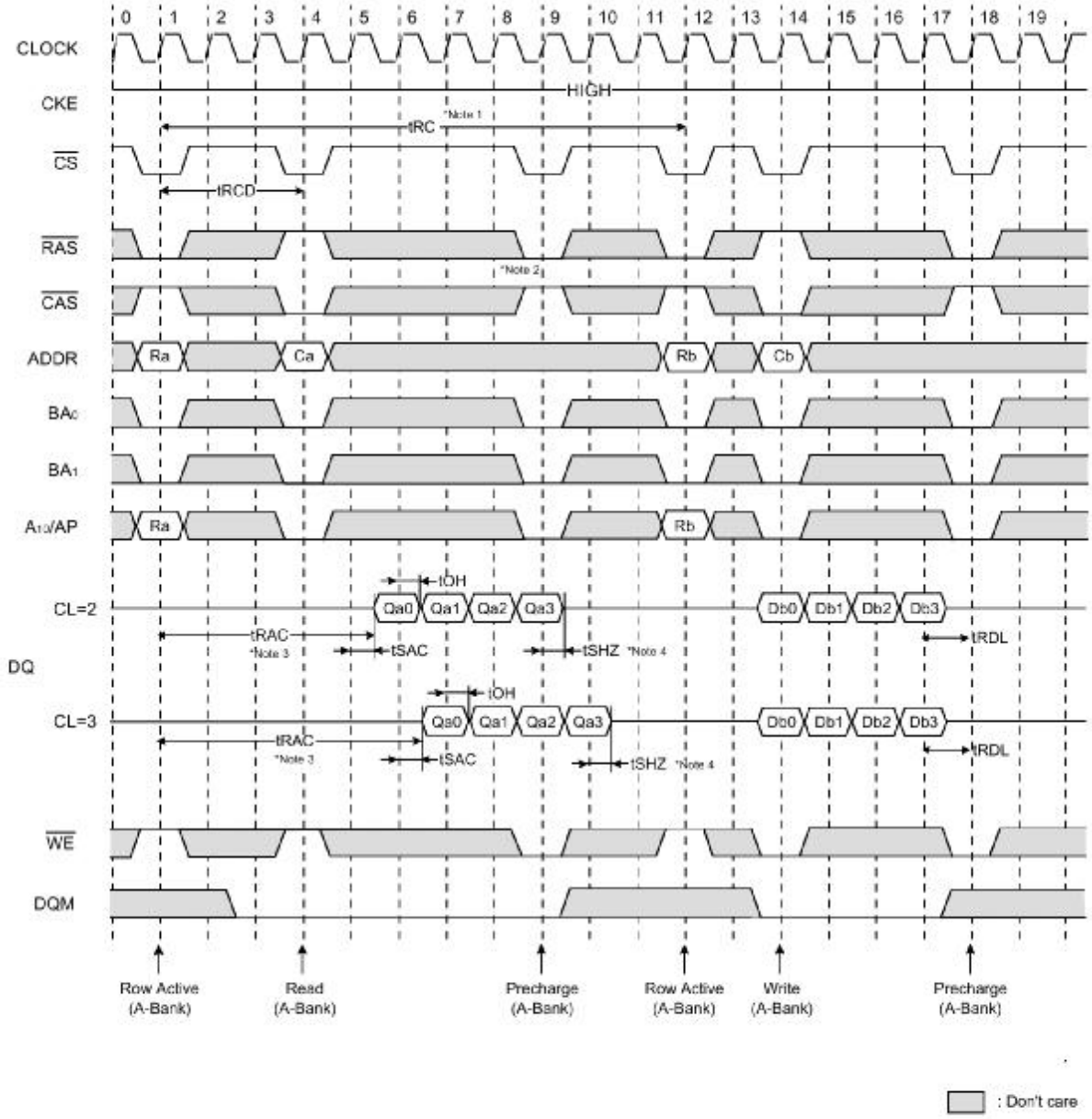
Notes : 1. In case of module timing, command cycles 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74LVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered MODULE.

2. D_{IN} is to be issued 1 clock after write command in external timing because D_{IN} is issued directly to module.

Power Up Sequence



Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK



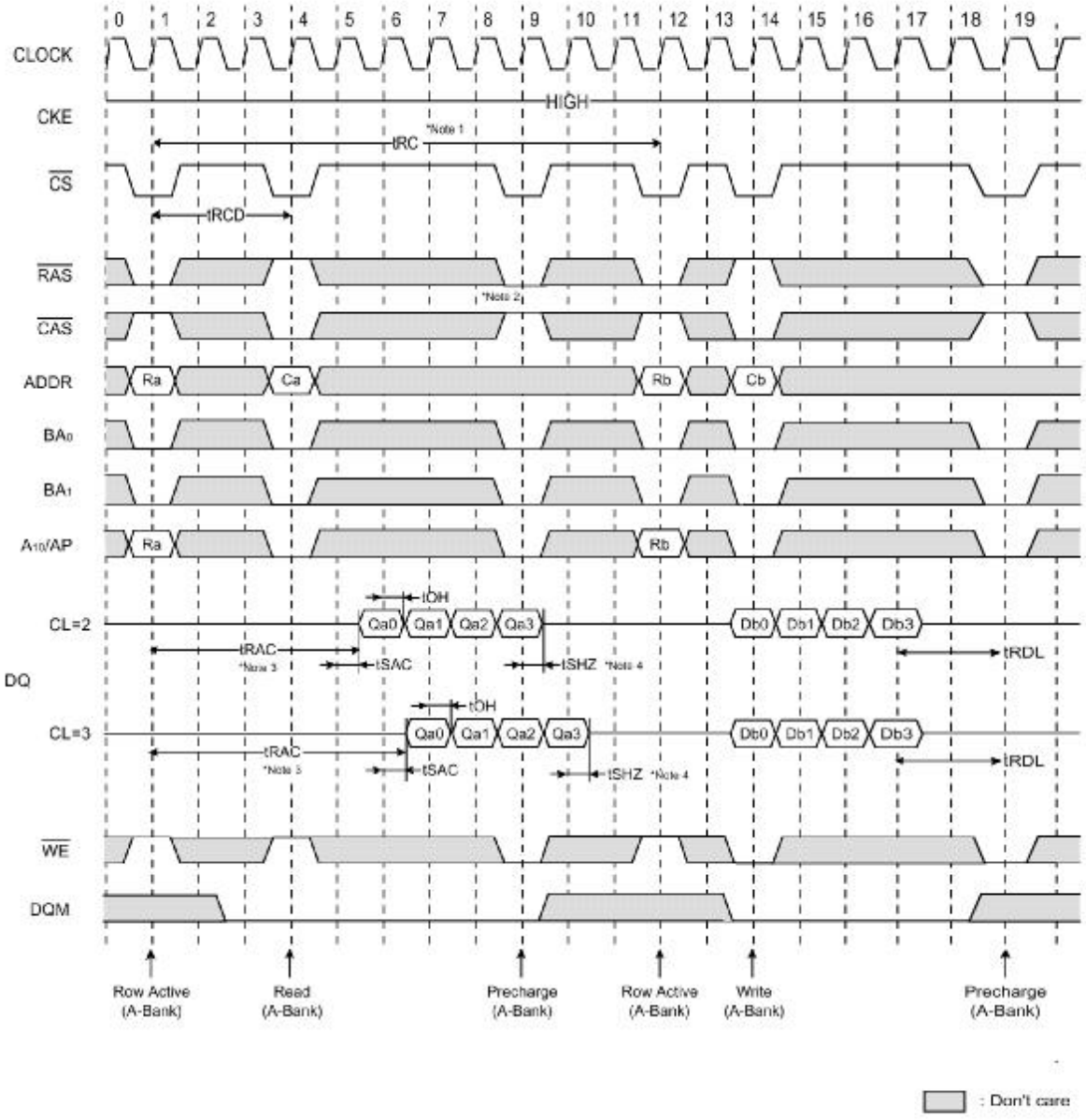
***Note :** 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(tSHZ) after the clock.

3. Access time from Row active command. tCC *(tRCD + CAS latency - 1) + tSAC

4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



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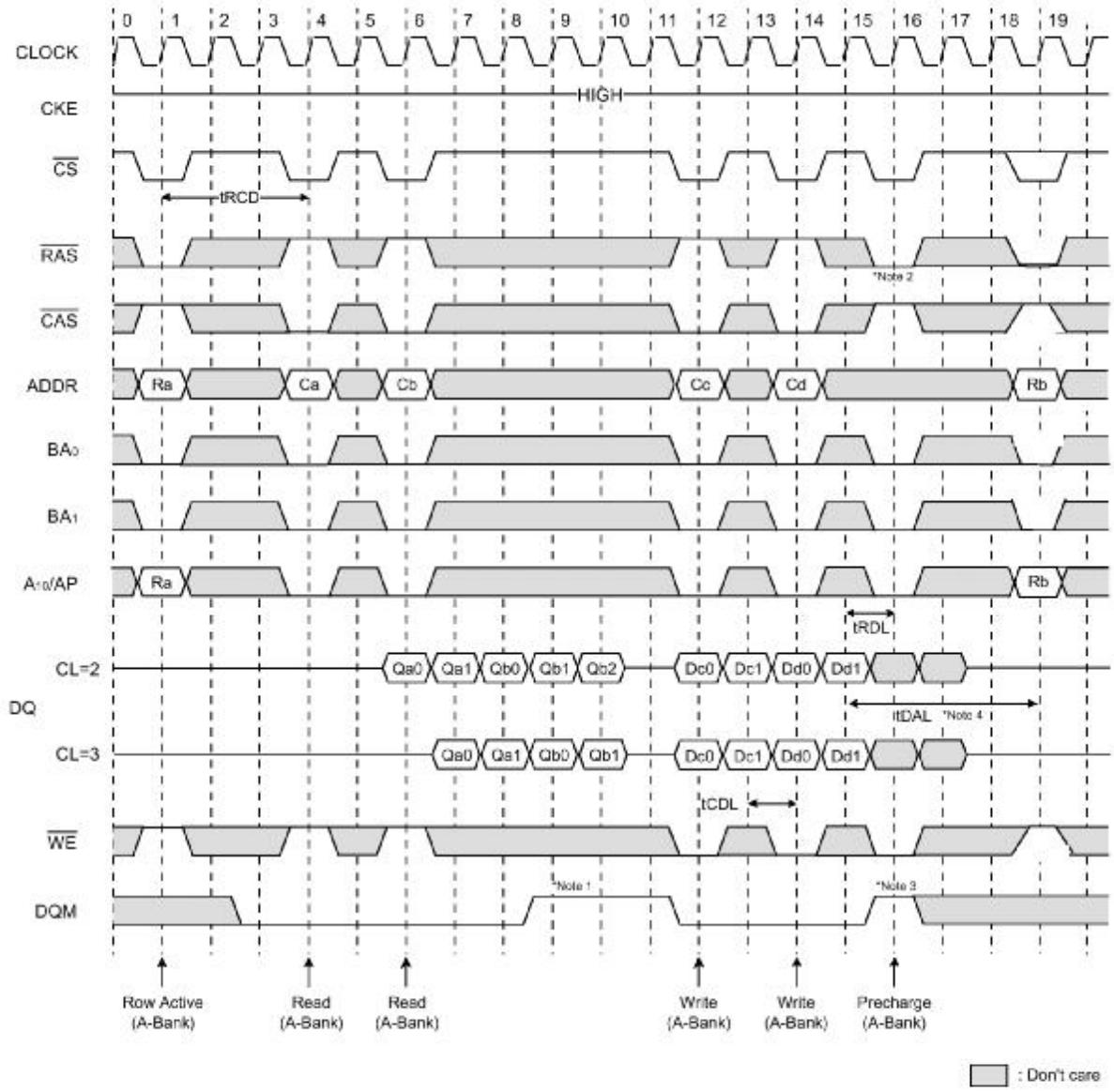
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(tSHZ) after the clock.

3. Access time from Row active command. tcc *(tRCD + CAS latency - 1) + tSAC

4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

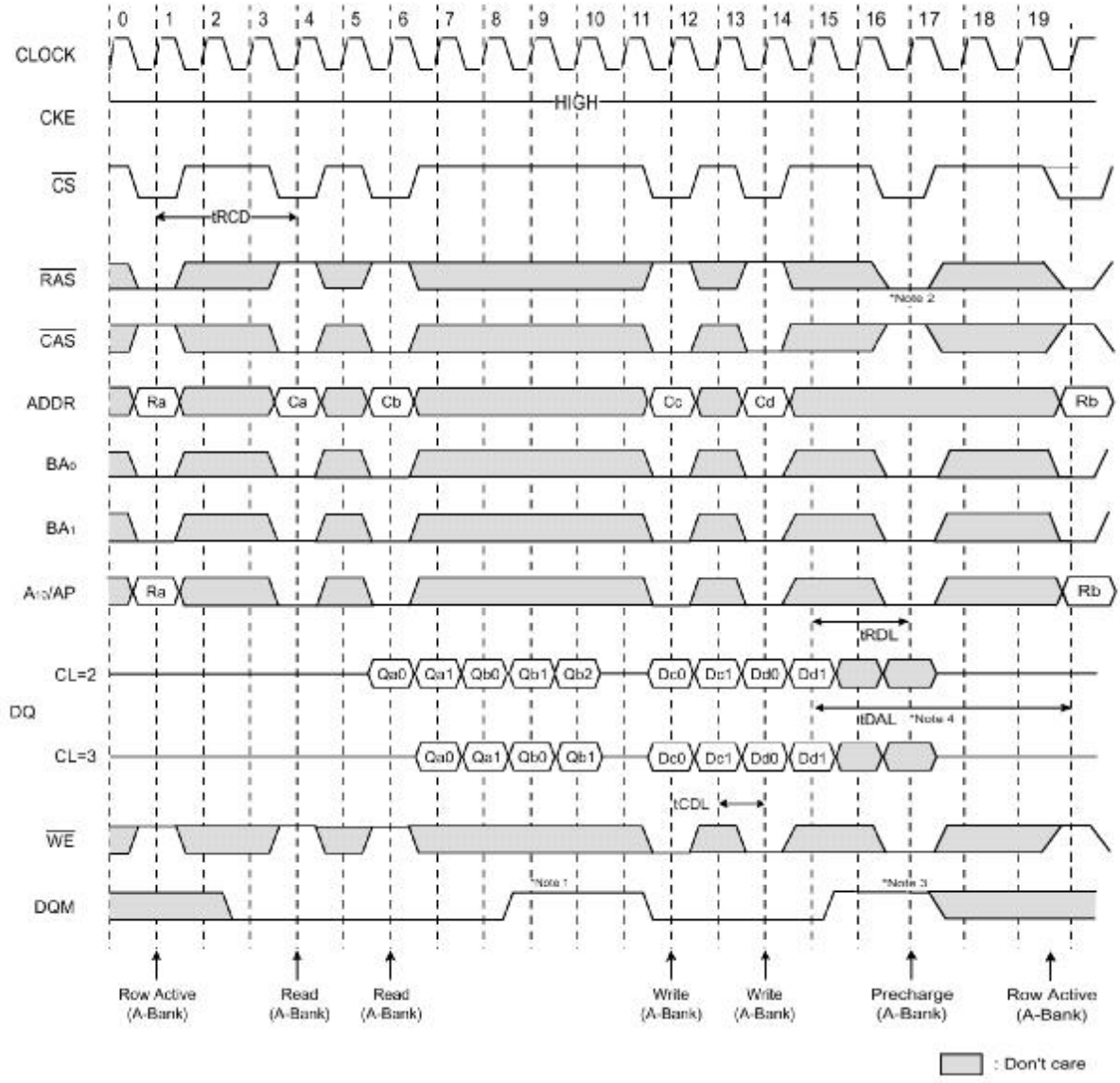
Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK



***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL, last data in to active delay, is 1CLK + 20ns

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK



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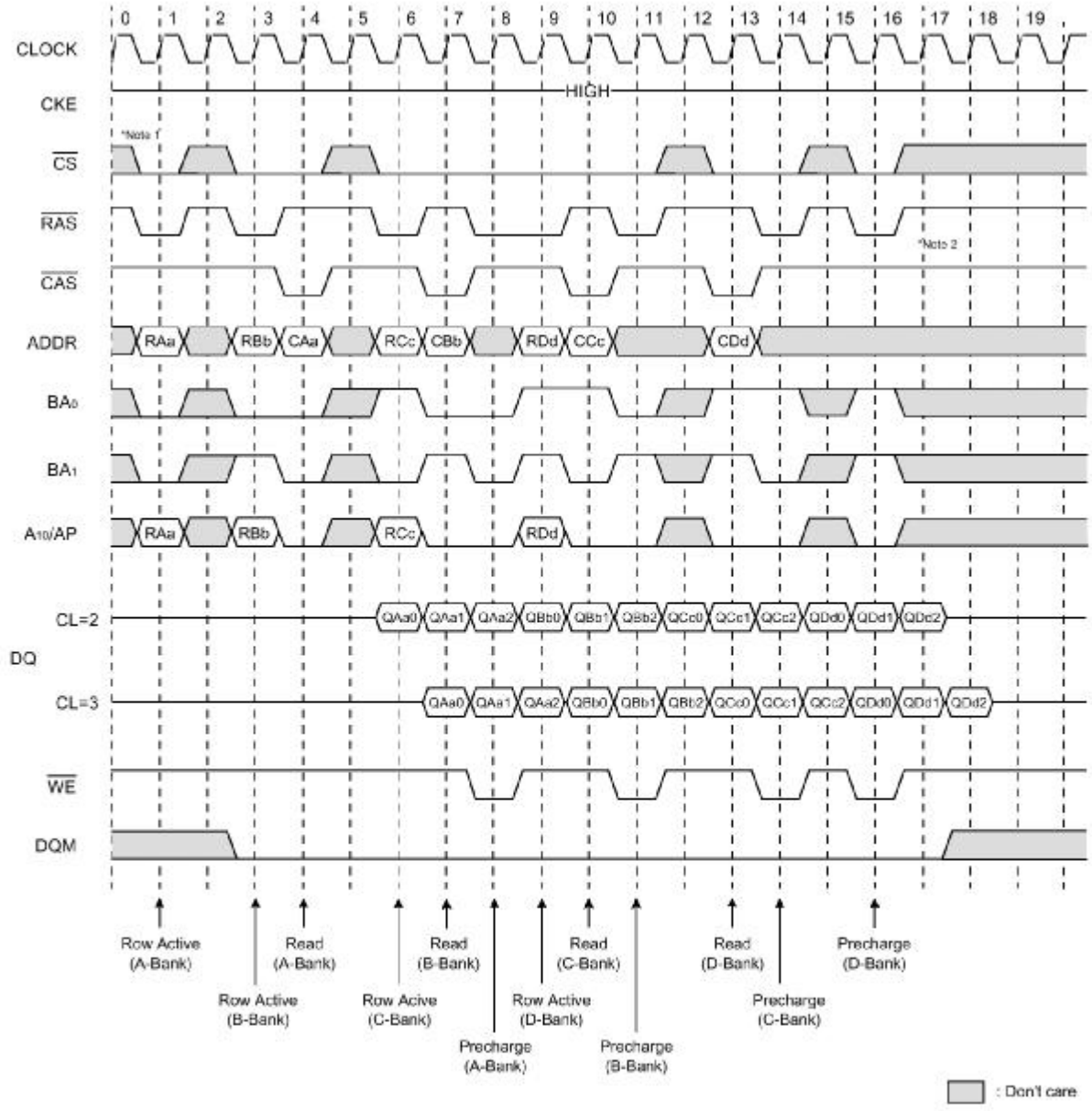
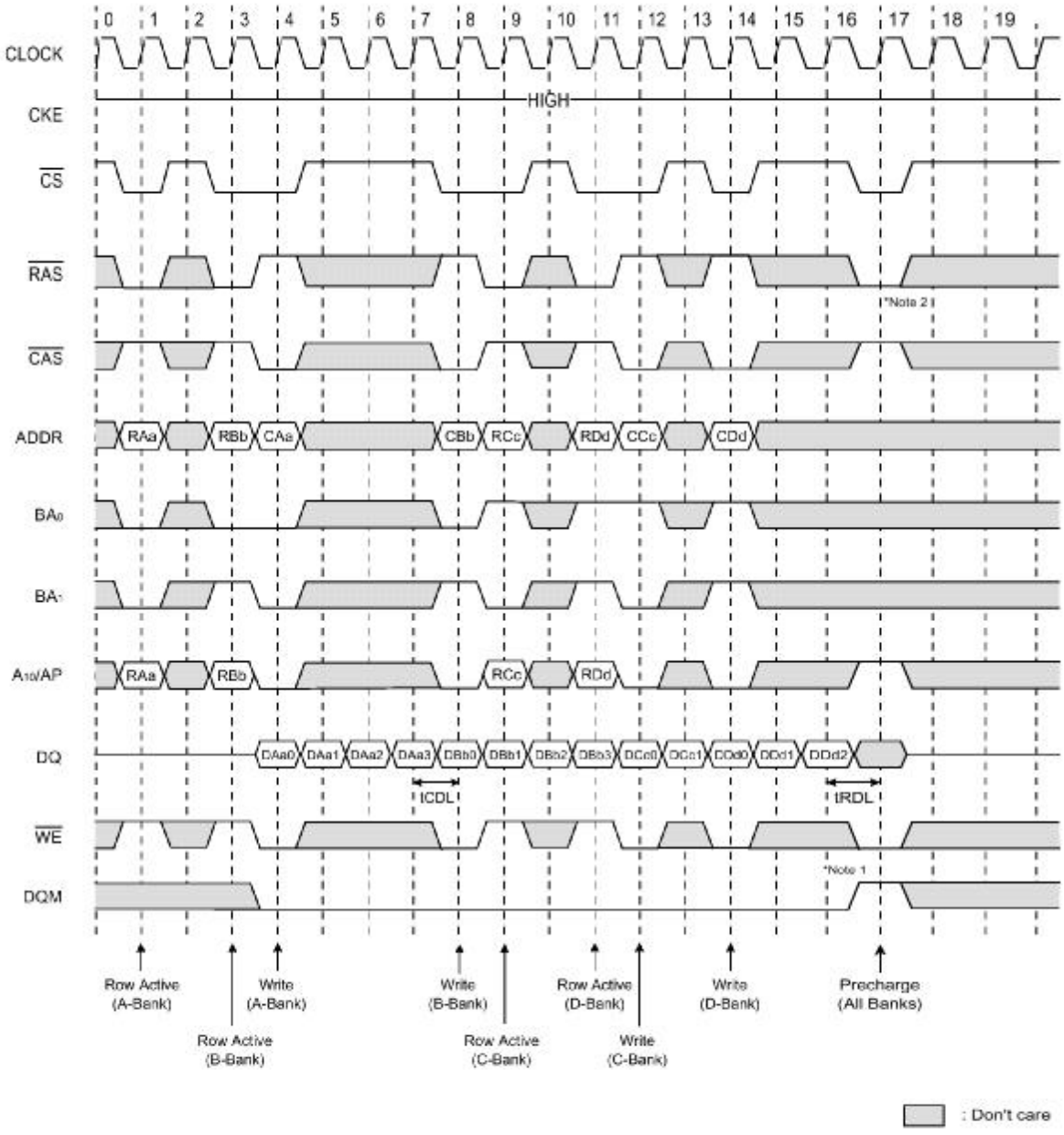
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. tDAL ,last data in to active delay, is 2CLK + 20ns

Page Read Cycle at Different Bank @Burst Length=4



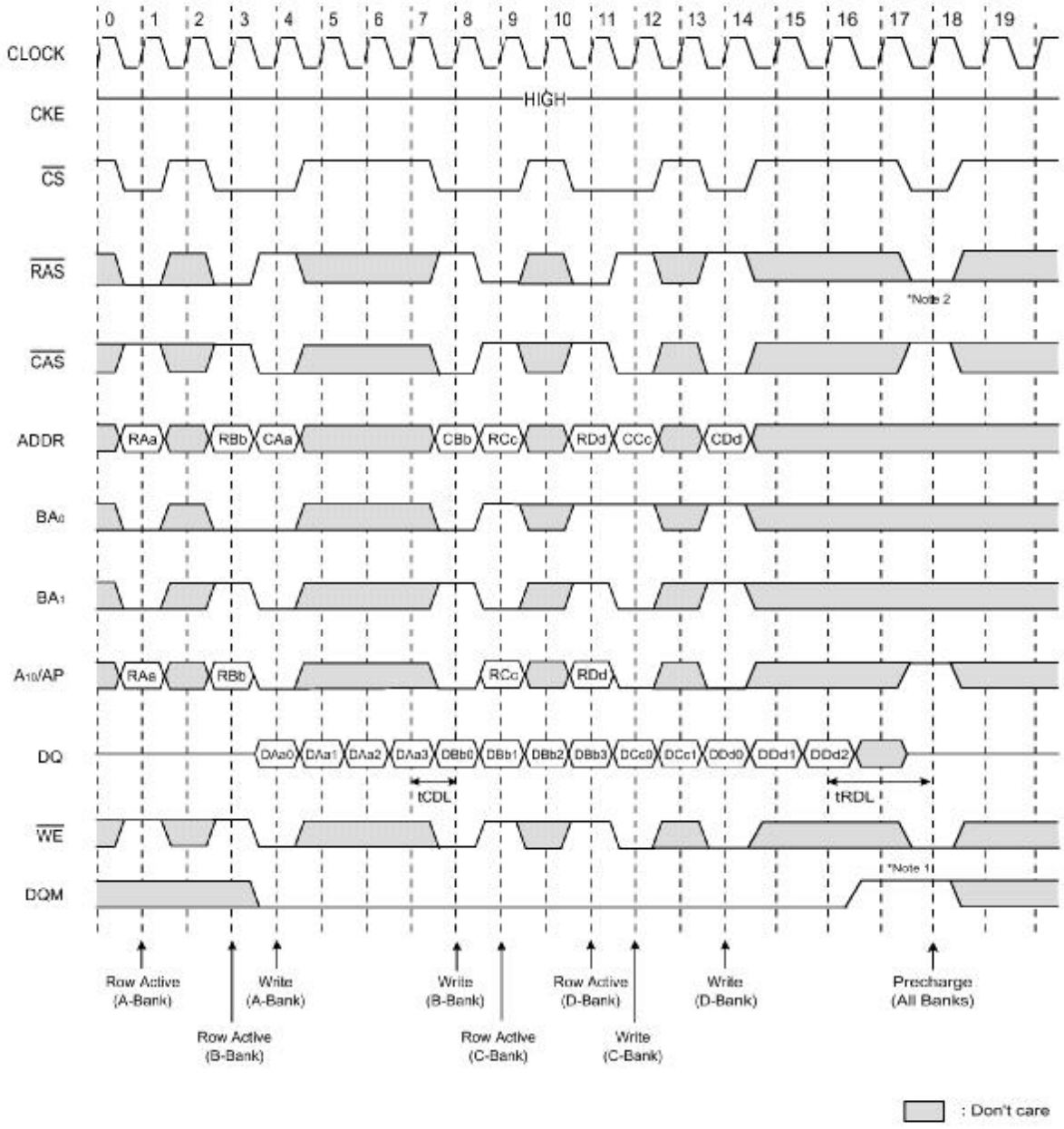
***Note :** 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK



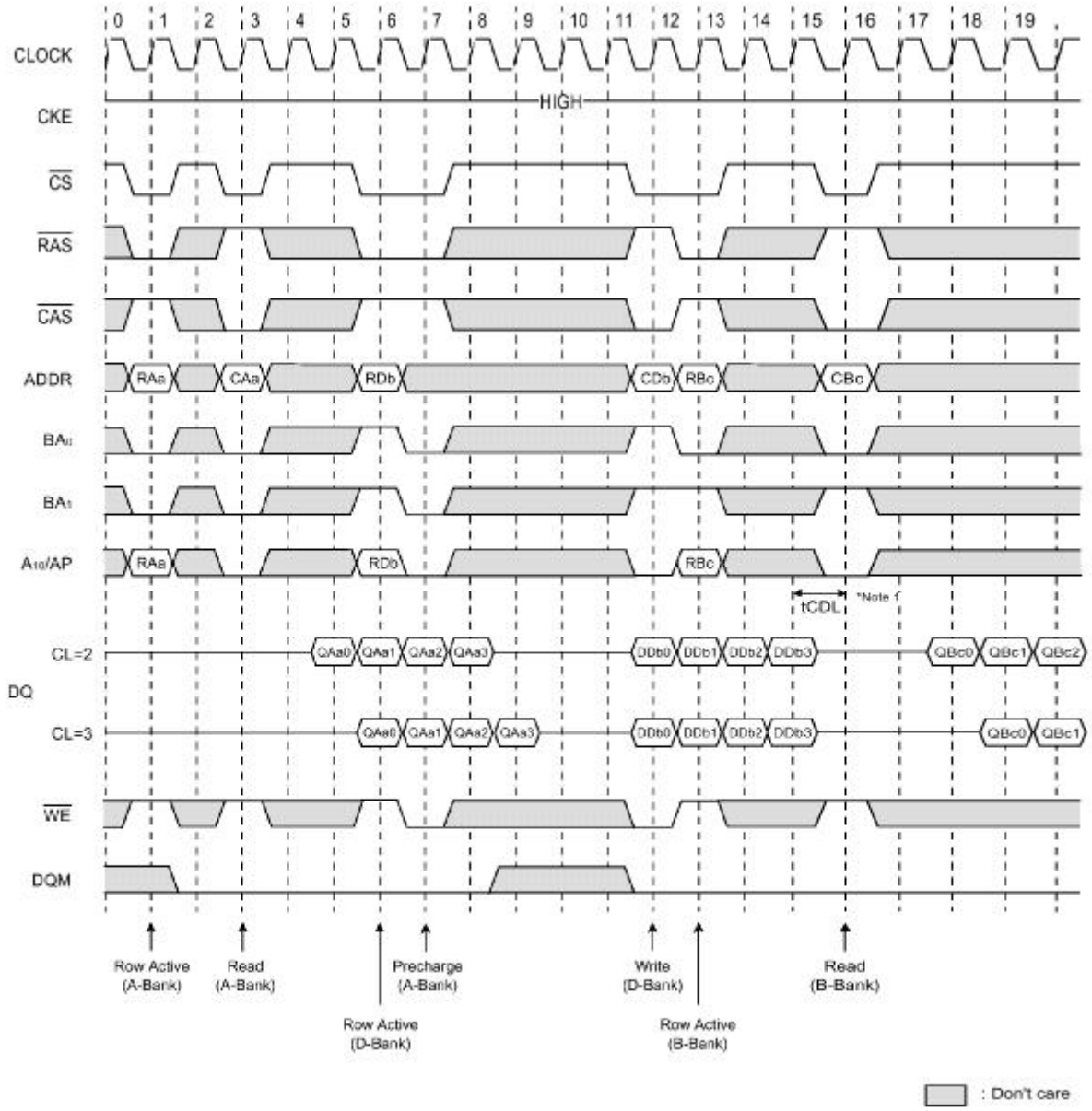
***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK



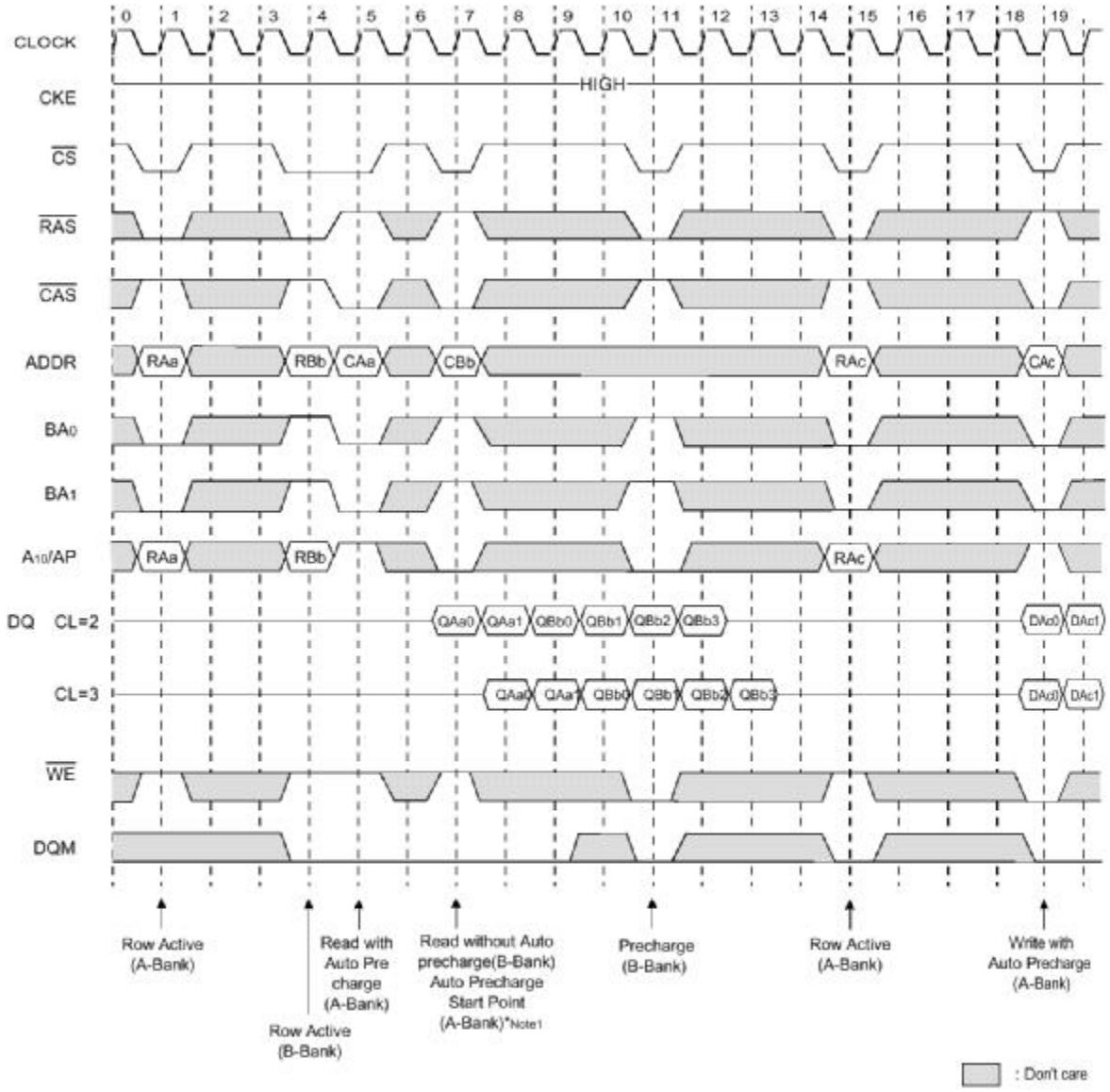
***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



***Note :** 1. tCDL should be met to complete write.

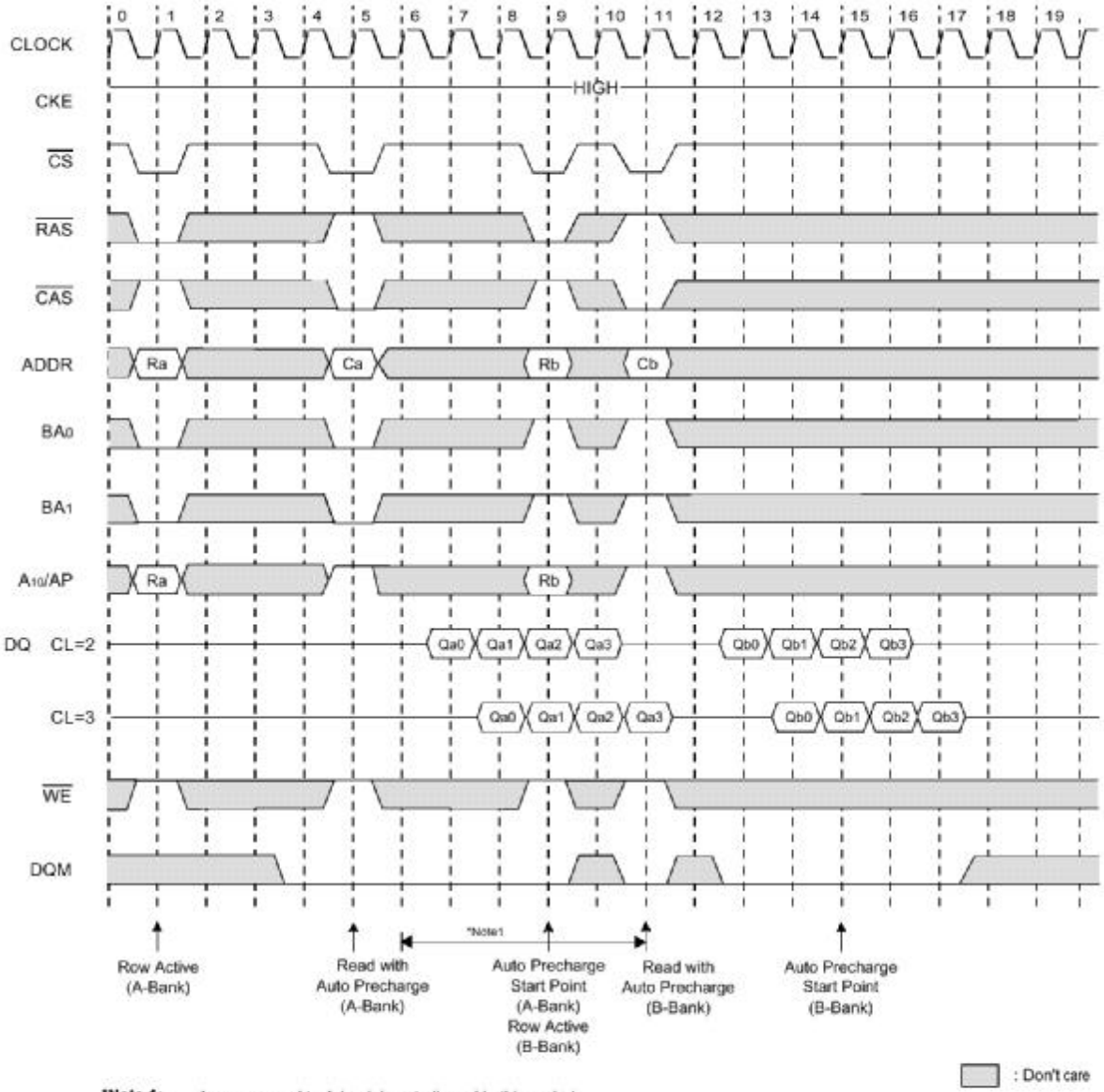
Read & Write Cycle with Auto Precharge I @Burst Length=4



***Note1:** When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.

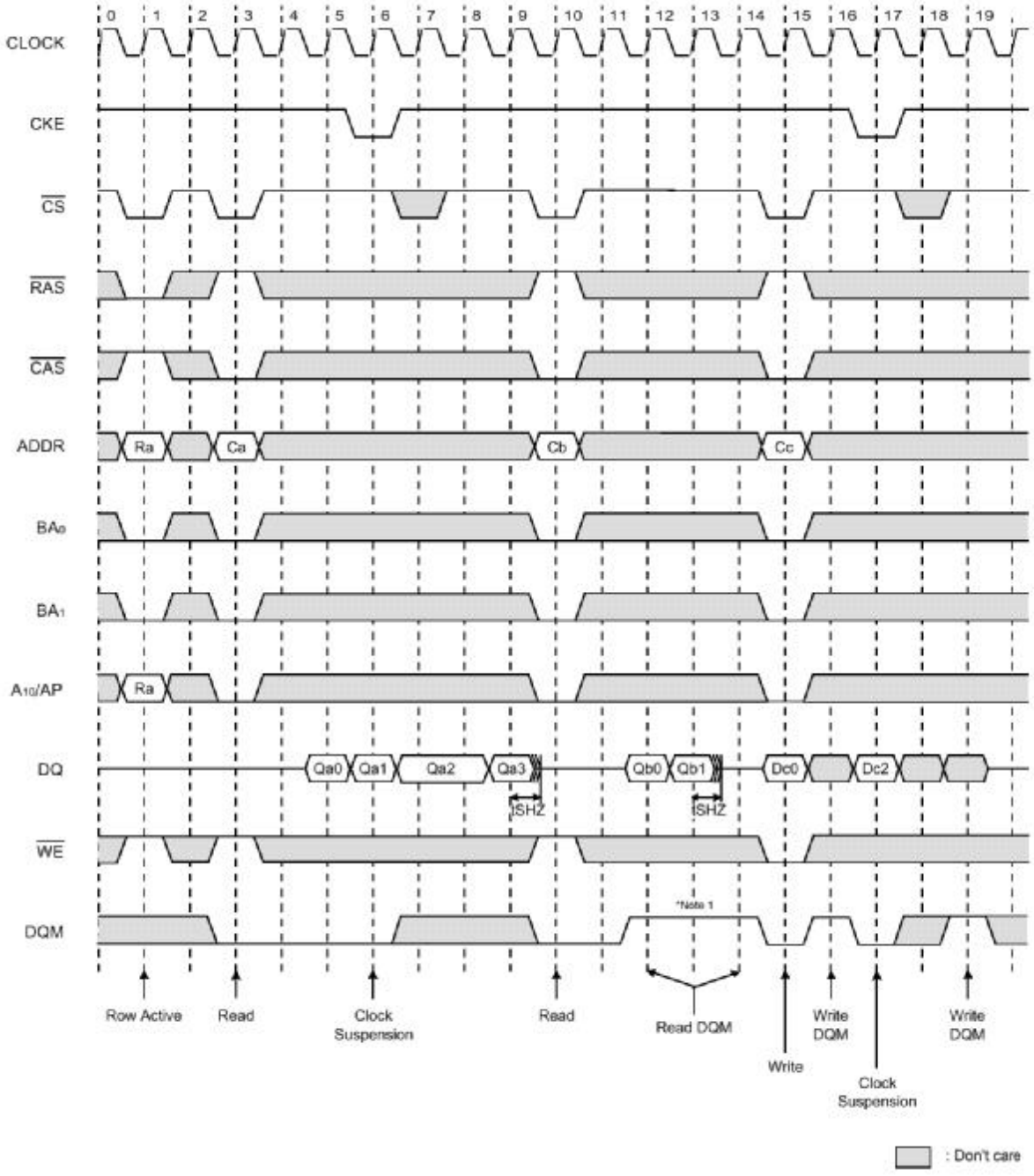
- if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point .
- any command can not be issued at A-Bank during tRP after A-Bank auto precharge starts.

Read & Write Cycle with Auto Precharge II @Burst Length=4



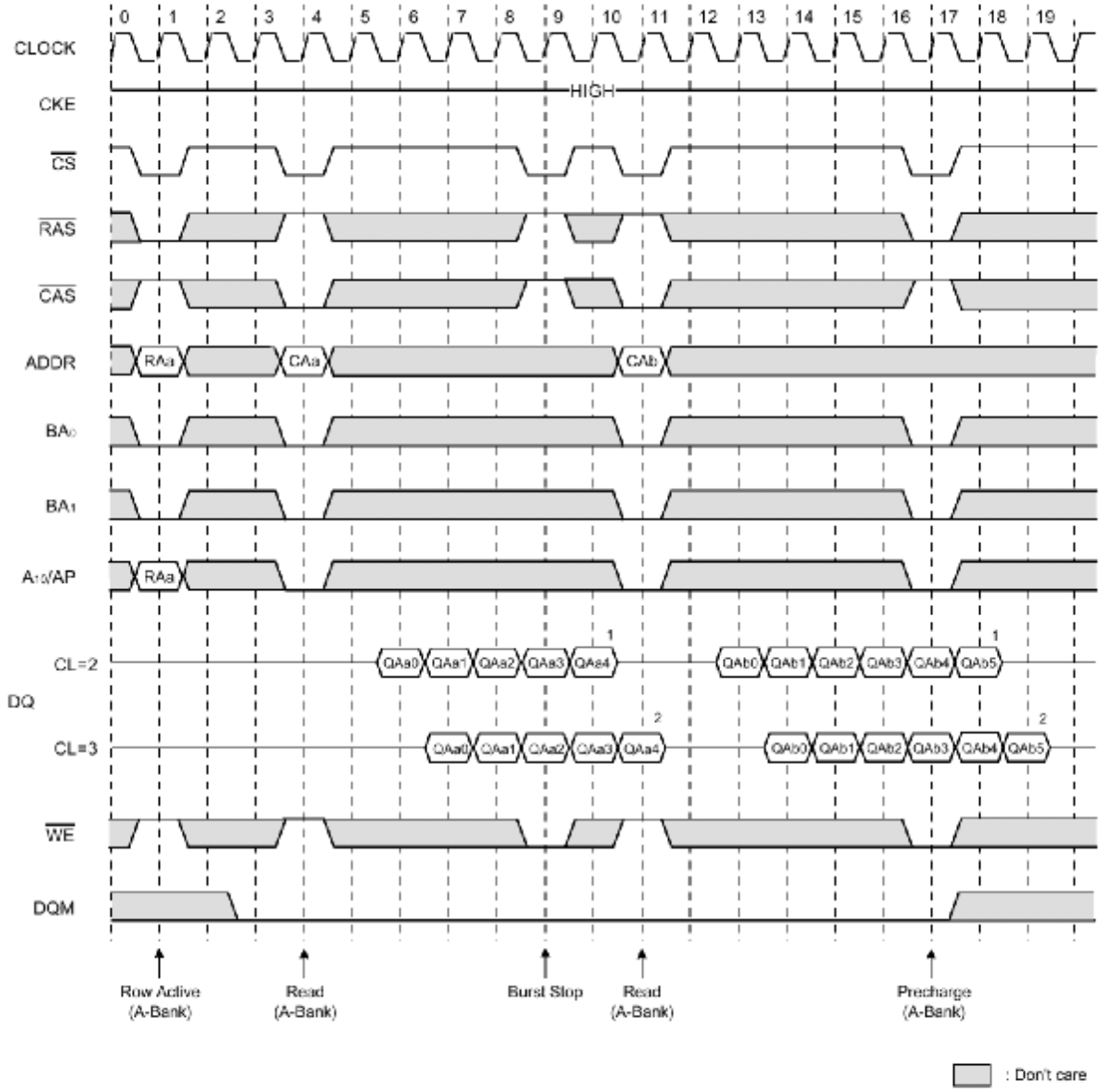
***Note 1:** Any command to A-bank is not allowed in this period.
tRP is determined from at auto precharge start point

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



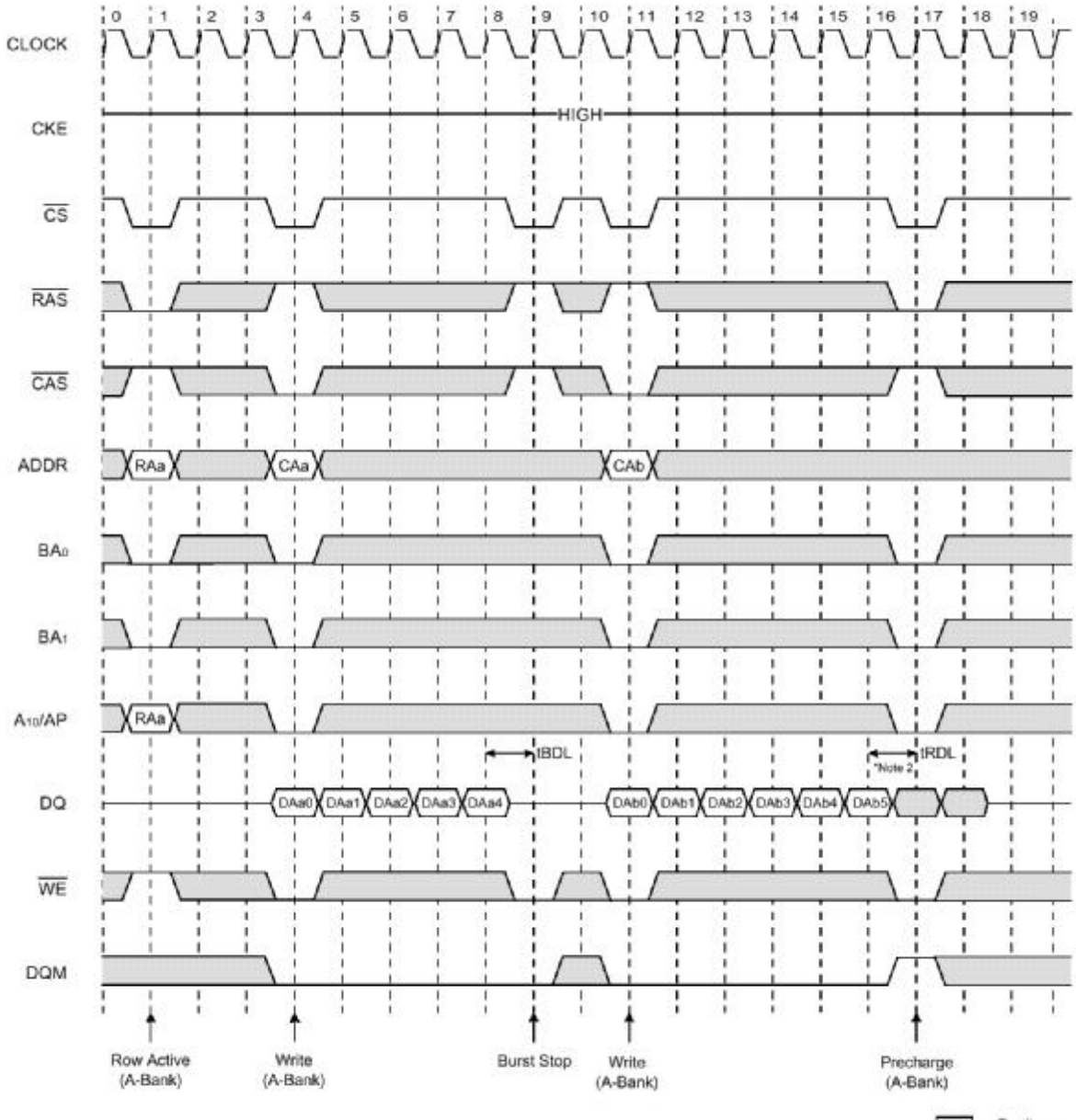
***Note1** : DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst



*Note : 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
Both cases are illustrated above timing diagram. See the label 1, 2 on them.
But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK



***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

3. Burst stop is valid at every burst length.

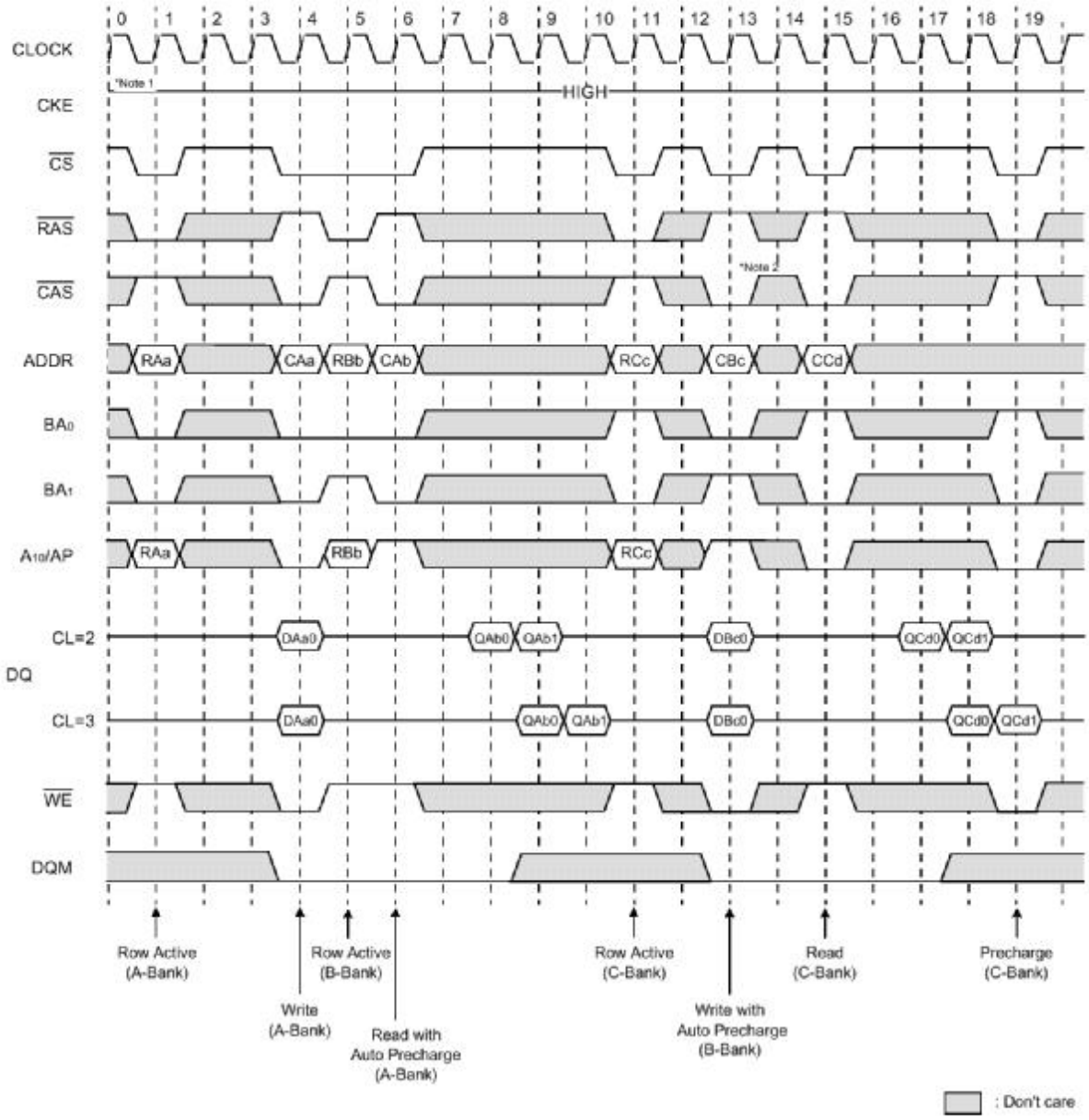
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK

***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

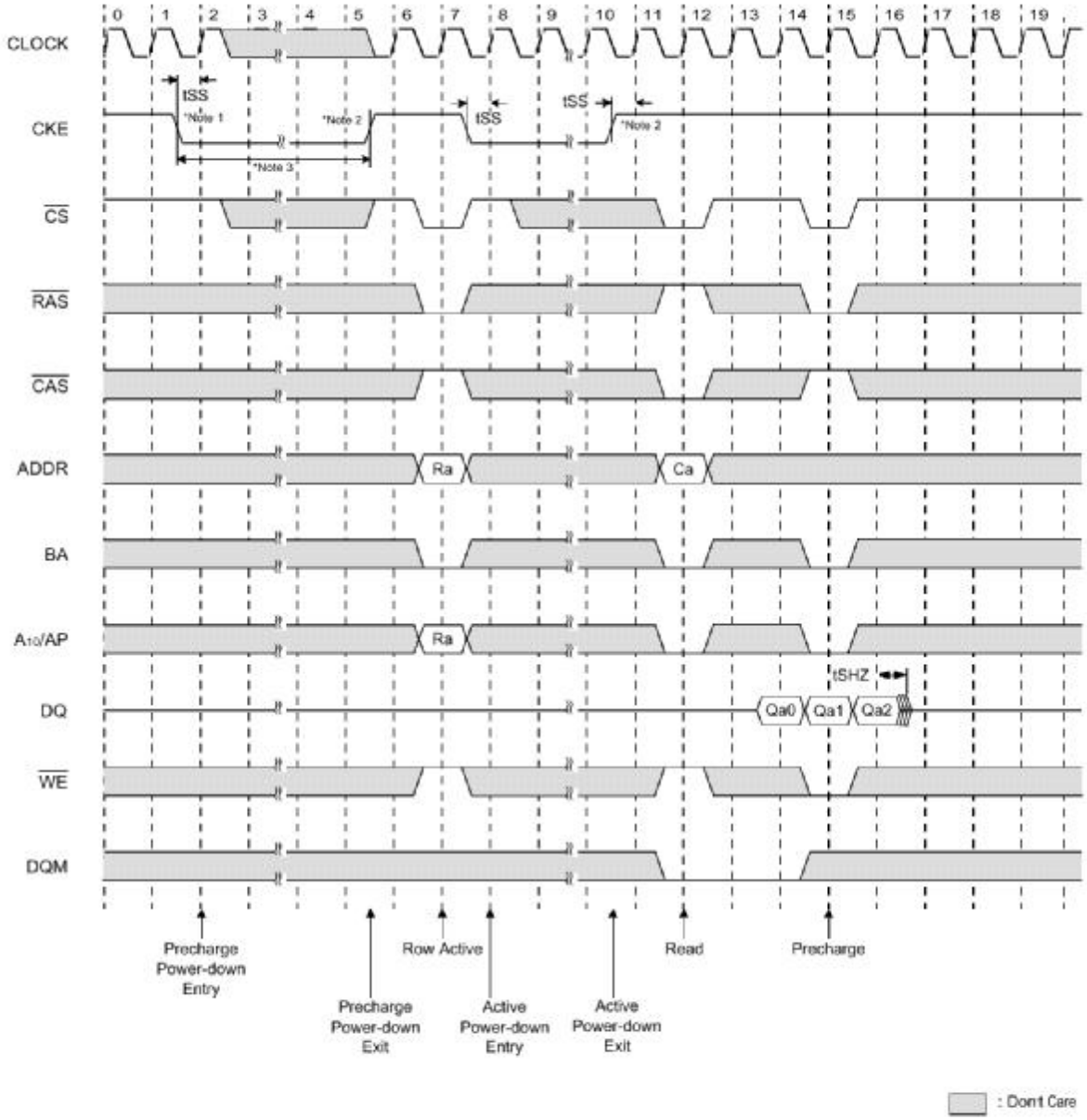
3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



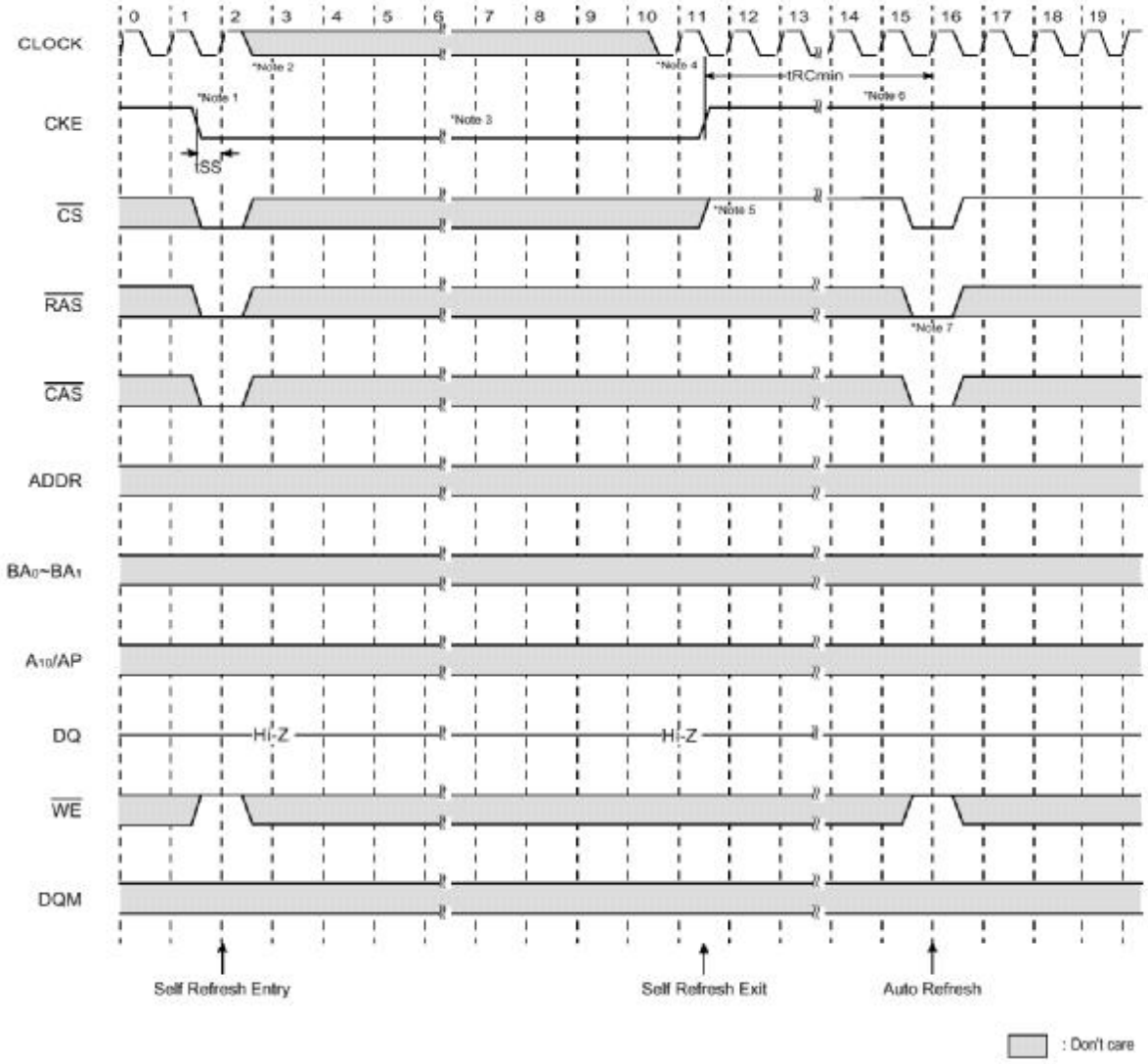
***Note :** 1. BRSW modes is enabled by setting A_9 "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



***Note :** 1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



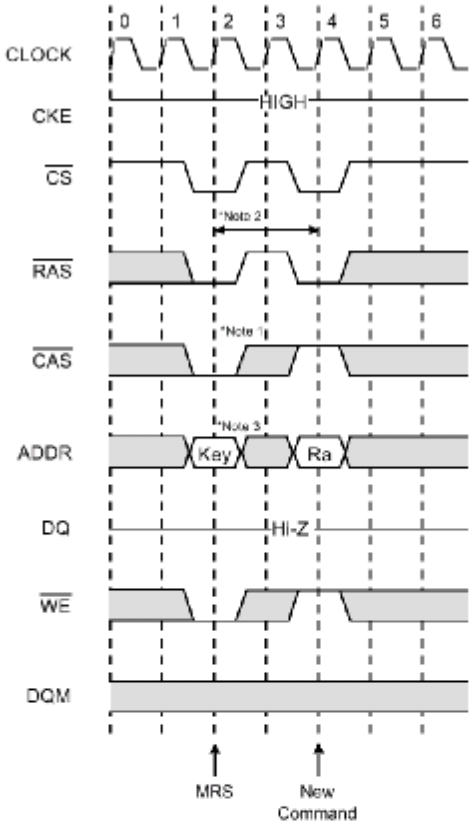
***Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

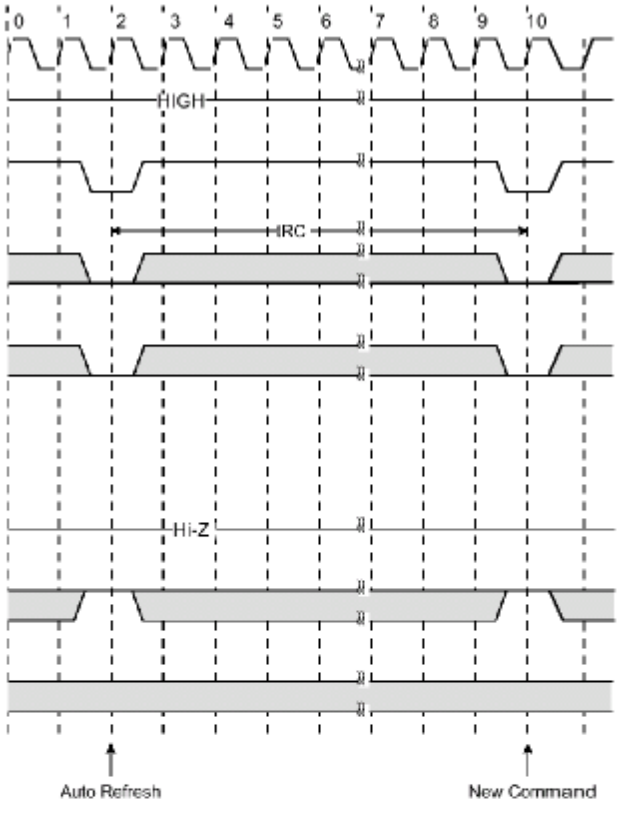
TO EXIT SELF REFRESH MODE

4. System colck restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K cycle(64Mb 5th, 128Mb 2nd/3rd) or 8K cycle(256Mb 2nd) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



: Don't care

* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

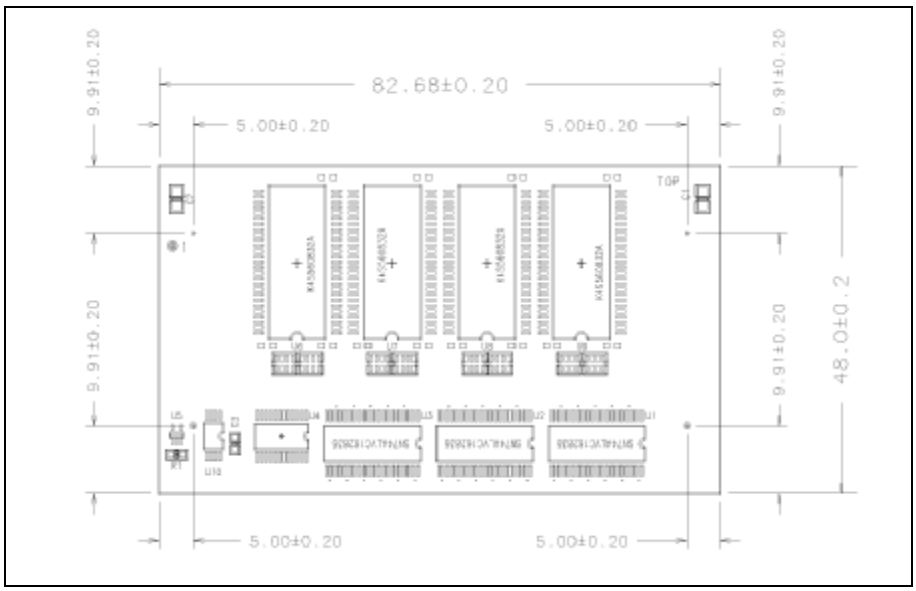
***Note :** 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

PACKAGING INFORMATION

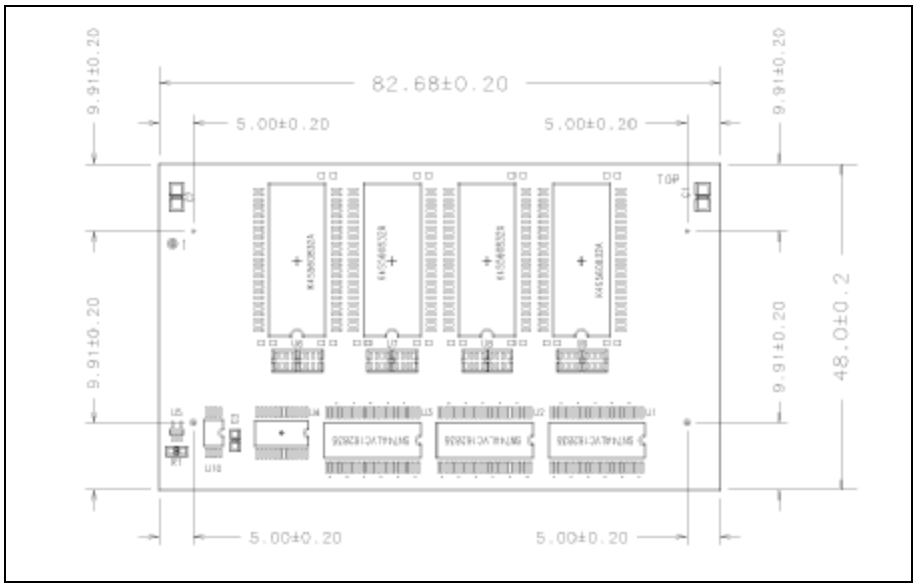
Unit : inch [mm]

Front –Side

TOLERANCE : ±0.008 [±0.20]



Rear-Side



ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HSD16M64F8K-10L	128MByte	16M x 64	120PIN STACKABLE	4K	3.3V		100Mhz