



P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
-20	0.074 @ $V_{GS} = -4.5$ V	-8 ^c	5.6 nC
	0.110 @ $V_{GS} = -2.5$ V	-7.4	

FEATURES

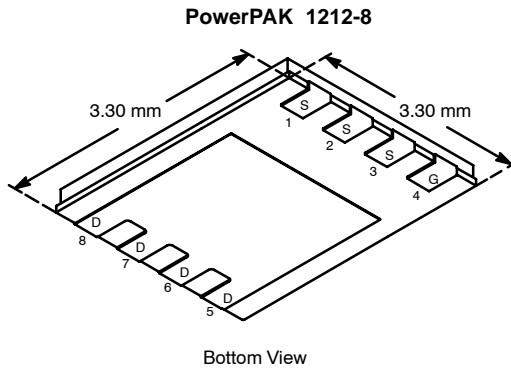
- TrenchFET® Power MOSFET: 2.5-V Rated
- RoHS Compliant
- New PowerPAK® Package
 - Low Thermal Resistance
 - Low 1.07-mm Profile



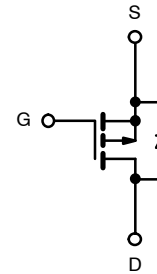
Product Is Completely Pb-free

APPLICATIONS

- Load Switching
- PA Switching



Ordering Information: Si7403BDN-T1—E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^{a, b}	$T_C = 25^\circ\text{C}$	I_D	-8 ^c	A
	$T_C = 70^\circ\text{C}$		-7.2	
	$T_A = 25^\circ\text{C}$		-5.1 ^{a, b}	
	$T_A = 70^\circ\text{C}$		-4.1 ^{a, b}	
Pulsed Drain Current		I_{DM}	-20	
Continuous Source-Drain Diode Current ^{a, b}	$T_C = 25^\circ\text{C}$	I_S	-8	
	$T_A = 25^\circ\text{C}$		-2.6 ^{a, b}	
Maximum Power Dissipation ^{a, b}	$T_C = 25^\circ\text{C}$	P_D	9.6	W
	$T_C = 70^\circ\text{C}$		6.1	
	$T_A = 25^\circ\text{C}$		3.1 ^{a, b}	
	$T_A = 70^\circ\text{C}$		2 ^{a, b}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{c, d}			260	

Notes:

- Surface Mounted on 1" x 1" FR4 Board.
- $t = 5$ sec
- Package limited.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10 \text{ sec}$	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	11	13	

Notes:

- a. Surface Mounted on 1" x 1" FR4 Board.
 b. Maximum under steady state conditions is 81 °C/W.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$		14		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-2		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.45		-1.0	V
		$V_{DS} = V_{GS}, I_D = -5 \text{ mA}$		-0.77		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = -8 \text{ V}$			-100	ns
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -5.1 \text{ A}$		0.059	0.074	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -4.2 \text{ A}$		0.080	0.110	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10 \text{ V}, I_D = -5.1 \text{ A}$		10		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		430		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			55		
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -5.1 \text{ A}$		9.7	15	nC
				5.6	8.5	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -5.1 \text{ A}$		0.95		
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		10		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 2.4 \Omega$ $I_D \cong -4.1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		5	10	ns
Rise Time	t_r			51	75	
Turn-Off Delay Time	$t_{d(off)}$			33	50	
Fall Time	t_f			60	90	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 2.4 \Omega$ $I_D \cong -4.1 \text{ A}, V_{GEN} = -8 \text{ V}, R_g = 1 \Omega$		4	8	
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			40	60	



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			-8	A
Pulse Diode Forward Current	I_{SM}				-20	
Body Diode Voltage	V_{SD}	$I_S = -2.6\text{ A}, V_{GS} = 0\text{ V}$		-0.7	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -4.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		20	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}			8	16	nC
Reverse Recovery Fall Time	t_a			12		ns
Reverse Recovery Rise Time	t_b			8		

Notes

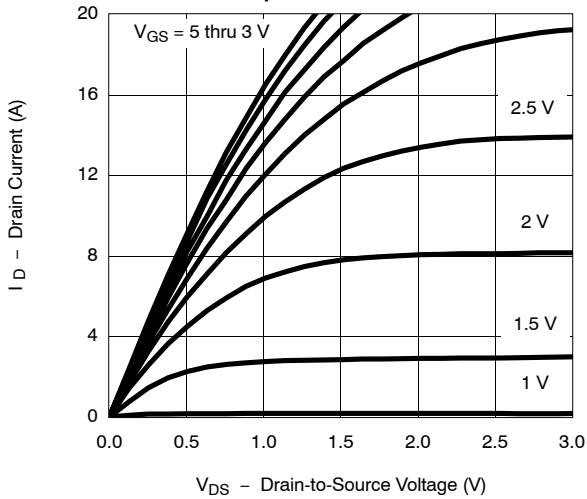
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

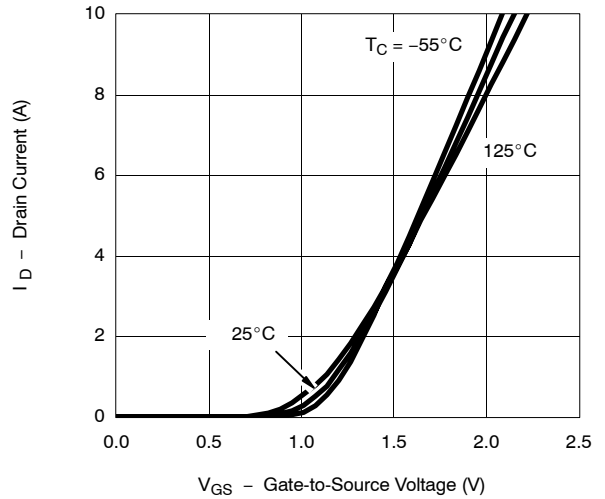


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

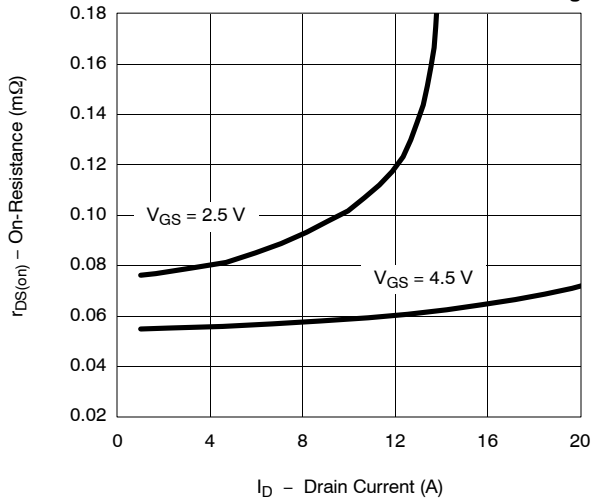
Output Characteristics



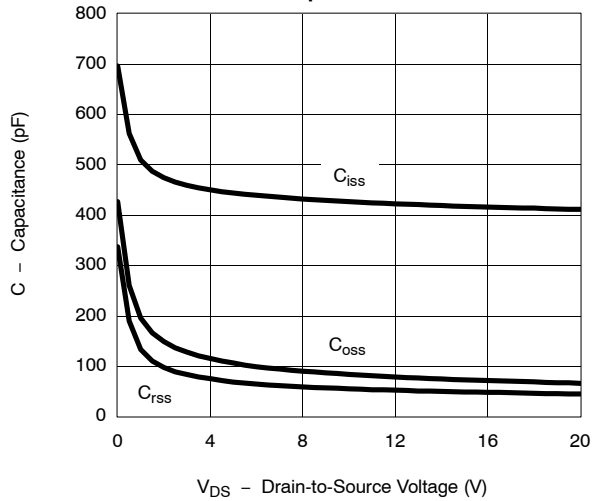
Transfer Characteristics



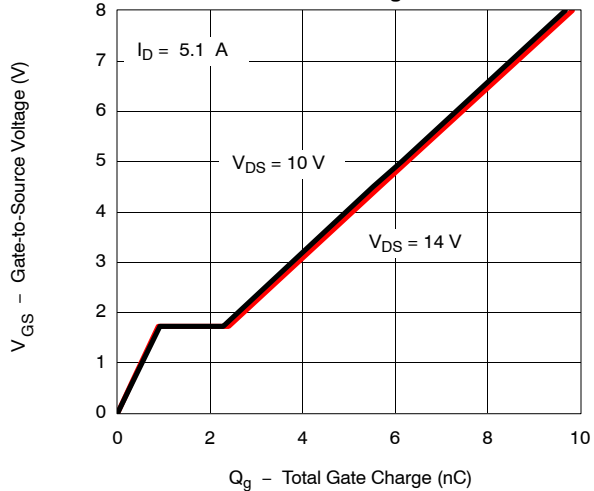
On-Resistance vs. Drain Current and Gate Voltage



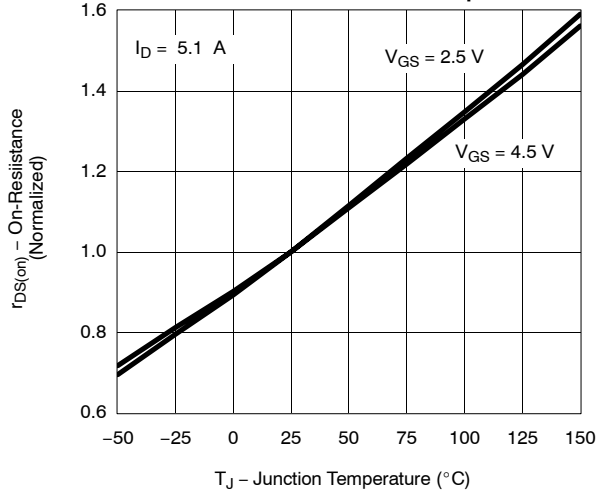
Capacitance



Gate Charge



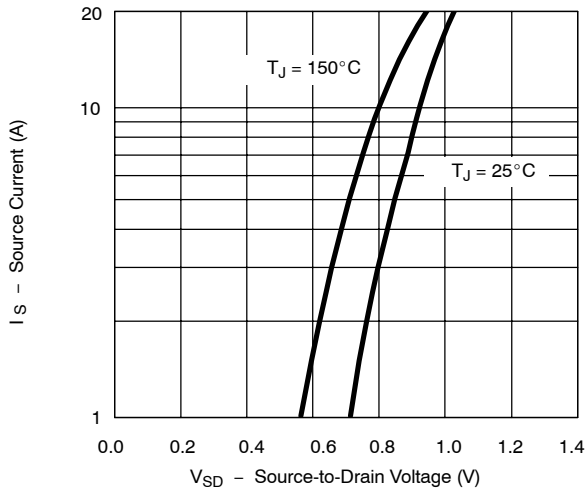
On-Resistance vs. Junction Temperature



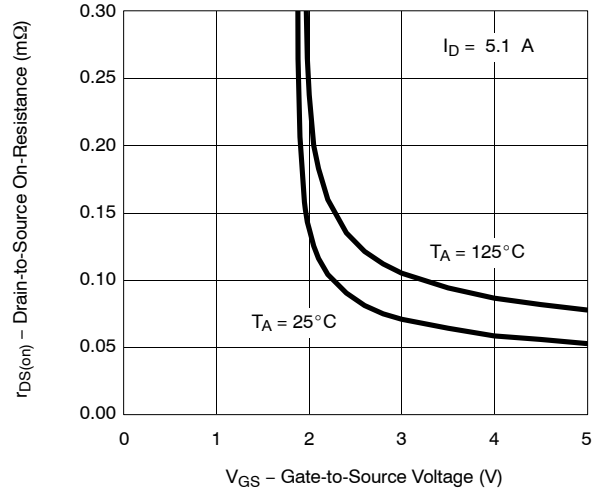


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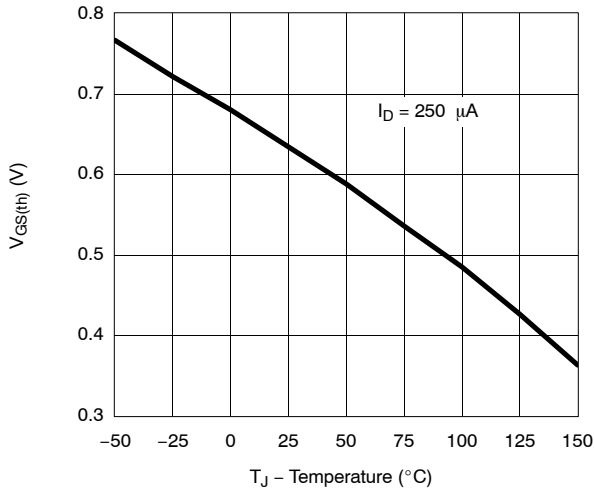
Source-Drain Diode Forward Voltage



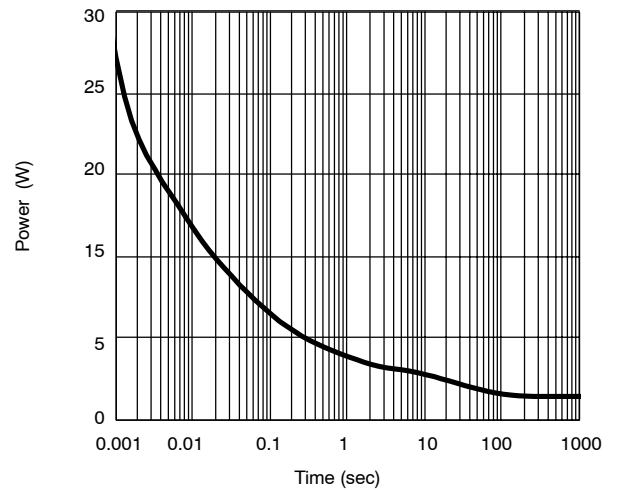
On-Resistance vs. Gate-to-Source Voltage



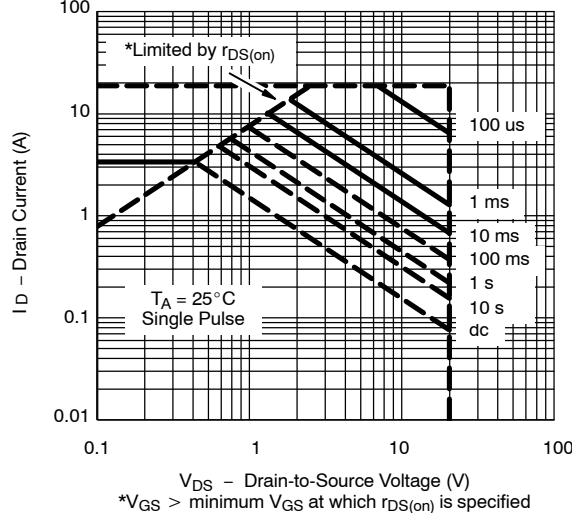
Threshold Voltage



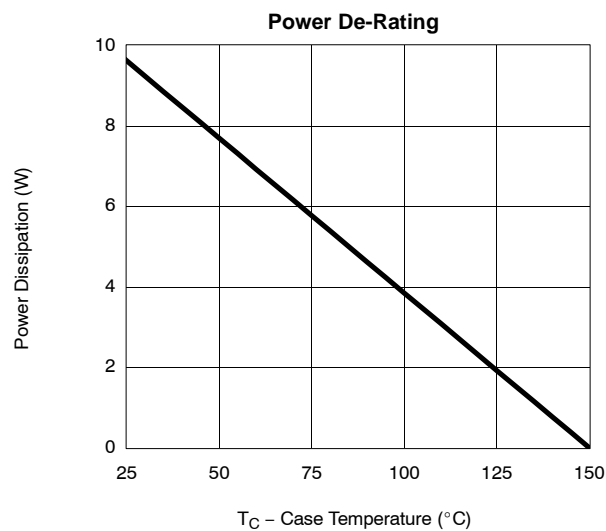
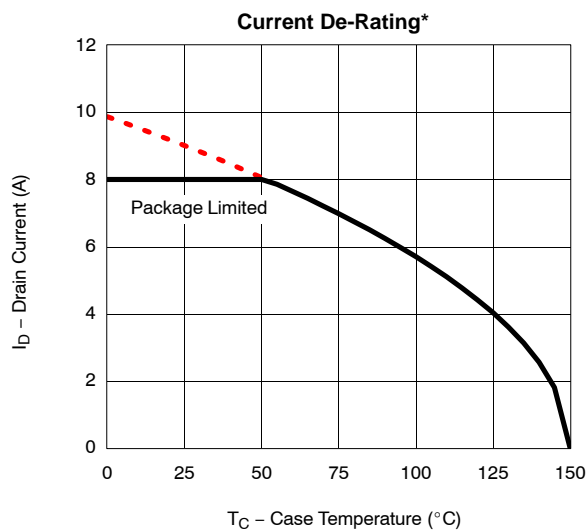
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient



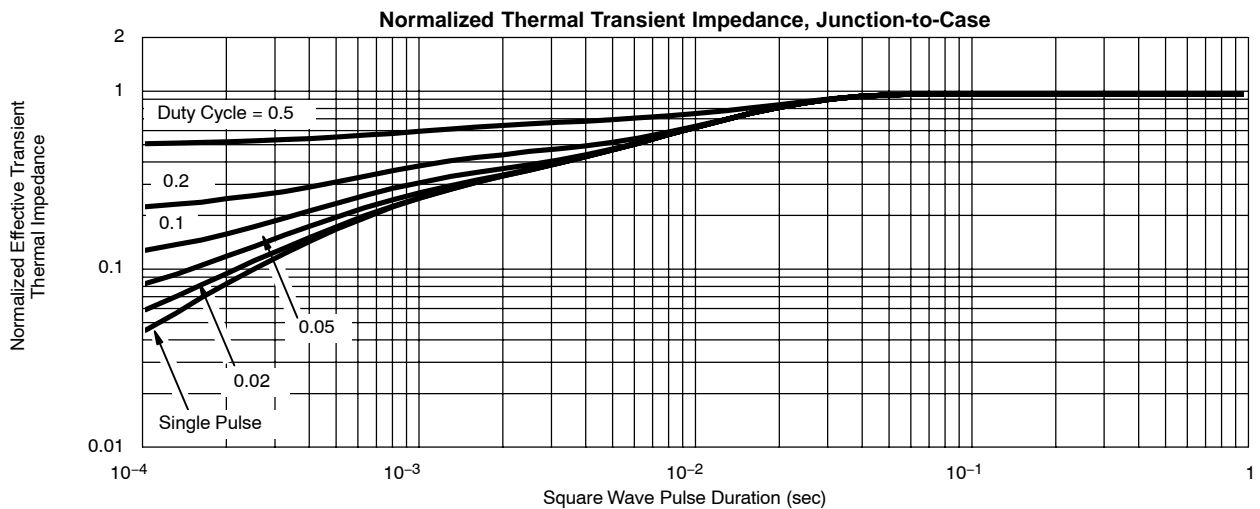
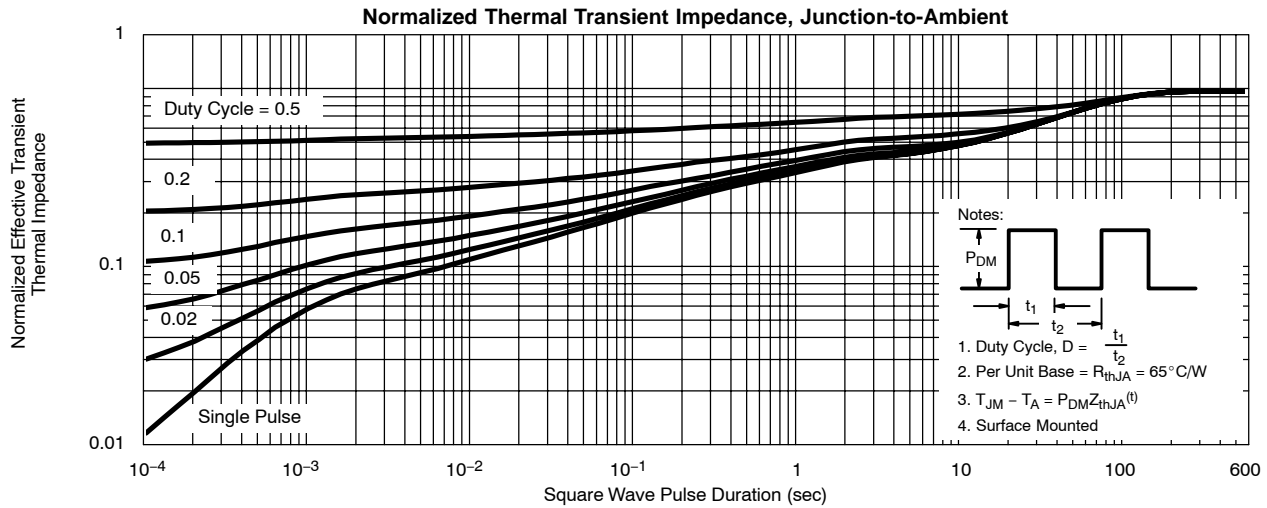
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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