Integrated Circuit Systems, Inc.

ICS95V860

2.5V DDR/Zero Delay Fan Out Buffer (100MHz - 225MHz)

Recommended Application:

DDR Memory Modules / Zero Delay Fan Out Buffer

Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 13 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- PD# for power management
- Spread Spectrum-tolerant inputs
- Auto PD when input signal removed
- 0°C to 85°C operation

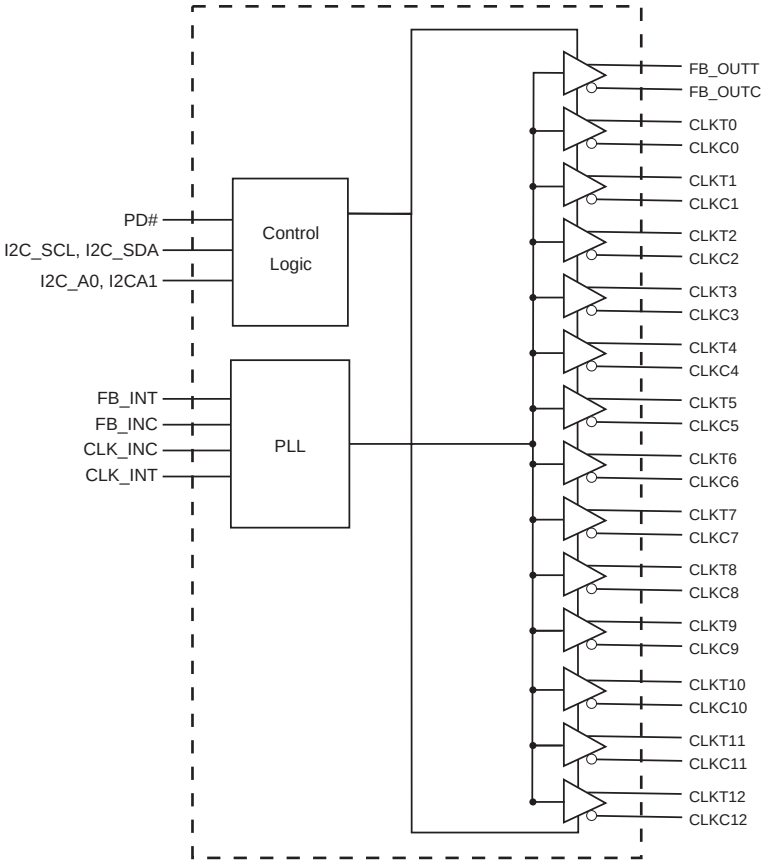
Functionality

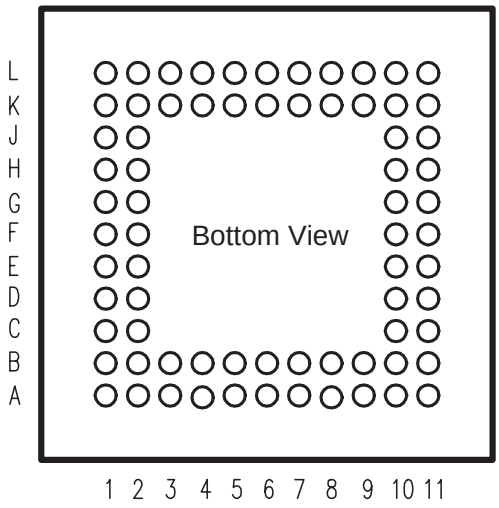
INPUTS				OUTPUTS				PLL State
AVDD	PD#	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	X	X	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz)		Z	Z	Z	Z	off

Switching Characteristics:

- CYCLE - CYCLE jitter (>100MHz):<75ps
- OUTPUT - OUTPUT skew: <70ps
- DUTY CYCLE: 49% - 51%

Block Diagram





	1	2	3	4	5	6	7	8	9	10	11
A	I2C_A0	CLKC0	CLKT0	CLKC1	CLKT1	CLKC2	CLKT2	CLKC3	CLKT3	PD#	VSS
B	I2C_A1	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	CLKC4
C	FB_OUTT	VSS								VDD	CLKT4
D	FB_OUTC	VDD								VDD	CLKC5
E	FB_INT	FB_INC								VSS	CLKT5
F	AVDD	AGND				Top View				VSS	CLKC6
G	CLK_INT	CLK_INC								VDD	CLKT6
H	CLKT12	VDD								VDD	CLKC7
J	CLKC12	VSS								VSS	CLKT7
K	I2C_SDA	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VSS
L	I2C_SCL	CLKT11	CLKC11	CLKT10	CLKC10	CLKT9	CLKC9	CLKT8	CLKC8	VDD_I2C	VSS

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
B3, B4, B7, B8, C10, D2, D10, G10, H2, H10, K3, K4, K7, K8	VDD	PWR	Power supply 2.5V
A11, B2, B5, B6, B9, B10, C2, E10, F10, J2, J10, K2, K5, K6, K9, K10, K11, L11	GND	PWR	Ground
F1	AVDD	PWR	Analog power supply, 2.5V
F2	AGND	PWR	Analog ground.
L10	VDD_I2C	PWR	I2C VDD pin for I2C_SDA, SCL bias.
A3, A5, A7, A9, C11, E11, G11, J11, L2, L4, L6, L8, H1	CLKT(12:0)	OUT	"True" Clock of differential pair outputs.
A2, A4, A6, A8, B11, D11, F11, H11, L3, L5, L7, L9, J1	CLKC(12:0)	OUT	"Complementary" clocks of differential pair outputs.
G2	CLK_INC	IN	"Complementary" reference clock input
G1	CLK_INT	IN	"True" reference clock input
D1	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
C1	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
E1	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
E2	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
A10	PD#	IN	Power Down. LVCMOS input
A1, B1	I2C_A0, I2C_A1	IN	I2C address bits.
K1	I2C_SDA	IN	I2C bus data line.
L1	I2C_SCL	IN	I2C bus clock line.

General Description

ICS95V860 is a zero delay buffer that distributes a differential clock input pair (CLK_INC, CLK_INT) to thirteen differential clock output pairs (CLKT[0:12], CLKC[0:12]) and one differential clock output feedback pair (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INC, CLK_INT), the feedback clocks (FB_INT, FB_INC) the input (PD#) and the Analog Power input (AV_{DD}). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are Tri-Stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL (appproximately 20MHz), the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the (PD#) input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INC, CLK_INT).

(continued)

General Description (Continued)

The **ICS95V860** is able to track Spread Spectrum Clock (SSC) for reduced EMI.

The **ICS95V860** is an I^2C slave/receiver that supports standard and "fast" mode. The **ICS95V860** I^2C interface is compliant to "The I2C-Bus Specification", version 2.1 January 2000 Philips Semiconductors, except that I2C_SDA and I2C_SCL are not 5.0V tolerant, but have a maximum input voltage of 4.2V or V_{DDI2C} + 0.6V, whichever is lower. Register bits control the enable for each output pair and a global enable bit (GLOBALEN#) disables all outputs except the feeback output pair. A low places the disabled output pair in a high impedance state. Outputs are active during power up and are guaranteed to be at the correct duty cycle and period after the clock stabilization time.

Device I2C address = 11001, A1, A0, R/W

I^2C Table: Output Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	A2,A3	CLK0EN	Output Control	RW	Disable	Enable	1
Bit 6	A4,A5	CLK1EN	Output Control	RW	Disable	Enable	1
Bit 5	A6,A7	CLK2EN	Output Control	RW	Disable	Enable	1
Bit 4	A8,A9	CLK3EN	Output Control	RW	Disable	Enable	1
Bit 3	B11,C11	CLK4EN	Output Control	RW	Disable	Enable	1
Bit 2	D11,E11	CLK5EN	Output Control	RW	Disable	Enable	1
Bit 1	F11,G11	CLK6EN	Output Control	RW	Disable	Enable	1
Bit 0	H11,J11	CLK7EN	Output Control	RW	Disable	Enable	1

I^2C Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	L8,L9	CLK8EN	Output Control	RW	Disable	Enable	1
Bit 6	L6,L7	CLK9EN	Output Control	RW	Disable	Enable	1
Bit 5	L4,L5	CLK10EN	Output Control	RW	Disable	Enable	1
Bit 4	L2,L3	CLK11EN	Output Control	RW	Disable	Enable	1
Bit 3	H1,J1	CLK12EN	Output Control	RW	Disable	Enable	1
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	GLOBALEN#	Output Control	RW	Enable	Disable	0

NOTE: GLOBALEN# does not tristate the feedback output pair. The PLL continues to run and maintains lock even though all other outputs are tri-stated
Disable = Output in high-impedance state

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 3.6V
Logic Inputs (except SDA, SCL) . . . . . GND –0.5 V to V_{DD} + 0.5 V
Logic Inputs (SDA, SCL) . . . . . GND –0.5 V to V_{DDI2C} + 0.6 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz		250	290	mA
	I_{DDPD}	Enable = Low, F_{IN} = 0 MHz			200	µA
High Impedance Output Current	I_{OZ}	V_{DD} = 2.7V, Vout=V_{DD} or GND			±10	µA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -1 mA	V_{DD} - 0.1			V
		I_{OH} = -12 mA	1.7V			V
Low-level output voltage	V_{OL}	I_{OL}=1 mA			0.1	V
		I_{OL}=12 mA			0.6	V
Input Capacitance[4]	C_{IN}	V_I = GND or V_{DD}	2.5		3.5	pF
Supply Voltage	V_{DDQ}, A_{VDD}		2.3		2.7	V
I2C Supply Voltage	$V_{DD\ I2C}$	I2C VDD supply pin	2.3		3.6	V
Low level input voltage	V_{IL}	CLKT, CLKC, FB_INC			V_{DDQ}/2 - 0.18	V
		PD#, I2C_A0, I2C_A1	-0.3		0.7	V
	$V_{IL\ I2C}$	I2C_SDA, I2C_SCL	-0.3		0.3 x $V_{DD\ I2C}$	V
High level input voltage	V_{IH}	CLKT, CLKC, FB_INC	V_{DDQ}/2 + 0.18			V
		PD#	1.7		V_{DDQ} + 0.6	V
	$V_{IH\ I2C}$	I2C_SDA, I2C_SCL	0.7 x $V_{DD\ I2C}$		$V_{DD\ I2C}$ + 0.6	V
DC input signal voltage[2]			-0.3		V_{DDQ}	V
Differential input signal voltage[3]	V_{ID}	DC - CLKT, FB_INT	0.36		V_{DDQ} + 0.6	V
		AC - CLKT, FB_INT	0.7		V_{DDQ} + 0.6	V
Output differential cross-voltage	V_{OX}		V_{DDQ}/2 - 0.15		V_{DDQ}/2 + 0.15	V
Input differential cross-voltage	V_{IX}		V_{DDQ}/2 - 0.2		V_{DDQ}/2 + 0.2	V
High level output current	I_{OH}	V_{OH} = 1.7V			-12	mA
Low level output current	I_{OL}	V_{OL} = 0.6V			12	mA
Input slew rate	S_R		1		4	V/ns
Operating free-air temperature	T_A		0		85	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VT-VC] required for switching, where VT is the true input level and VC is the complementary input level.
4. Guaranteed by design, not 100% tested in production.

0675D—01/07/04

Timing Requirements

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input clock frequency	$freq_{op}$		100	225	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			10	µs

Switching Characteristics

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		5.5		ns
Output enable time	t_{EN}	PD# to any output		5		ns
Output disable time	t_{dis}	PD# to any output		5		ns
Period jitter	$T_{jit\ (per)}$		-75		75	ps
Half-period jitter	$t_{(jit\_hper)}$		-70		70	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2.5	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}		-75		75	ps
Static phase offset	t_{spo}		-75	0	75	ps
Output to Output Skew	T_{skew}				70	ps
Duty cycle	D_C[2]		49		51	%

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{WH}/t_C, where the cycle (t_C) decreases as the frequency goes up.

Parameter Measurement Information

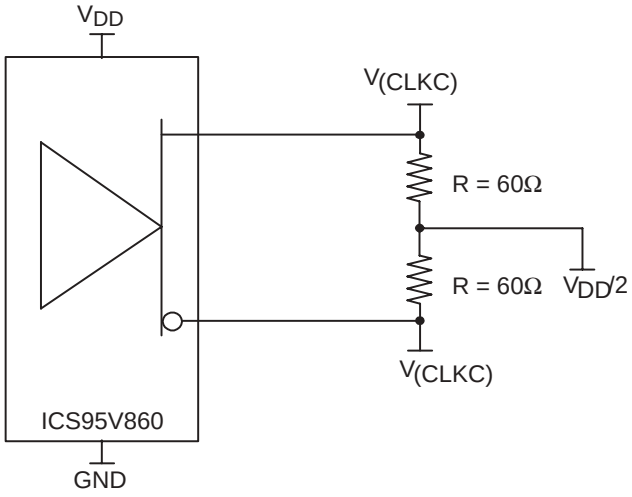
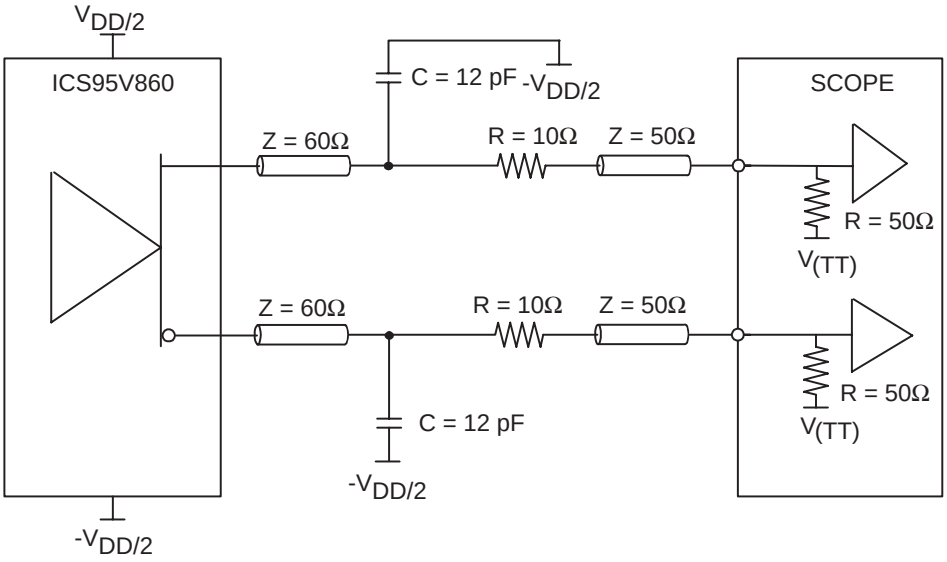
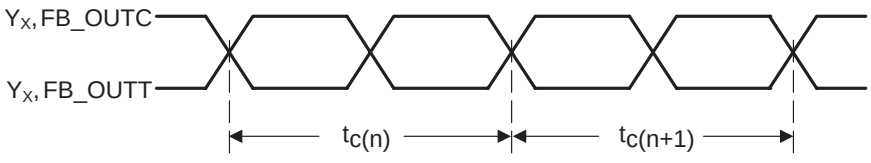


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

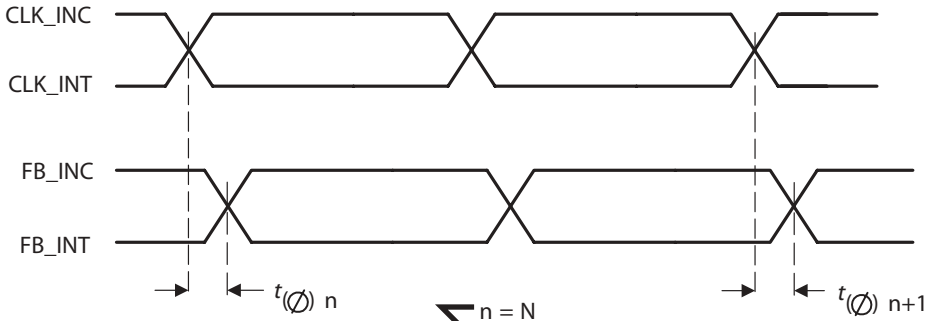
Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information



$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)\ n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

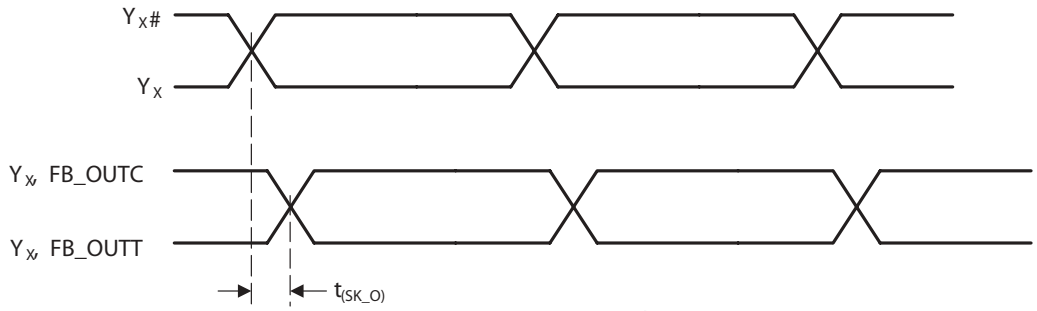
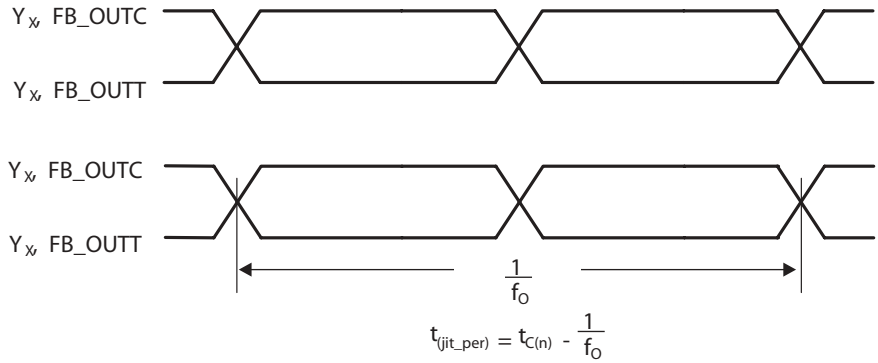


Figure 5. Output Skew



$$t_{(jit\_per)} = t_{C(n)} - \frac{1}{f_O}$$

Figure 6. Period Jitter

Parameter Measurement Information

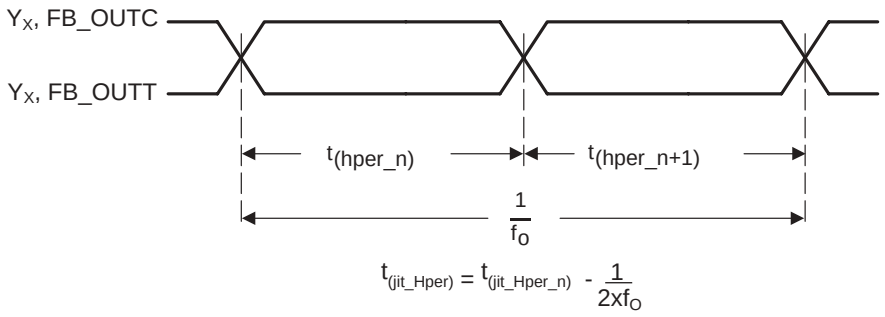


Figure 7. Half-Period Jitter

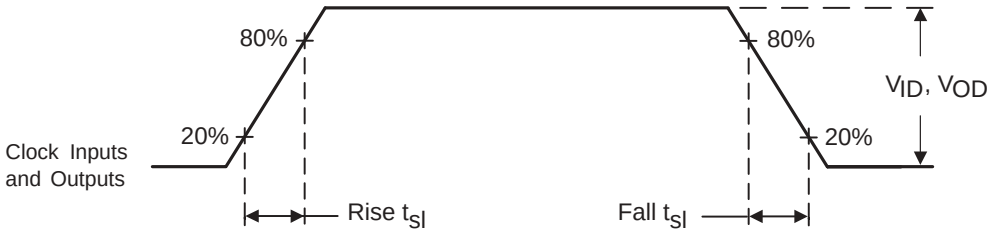
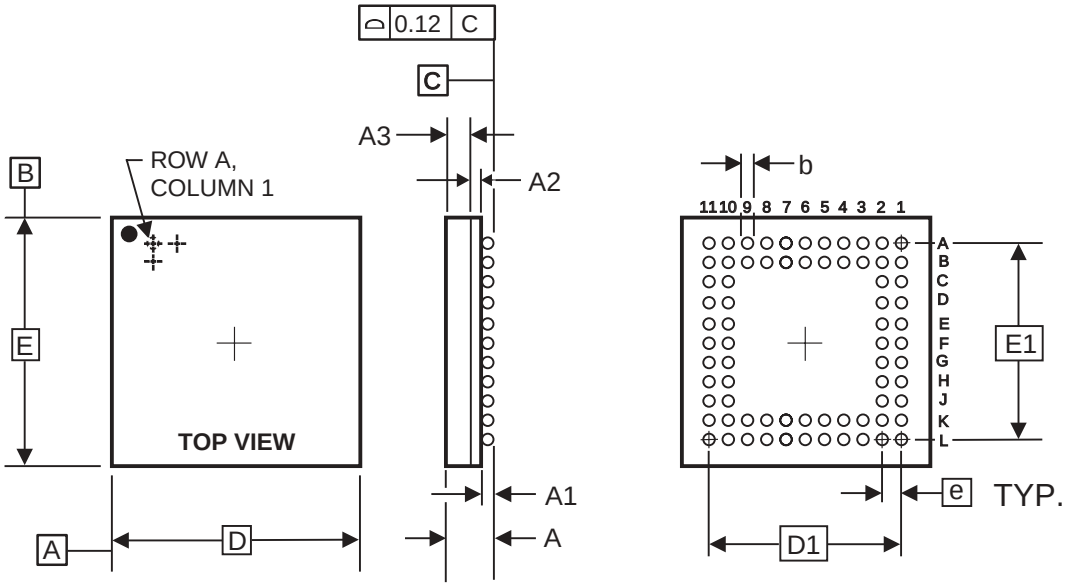


Figure 8. Input and Output Slew Rates



SYMBOL	MILLIMETER			INCH*		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.10	1.20	0.039	0.043	0.047
A1	0.165	0.20	0.235	0.006	0.008	0.009
A2	0.16	0.20	0.24	0.006	0.008	0.009
A3	0.675	0.70	0.725	0.027	0.028	0.029
b	0.25	0.30	0.35	0.010	0.012	0.014
D	7.00 BSC			.276 BSC		
D1	5.00 BSC			.197 BSC		
E	7.00 BSC			.276 BSC		
E1	5.00 BSC			.197 BSC		
e	0.50 BSC			.0197 BSC		

* For Reference Only. Controlling dimensions in mm.

ref.: AIT-R0072MK-01

Ordering Information

ICS95V860yHLF-T

Example:

ICS XXXX y H LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  H = BGA
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0675D—01/07/04